A Compact Threshold-Voltage Model of MOSFETs with Stack High-*k* Gate Dielectric

F. Ji, J. P. Xu*, J. J. Chen, H. X. Xu, C. X. Li, P. T. Lai*

Abstract — In this paper, a compact threshold-voltage model is developed for stack high-*k* gate-dielectric MOSFET with a thin interlayer. The simulated results are in good agreement with 2-D simulations. The influences of *k* value of the interlayer on threshold behaviors are investigated in detail. A low-*k* interlayer can effectively improve the threshold-voltage behaviors. Furthermore, the ratio of low-*k* interlayer EOT (equivalent oxide thickness) to high-*k* layer EOT is optimized by considering both threshold-voltage roll-off and gate leakage current.

Keywords: MOSFET, Threshold voltage, stack gate dielectric

I. INTRODUCTION

High-*k* gate dielectric has become a promising candidate for future nano-scaled MOSFETs. However, both high-*k*/Si [1, 2] and high-*k*/Ge [3, 4] interfaces suffer from unacceptably high interface-state density, thus resulting in low carrier mobility. So, a thin interlayer, e.g. SiON for Si MOS [5] and TaO_xN_y for Ge MOS [6], is needed to improve the interface properties, and thus stack gate-dielectric MOS devices with thin interlayer become attractive.

The threshold voltage of MOSFET with a single-layer high-*k* gate dielectric has been studied widely [7, 8], and however, threshold behaviors of the stack high-*k* gate-dielectric MOSFET are less addressed. In this work, for the first time, a threshold-voltage model of the stack gate-dielectric MOSFET is developed, and the influences of *k* value of the thin interlayer on surface potential and threshold voltage roll-off are discussed in detail. It is found that threshold behaviors of the stack-gate dielectric MOSFET can be improved by using a low-*k* interlayer, and a suitable ratio of equivalent oxide thickness (EOT) of the interlayer to EOT of the high-*k* dielectric layer is required to reduce both threshold-voltage roll-off and gate leakage current.

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II. MODEL DERIVATION

A schematic diagram of the stack high-*k* gate-dielectric MOSFET with a thin interlayer is shown in Fig.1, where T_{ox1} and T_{ox2} are high-*k* dielectric thickness and interlayer thickness respectively (corresponding EOT is denoted as EOT1 and EOT2); $T_{ox} = T_{ox1} + T_{ox2}$ is total gate-dielectric thickness, and x_d is the depletion-region width in the substrate.

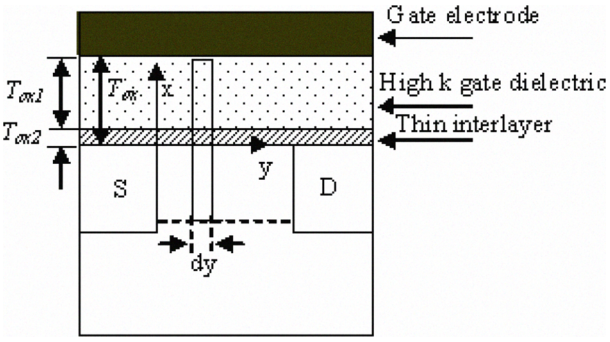

Fig. 1 Schematic diagram of MOSFET with stack high-*k* gate dielectric.

For simplicity, the polysilicon depletion effect and quantum effects are neglected. So, the 2-D Poisson's equation in the depletion region and stack gate-dielectric region can be written as.

$$\frac{\partial^2\varphi(x,y)}{\partial x^2}+\frac{\partial^2\varphi(x,y)}{\partial y^2}=\begin{cases}0, & T_{ox2}\le x\le T_{ox},\\ 0, & 0\le x\le T_{ox2},\\ qN_A/k_{sub}, & -x_d\le x\le 0,\end{cases} \quad (1)$$

where N_A is the doping concentration of p-type substrate; k_{sub} is the permittivity of the substrate. The solution of Eq. (1) can be found to be [7, 8]:

$$\varphi(x,y)=\varphi_0(x)+[\varphi(x,0)-\varphi_0(x)]\frac{\sinh[(L-y)/l]}{\sinh(L/l)}+[\varphi(x,L)-\varphi_0(x)]\frac{\sinh(y)}{\sinh(L/l)} \quad (2)$$

in which L is the channel length; l is defined as characteristic length; $\varphi_0(x)$ is the solution of the 1-D

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Poisson's equation for a long-channel MOSFET.

By applying the Gauss's law to a rectangular box [Gaussian box: dy × (x_d + T_{ox})] from the bottom of the depletion region to the top of the high k dielectric layer via the interlayer, as shown in Fig.1, the characteristic length can be derived as:

$$l^2 = \frac{k_{sub} x_d}{C_{ox}} + \frac{\int_0^{T_{ox}} k(x)[\varphi(x,0) - \varphi_0(0)]dx}{C_{ox}[\varphi(0,0) - \varphi_0(0)]} \quad (3)$$

where k(x) is the relative permittivity somewhere between x = 0 and $x = T_{ox}$, C_{ox} is total gate capacitance. Using boundary conditions: $\varphi(x,0) = V_{bi}$ and $\varphi(x, L) = V_{bi} + V_{ds}$ (V_{bi} and V_{ds} are the built-in potential of drain-substrate junction and the drain-source voltage, respectively), l can be written as:

$$l^2 = \frac{k_{sub} x_d}{C_{ox}} + \frac{C_{ox}\left(\frac{k_{ox2}}{k_{ox1}} T_{ox1} T_{ox2} + \frac{T_{ox1}^2 + T_{ox2}^2}{2}\right)}{C_{ox}} \quad (4)$$

where k_{ox1} and k_{ox2} are the relative permittivity of the high-k dielectric and interlayer respectively. Based on Liu's [7] and our previous work [8], the threshold voltage can be expressed as:

$$V_{th} = V_{th0} - \frac{[2(V_{bi} - 2\phi_f) + V_{ds}]}{2\cosh(L/2l) - 2} \quad (5)$$

in which V_{th0} is threshold voltage of 1-D long-channel MOSFET. Threshold-voltage roll-off resulted from the short-channel effect (SCE) and fringing-field effect (FFE) is defined as:

$$V_{th} - V_{th0} = -\frac{[2(V_{bi} - 2\phi_f) + V_{ds}]}{2\cosh(L/2l) - 2} \quad (6)$$

III. RESULTS AND DISCUSSION

Eq. (5) shows that the threshold voltage is related to the characteristic length, and the larger the characteristic length, the stronger is the FFE. Change of the characteristic length of Si MOSFET with the depletion-region width is depicted in Fig.2 for different gate-stack structures. For Si MOSFET with SiO_2 as gate dielectric, the simulated results exhibit good agreement with that in [9], thus confirming the validity of the model. At a given x_d, the characteristic length for $k_{ox1} = k_{ox2} = 60$ (i.e. single-layer high-k gate dielectric) is larger than that for $k_{ox1} = k_{ox2} = 3.9$ (i.e. single-layer SiO_2 gate oxide), implying a strong FFE in high-k MOSFET. Also, it can be seen that the l of MOSFET with stack gate dielectric of SiO_2 as interlayer is close to that of MOSFET with single SiO_2 as gate dielectric, meaning that the SiO_2 interlayer plays an important role in alleviating the FFE of the stack high-k gate-dielectric MOSFET.

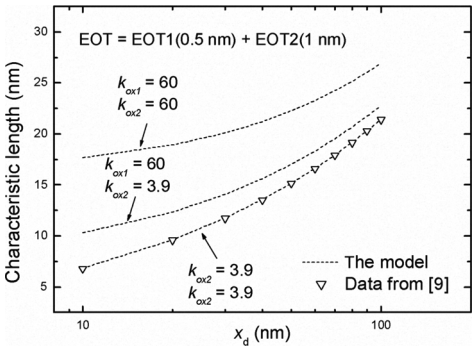
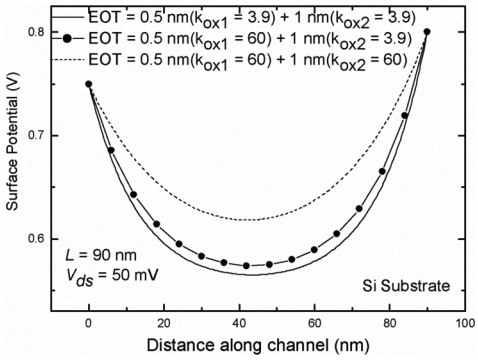
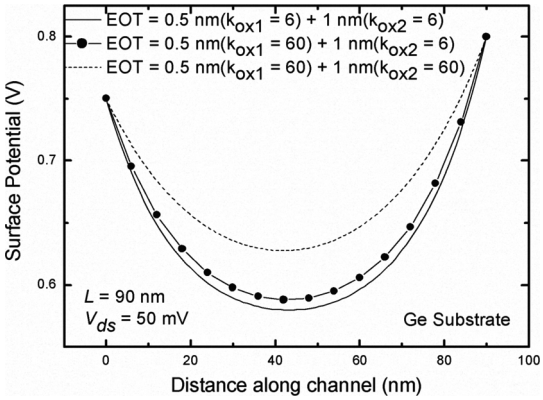


Fig. 2 Characteristic length versus x_d for different k_{ox1} and k_{ox2}

Surface potential of both Si and Ge MOSFETs with single and stack gate dielectric is plotted in Fig.3 (a) and (b) respectively. For the MOSFET with single gate dielectric, it can be seen that the surface potential of the MOSFET is higher for $k_{ox1} = k_{ox2} = 60$ than $k_{ox1} = k_{ox2} = 3.9$. However, the surface potential of the stack-gate dielectric MOSFET with $k_{ox1} = 60$ and $k_{ox2} = 3.9$ is slightly higher than that of MOSFET with $k_{ox1} = k_{ox2} = 3.9$, and much lower than that of MOSFET with $k_{ox1} = k_{ox2} = 60$. Compared with single high-k gate-dielectric MOSFET, the stack gate-dielectric MOSFET with low-k interlayer can alleviate the influence of the fringing-field effect on channel surface potential, thus giving better threshold voltage behaviors.



(a) Si substrate

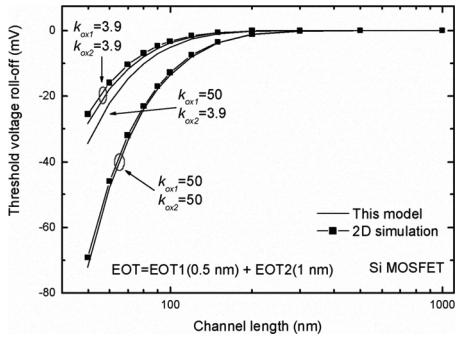


(b) Ge substrate

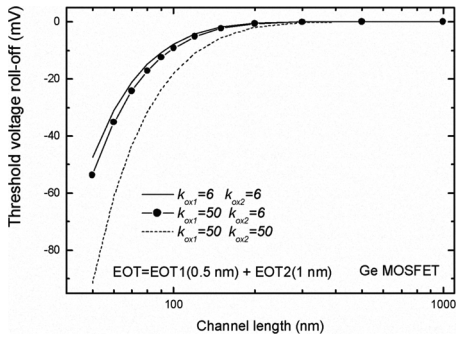
Fig. 3 Surface potential of (a) Si and (b) Ge MOSFETs with single and stack gate dielectric.

Fig.4 shows the dependence of threshold-voltage roll-off on channel length for different gate-dielectric

structures. As L decreases, the threshold voltages of Si and Ge MOSFETs are decreased due to the enhanced fringing-field effect and short-channel effect. For MOSFET with single gate dielectric, good agreement of this model with 2-D simulation [7] verifies the validity of this model. Compared to single high-k gate-dielectric MOSFET with $k_{ox1} = k_{ox2} = 60$, threshold-voltage roll-off of the stack gate-dielectric MOSFET with $k_{ox1} = 60$ and $k_{ox2} = 3.9$ is closer to that of MOSFET with single SiO_2 as gate dielectric, indicating the fringing-field effect of small-scaled MOSFET can be effectively suppressed by inserting a low-k interlayer between the high-k gate dielectric and substrate. The above results show this analytical model can describe the short-channel effect and fringing-field effect of MOSFET with stack-gate dielectric.



(a) Si MOSFET



(b) Ge MOSFET

Fig. 4 Threshold-voltage roll-off of (a) Si and (b) Ge MOSFET with single and stack gate dielectric versus channel length.

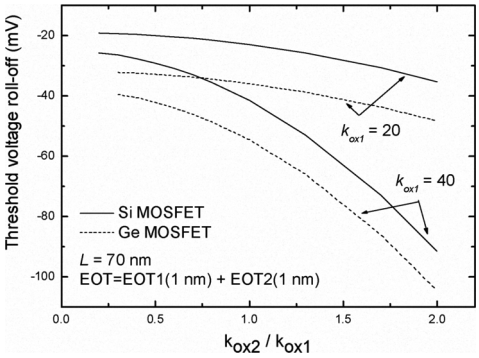
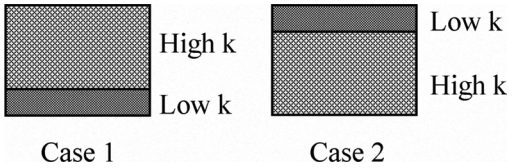


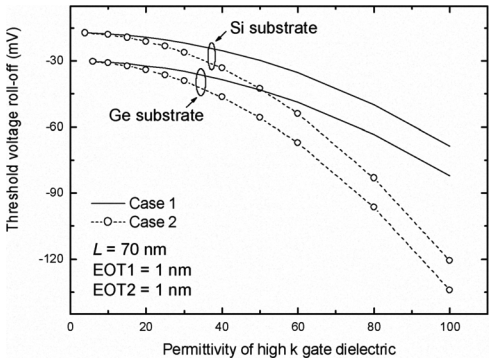
Fig.5 Dependence of threshold-voltage roll-off on k_{ox2} / k_{ox1}

For a given k_{ox1}, as the ratio of k_{ox2}/k_{ox1} increases, the threshold-voltage roll-off is increased (as seen in Fig. 5), which shows a low-k interlayer with good interface quality with Si (e.g. SiO_2) or Ge (e.g. GeON) should be used to improve the threshold-voltage properties.

For two different double-layer gate dielectric stacks, as shown in Fig. 6(a), setting EOT1 = 1 nm, EOT2 = 1 nm and total EOT = 2 nm, the simulated results show that much better threshold-voltage behavior is obtained for the case 1 than the case 2, due to electric field divergence on the top low-k dielectric layer for case 2 [9], as can be seen in Fig. 6(b). This implies that a stable metal gate electrode, which would not react with the underlying high-k dielectric layer to produce low-k interlayer at metal/high-k interface, should be used to improve the threshold-voltage behaviors of MOSFETs.



(a)



(b)

Fig. 6 (a) Two schematic stack gate dielectrics, and (b) threshold-voltage roll-off of corresponding MOSFETs.

Influence of low-k interlayer thickness on threshold-voltage roll-off of MOSFET with stack-gate dielectric EOT of 2 nm is shown in Fig.7. The threshold-voltage roll-off at EOT1 = 0 nm and EOT2 = 2 nm (i.e. single-layer low-k gate dielectric) is mainly resulted from the short-channel effects. For both Si and Ge MOSFETs, as EOT2 decreases (EOT1 increases), threshold-voltage roll-off is increased due to enhancement of fringing-field effect induced by the high-k gate dielectric. So, the thicker the EOT2, the smaller is the threshold-voltage roll-off. On the other hand, larger EOT2 results in smaller total physical thickness of gate dielectric for a given EOT, which would give rise to a larger gate leakage current. Gate leakage current of MOS device with SiO_2 interlayer and HfO_2 ($k \approx 25$) high-k layer was calculated for different EOT1/EOT2 and fixed total EOT of 2 nm [10]. Although gate leakage current is below 10^{-9} A/cm^2 at V_g = -1 V for EOT1/EOT2 = 1.75 nm/0.25 nm [10], threshold-voltage

roll-off is large, as calculated by the above model (solid square symbol in Fig.7). Contrarily, for EOT1/EOT2 = 0.25 nm /1.75 nm, a good threshold behavior is achieved ($\Delta V_{th} \approx 17$ mV, solid circle symbol in Fig.7), but the gate leakage current density (J_g) is larger than 10^{-3} A/cm^2 at V_g = -1 V, which cannot meet the requirement of $J_g < 10^{-3}$ A/cm^2 [11]. Therefore, the ratio of EOT1/EOT2 needs to be optimized for stack gate dielectric. This can be realized by considering a trade-off between gate leakage current and threshold-voltage behaviors. For example, J_g is calculated to be < 10^{-4} A/cm^2 [10] for EOT1/EOT2 of 0.5 nm/1.5 nm to 1.25 nm/0.75 nm, while threshold-voltage roll-off is 18 ~ 22 mV, closed to the value for EOT1/EOT2 = 0.25 nm/1.75 nm (~ 17 mV), as shown by the open up-triangle and open down-triangle symbols in Fig. 7. Thus, the EOT1/EOT2 = 0.5 nm/1.5 nm to 1.25 nm/0.75 nm would be a reasonable choice for gate stack structure.

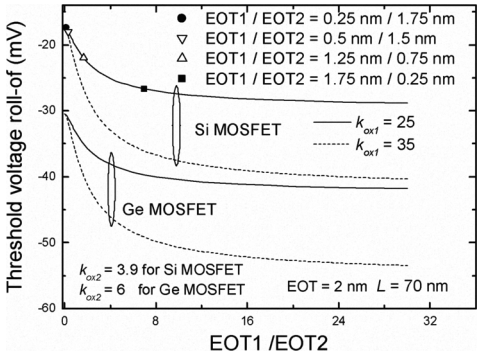


Fig.7 Threshold-voltage roll-off as a function of EOT1/EOT2

IV. Conclusion

An analytical threshold-voltage model suitable for both Si and Ge MOSFETs with stack gate dielectric is derived. Influences of the k value of interlayer on threshold properties are discussed in detail. It is found that when the interlayer is a low-k dielectric, e.g. SiO_2, or GeON, the threshold behaviors of the stack high-k gate-dielectric MOSFET could be improved, but on the contrary, the threshold-voltage roll-off of the MOSFET is increased. Therefore, optimization of the EOT1/EOT2 ratio is required to obtain both small threshold-voltage roll-off and low gate leakage current.

Acknowledgements

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