

Fully transparent organic transistors with junction-free metallic network electrodes

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We utilize highly transparent, junction-free metal network electrodes to fabricate fully transparent organic field effect transistors (OFETs). The patterned transparent Ag networks are developed by polymer crack template with adjustable line width and density. Sheet resistance of the network is 6.8 Ω/sq and optical transparency in the whole visible range is higher than 80%. The bottom contact OFETs with DNTT active layer and parylene-C dielectric insulator show a maximum field-effect mobility of 0.13 $\text{cm}^2/\text{V s}$ (average mobility is 0.12 $\text{cm}^2/\text{V s}$) and on/off ratio is higher than 10^7 . The current OFETs show great potential for applications in the next generation of transparent and flexible electronics. © 2015 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4927445>]

The continuous development of transparent electronics has attracted great attention in the field of the next generation consumer electronics, including “see-through” or “invisible” devices such as transparent sensors or displays.^{1,2} In these transparent electronics, high performance transistors are essential and important elements that govern the overall performance of the device. For example, in commercial displays, although poly-silicon field effect transistors (poly-Si FETs) and amorphous silicon field effect transistors (a-Si FETs) are widely used for the driving and switching functions,³ the opaque nature of silicon and metal electrodes may limit their applications in fully transparent displays. To realize fully transparent transistors, we have to take into account the transparency of all the components, including gate, source, and drain electrodes, dielectric insulator, as well as the semiconductor active layer. Compared with the dielectric and the semiconductor layer, it is more difficult to achieve electrodes with high optical transparency using conventional metallic thin films. In this regard, different transparent conductive electrodes such as transparent conducting oxide (TCO), including indium-tin oxide (ITO),^{2,4,5} aluminum-doped zinc oxide (AZO),² fluorine-doped tin oxide (FTO),⁶ indium-zinc oxide (IZO),⁴ or carbon-based conductors such as carbon nanotubes (CNTs)⁷ and graphene films⁸ have been developed as the transparent electrodes in FETs. However, there are many drawbacks in the application of these materials. For example, brittleness and scarcity of indium in ITO have become a concern for their long-term application in flexible and wearable devices. More importantly, high deposition temperatures of these TCO (usually deposited by sputtering) make them incompatible with polymer based flexible substrates or organic semiconductor active layers. For graphene, since chemical vapor deposition (CVD) approach operates at a high temperature (1000 °C),⁹ extra processing is usually required to transfer the two-dimensional graphene onto the transistor structures, which is especially challenging and tedious for large area fabrication and mass production.

For solution-coated CNT or Ag nanowire films, there is a threshold nanowire density for charge percolation to occur which would, at the same time, increase the surface roughness of the nanowire network.¹⁰ Other than the increase of roughness, the contact resistances at the junctions between the nanotubes or nanowires would also limit the conductivity of these transparent films¹¹ and thus their applications in high performance transistors.

For the active layer materials, organic semiconductors with moderate carrier mobility and high visible regime transparency would have great application potentials in transparent transistors. Different from their inorganic counterparts bonding together by strong covalent bonds, the weak van der Waals interaction between the molecules of thin organic film can provide excellent mechanical flexibility. The “soft” and low processing temperature properties of organic thin films make them suitable for low cost and large area processing such as roll-to-roll fabrications. Recently, thienoacenes based organic semiconductors, such as dinaphtho[2,3-b:2,3-f]thieno[3,2-b]thiophene (DNTT), 2,9-di-decyl-dinaphtho-[2,3-b:2',3'-f]-thieno[3,2-b]thiophene (C_{10} -DNTT), and diphenyl-dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DPh-DNTT) have shown not just high carrier mobilities but also very high stability under ambient air and high temperature environment.¹² The continuous development of the organic semiconductors can provide tailor made properties for flexible electronics such as ambipolar transfer, thermal responses, or optical sensing capability. As a result, if we can develop high performance, low cost transparent electrodes which is compatible with that in the fabrication process of OFETs and produce fully transparent devices, it will be an important step towards the mass production of the next generation of transparent electronics such as displays, optical memories, and smart sensors.

In this work, we optimized a recently developed interconnected crack template masking method¹³ and further combined it with thermal evaporation to obtain a junction-free, highly conductive, and transparent metallic network electrodes. The resulting electrode exhibits better conductivity than ITO and with its sheet resistance (R_s) down to 6.8 Ω/sq and

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the whole visible wavelength regime with transparency higher than 80%. Besides the gate electrode, the highly uniform metallic network electrodes were also utilized as the source and drain electrodes together to develop fully transparent OFETs. Transparent para-chloro-xylylene (parylene-C) and DNNT are used as the dielectric insulator and the active layer, respectively. The transparent OFETs under bottom contact configurations showed a maximum field-effect mobility of $0.13 \text{ cm}^2/\text{V s}$ (an average field-effect mobility of $0.12 \text{ cm}^2/\text{V s}$), subthreshold swing (SS) of 150 mV/dec , and on/off ratio larger than 10^7 . The statistical study of the devices shows consistent performance, which suggests that the patterned junction-free network electrodes are uniformly developed on different regions of the whole substrates. The current fully transparent OFETs can be potentially scaled up for larger area sensor array or digital logic chip applications.

The schematic diagrams of metallic network electrodes fabrication processes are shown in Figure 1. Acrylic resin emulsion (as a template film) is spin-coated on pre-cleaned glass substrate, followed by room-temperature drying to develop highly uniform cracks onto the substrate. By using the crack template as the shadow mask, 50 nm of Ag is thermally evaporated at a growth rate of $\sim 1 \text{ Å/s}$. Then, the sacrificial crack template film is dissolved by chloroform and leaves the junction-free, conductive Ag network electrode. The optical images of the polymer cracks and the metallic network are also shown in Figures 2(a) and 2(b), respectively. The obtained Ag network on glass appears to be well interconnected throughout the whole substrate without any disconnections as shown by the SEM image in Figure 2(c). Through image processing on the optical image, the fill factor of the Ag network is estimated to be around 14% with a wire width of $\sim 2 \mu\text{m}$. The pitch distance (spacing between the Ag microwires) varies from 20 to $80 \mu\text{m}$. Different from staggered junctions commonly seen in solution-processed Ag nanowires electrode, which requires additional post-treatments to improve the contact resistance between the wires, the current Ag network is perforated flat without contact junctions, and thus, the contact resistance can be eliminated which can be confirmed by Figure 2(d). The surface roughness and thickness of the junction-free wires are confirmed to be 4.2 nm and 50 nm , respectively, by atomic force microscopy (AFM) as shown in Figures S1(a) and S1(b).¹⁴ Other than lower sheet resistance of $6.8 \Omega/\text{sq}$, our junction-

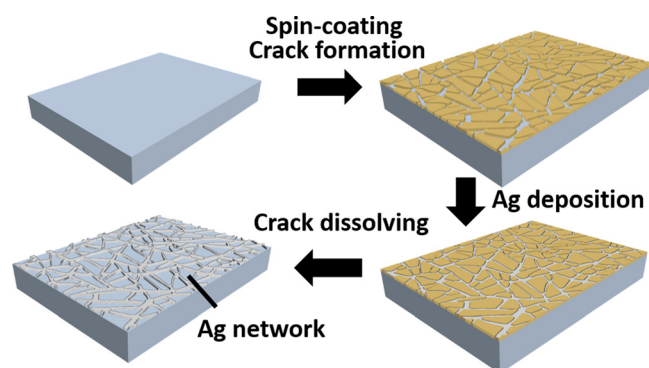


FIG. 1. Schematic procedures for fabrication of metallic network electrode using crack template and thermal evaporation.

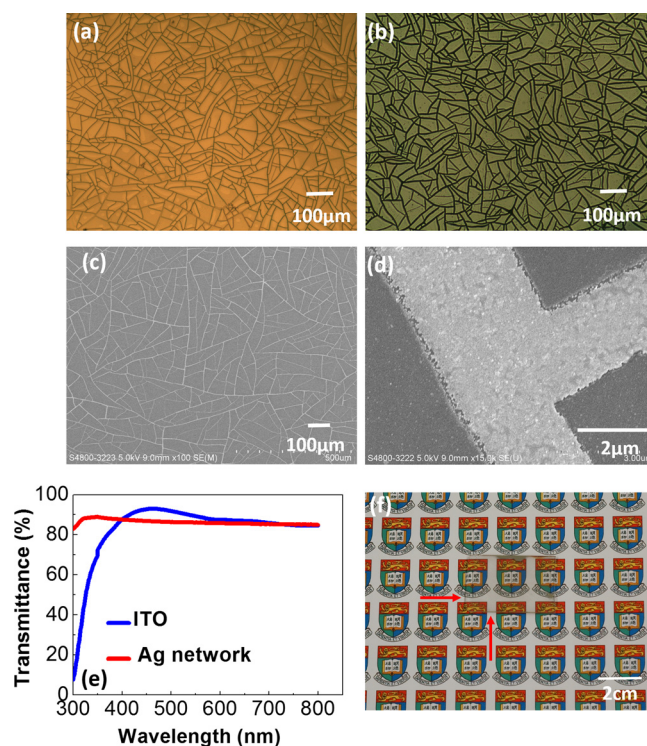


FIG. 2. Optical images of the (a) cracked polymer and (b) Ag network after dissolving the crack template. (c) SEM images of Ag network in (b). Magnified SEM image of the Ag network junction. (e) Transmittance spectra of Ag network and ITO glass substrates. (f) Optical image of Ag network deposited onto glass substrate. The edges of the sample are indicated by red arrows.

less Ag network electrode also exhibits comparable transmittance (86% at 550 nm) with the ITO glass control sample ($14.5 \Omega/\text{sq}$, 89% at 550 nm) (Figure 2(e)). Different from the ITO control sample, the Ag network electrode can maintain high transmittance at wavelength down to the UV region, which highlights its application potential in UV detectors. The high transmittance of the Ag network electrode on glass substrate can be clearly observed from the optical image of the electrode shown in Figure 2(f) (sample is indicated by the red arrow).

To study the feasibility of using this metallic network as general electrodes in OFETs, we first employed it as gate electrode only in OFETs with conventional top source-drain contact pads. The channel width (W) and length (L) of the devices are $3000 \mu\text{m}$ and $100 \mu\text{m}$, respectively. (Thickness and fabrication process of each layer can be found in the supplementary material.) For comparison, we also fabricated devices on glass with ITO gate electrode. The corresponding structures of these two types of OFETs are schematically shown in Figures 3(a) and 3(b), respectively. The parylene-C dielectric and DNNT active layer of all devices are deposited together for direct comparison. It is important to point out that, in fact, the two types of OFET devices are not fully transparent due to the opaque source and drain Ag contacts. The typical transfer curves and output curves of the transistors are shown in Figures 3(c) and 3(d). Our Ag network gate based OFET gives a mobility of $0.154 \text{ cm}^2/\text{V s}$, on/off ratio of 4.21×10^6 , and SS of 236 mV/dec . Other than the drop in the mobility, both on/off ratio and SS of the Ag network gate

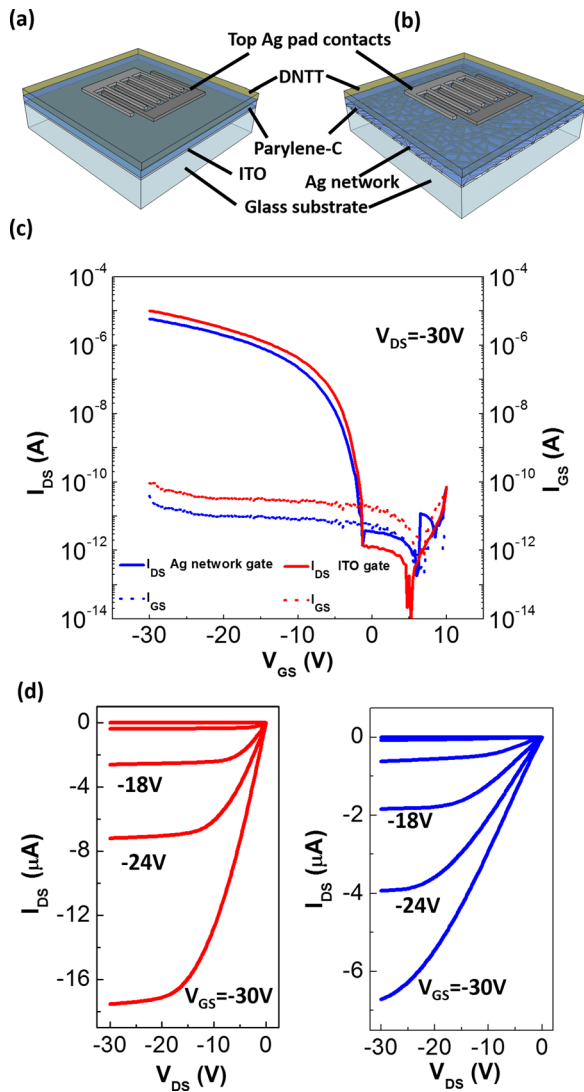


FIG. 3. Schematic structure of top source-drain contact OFETs with (a) ITO gate and (b) Ag network gate electrode. (c) Transfer curves of the transistors with structure shown in (a) and (b). (d) Output curves of the source-drain contact OFETs.

OFETs are comparable with the ITO gate devices (mobility of $0.297 \text{ cm}^2/\text{V s}$, on/off ratio of 8.56×10^6 , and SS of 205 mV/dec). Note that the carrier mobilities here are calculated from the saturation region of transfer curves and the areal capacitance used is 4.71 nF/cm^2 . The capacitance of the parylene-C was evaluated from capacitance–frequency (C - f) plots which will be discussed later.

To develop fully transparent OFETs, we take a step further to modify the device structures by utilizing the transparent Ag network as all the source, drain, and gate contacts of the device, and the structure of the OFET is shown in Figure 4(a). Here, we adapted the bottom source-drain contact structure to avoid the damage to the organic active layer while removing the crack template. We performed C - f measurements of the parylene-C thin film under metal-dielectric-metal (MIM) structure with different contact electrodes, and the obtained C - f results are shown in Figure 4(b). As the parylene-C of all the samples is deposited together, the differences in the measured capacitance can be correlated to the overlapping area of parallel conductive electrodes in the MIM geometry. The relationship between the measured

capacitance C , the thickness of the parylene-C (t), and effective overlapping area (A) can be written as

$$\frac{C_0}{A_0} = \frac{C_1}{A_1} = \frac{C_2}{A_2} = \frac{\epsilon_\gamma \times \epsilon_o}{t}. \quad (1)$$

Here ϵ_γ is the permittivity of free space and ϵ_o is the permittivity of the parylene-C. To facilitate the comparison and analysis between different samples, we use C_0/A_0 to denote the areal capacitance of the parylene-C sandwiched by bottom ITO and top Ag pad ($1.1 \text{ mm} \times 2.1 \text{ mm}$), C_1/A_1 to denote the areal capacitance sandwiched by bottom transparent Ag network and top Ag pad, and C_2/A_2 to denote the areal capacitance sandwiched by two transparent Ag networks. For the 600 nm thick, parylene-C, the measured C_0 at 1 kHz of the parylene-C is 108.8 pF and thus the calculated areal capacitance C_0/A_0 is 4.71 nF/cm^2 , which corresponds to a dielectric constant (ϵ_o) of 3.18 . It agrees well with the reported value in the literature.¹⁵ Note that since this areal capacitance of parylene-C is normalized by the electrode area, it only depends on the thickness of the parylene-C film (600 nm), and the same value is used to evaluate the saturated mobilities of all the mentioned devices. Here, since the transparent Ag network electrodes in the device would significantly reduce the electrode overlapping area, it would be important for us to use Eq. (1) to calculate the real overlapping area under such structure. The measured C_1 at 1 kHz is 15.1 pF , and the overlapping area A_1 is calculated to be 13.9% of A_0 . This is quite consistent with fill factor of Ag network analyzed by optical images. Based on the same method, the measured C_2 is 5.1 pF and we could also extract A_2 , which is equal to 4.68% of A_0 . In this case, since the stacking orientation of two parallel transparent Ag network electrodes is random, the exact overlapping area cannot be precisely control. However, we can evaluate the range of A_2 under two extreme cases. If the stacking of the upper and lower Ag network is exactly the same, A_2 should be close to 14% of A_0 . On the other hand, if the network is completely random with minimized overlap, A_2 should be close to $0.14^2 \times A_0$. The theoretical overlapping area should be in a floating range defined by

$$(F_1 \times F_2) \times A_0 \leq A_2 \leq (F_1 \text{ or } F_2) \times A_0, \quad (2)$$

where F_1 and F_2 are the fill factor of the upper and lower metal network electrodes, respectively. From the C - f measurements of different MIM geometries, we have confidence that the transparent source-drain electrodes are suitable for the proposed bottom contact OFET devices.

In the bottom contact OFETs, it has been observed that the contact resistance between the source-drain electrodes and the organic active layer will cause poor charge injection and lead to discontinuous carrier concentration in the channel.¹⁶ To overcome the charge injection barrier, we deposited pentafluorobenzenethiol (PFBT) self-assembled monolayer (SAM) onto the network based electrodes. The PFBT SAM treatment has been previously employed on different continuous film based metal contacts including Cu, Ag, and Au.¹⁷ It is believed that the strong electron withdrawing character of the PFBT would enhance the work function of the metal

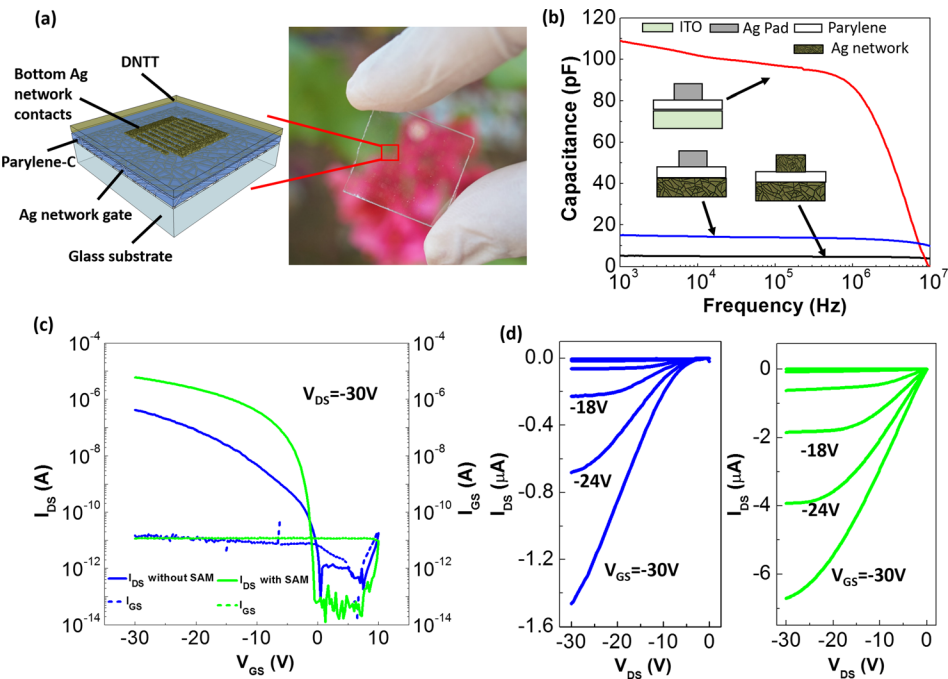


FIG. 4. (a) Schematic structure and optical image of fully transparent transistor device based on Ag network electrodes. (b) C-f results of different MIM structures, ITO/parylene/Ag pad (red line), Ag network/parylene/Ag pad (blue line), and Ag network/parylene/Ag network (black line). (c) Transfer curves and (d) output curves of bottom contact fully transparent transistor without and with PFBT SAM treatment.

electrodes,^{18,19} and thus the hole injection barrier between the metal contact and the highest occupied molecular orbital (HOMO) of the organic semiconductor can be reduced. Here, instead of the continuous thin film metal electrode, we applied PFBT (thiol-SAMs) onto network based electrode, and there was a significant improvement in the charge injection of the bottom contact devices. As shown in the output curves in Figure 4(d), the bottom contact devices with PFBT treatment have much more efficient charge injection from the transparent network contacts, and more linear I-V relationship can be observed at the low source-drain bias regime. Figure 4(c) shows the typical transfer curves of the devices at a drain-source voltage (V_{DS}) of $-30V$ for the bottom contact fully transparent OFETs with and without the PFBT SAM layer. The averaged field-effect mobility in the saturation regime was improved from 0.02 to $0.12\text{ cm}^2/\text{V s}$, while the current on/off ratio also increased from 10^5 to 10^7 and SS decreased from 295 mV/dec to 150 mV/dec . The transparent properties of our OFETs can be observed from the optical image in Figure 4(a), and the optical transmittance of the complete bottom contact OFET device is shown in Figure S2. Compare with commonly observed large absorption around 450 nm wavelength of DNNT, our OFETs show only slight absorption at that region due to the small patterned channel layer in our devices. The performance of all the top contact and bottom contact OFETs is summarized in Table I. Although the effective area of the SAM molecules attached onto the source and drain electrodes is limited by void-like geometry of our network electrodes, the performance of the devices after SAM modification is actually comparable to the top contact devices with opaque top electrodes. From the transfer curves and the histograms of carrier mobilities, on/off ratio of total 25 fully transparent transistors are shown in Figures S3(a)–S3(c) in the supplementary material; it can be noticed that the standard deviation of the carrier mobility is only $0.006\text{ cm}^2/\text{V s}$ (corresponding to 4.9% of the averaged mobility). The on/off ratio of all the devices still maintains a high value above 10^6 .

These results provide direct evidence that the junction-free Ag network developed by the current crack template deposition method is reliable and highly uniform. The overall performance of our devices is comparable with the previously reported transparent OFETs by using CVD-synthesized graphene, single-walled carbon nanotubes (SWNTs), metal grid, or transition metal oxide as transparent electrodes.^{20–23} In comparison with these devices, our transparent junction-free metallic network electrode has a simpler fabrication process, especially no transfer printing, solvent etching, or reactive ion etching are needed to pattern the electrodes. The fully transparent ITO-free OFETs proposed here have great scaling up potential for sensor array, display, or logic chip applications. They can be further integrated with other solution processed high-k dielectric to further reduce their operating voltage and make them suitable for portable usage.

In summary, here we demonstrated fully transparent OFETs by utilizing transparent junction-free metallic network as the electrodes of the devices. The Ag network electrode developed by the crack template method has excellent electric conductivity and optical transparency ($6.8\ \Omega/\text{sq}$,

TABLE I. Transistor performance under various device structures.

Device structure	V_{th} (V)	On/off ratio	SS (mV/dec)	Mobility ($\text{cm}^2/\text{V s}$)
Top Ag pad contacts ITO gate	-7.7	8.56×10^6	205	0.297
Top Ag pad contacts Ag network gate	-6.5	4.21×10^6	236	0.154
Bottom Ag network contacts	-12.6	1.14×10^5	295	0.020
Ag network gate, without SAM				
Bottom Ag network contacts	-3.5	7.59×10^7	150	0.123
Ag network gate, with SAM				

~86%), which is quite comparable to ITO (14.5 Ω/sq , ~89%), suggesting substantial potential as a substitute for ITO. The transparent transistors showed average field effect mobility of 0.12 $\text{cm}^2/\text{V s}$ and SS of 150 mV/dec with a current on/off ratio higher than 10^7 . Having the help from the charge injection SAM, the bottom contact devices show comparable performance with the top contact devices. The current transparent electrodes can provide an alternative path to develop the next generation of ITO-free transparent electronics. Ultimately, the OFETs provide a guide for achieving high performance and high transparency smart sensors or logic chips that can be utilized on different transparent substrates.

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¹⁴See supplementary material at <http://dx.doi.org/10.1063/1.4927445> for fabrication and characterizations details of OFET devices, AFM measurement of Ag network roughness, transmittance measurement of fully transparent OFETs, the transfer curves and the histograms of carrier mobilities, and on/off ratio of total 25 fully transparent transistors.

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