Bi_2O_2Se based MAGIC (Memristor Aided loGIC)

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Abstract

Implementing two dimensional materials into memristor architecture has been a new research focus recently, taking the advantages of their atomic thickness, unique lattice, physical and electronic properties. Among the van der Waals family, Bi_2O_2Se is an emerging ternary two dimensional layered material with ambient stability, suitable band structure and high conductivity, which exhibits supreme potential on electronic application. In this work, we proposed and experimentally demonstrated a Bi_2O_2Se based MAGIC (stands for Memristor Aided logic). Via carefully tuned the electric field polarity of Bi_2O_2Se through Pd contact, configurable NAND gate with zero static power consumption was realized. To provide more knowledge on the NAND operation, kinetic Monte Carlo simulation has been carried out. Due to the NAND gate is a universal logic gate, cascading more NAND gates could exhibit versatile logic functions. In this scenario, the proposed Bi_2O_2Se based MAGIC could be a promising building block for developing next-generation in-memory logic computers with multifunction.

1. Introduction

The modern computer is based on von Neumann architecture, where data shuttled back and forth between processing unit and memory unit. These physically separation represents a fundamental limitation of modern computers, known as the memory wall[1]. To alleviate this issue, methods have been proposed, e.g. cache hierarchies, advanced 2.5D and 3D packaging, and monolithic logic-memory integration, which aim at improving memory access latency, and increasing communication bandwidth between computation and memory units. ~~spatial architectures, where distributed on-chip memory is closer to the computation unit, as well as further scaling of integrated circuits (IC), enabling more transistors placed into the same chip area. However, the current Si-based CMOS technology has encountered significant hardships to continue its revolutionary trajectory based on Moore's law, because of the fundamental thermodynamic limitations at the device physics level and the fundamental quantum mechanical limitations at the material level. Among those methods,~~ Further performance enhancement would rely on novel approaches to break the von Neumann separation and the in memory computing with resistive switching devices seems to be a promising way. The resistive switching devices has aroused worldwide research interest due to its high density, industry compatible fabrication technologies, fast resistive switching and high stability between its high and low resistance states (HRS/LRS). The toggling between HRS and LRS in a resistive switching device is through forming or rupture a conductive filament in its sandwiched metal/insulation/metal (MIM) structure, which typically contains oxygen vacancies in valence change cells (VCM) or ionic metals (such as Ag or Cu) in electrochemical metallization cells (ECM)[2]. Through leveraging their conditional resistive switching properties, logic operations can be executed in multiple device architectures including one memristor-one resistor (1M1R)[3], one transistor-one RRAM (1T1R)[4], one selector-one RRAM (1S1R)[5] as well as complementary resistive switching (CRS)[6]. Based on those structures, noteworthy progress in this area have been achieved, including material implication, 16 logic operations, full adder, flip flop and shifting register[7–9]. Among most of those strategies, additional selecting devices seem requisite for realization of logical functions in memristor architecture. New materials, device architectures or new operation modes are demanded to be further proposed and developed.

Recently the integration of two dimensional materials (2DMs) into memristor has been a new

research focus in the electronic community, ranging from semimetallic graphene[10,11], to the semiconducting transition metal dichalcogenides (TMDs)[12–14], black phosphorus (BP)[15], as well as two dimensional hexagonal boron nitride (h-BN)[16,17], perovskite[18] and MXene[19]. Their dangling-bond-free interface, weak surface van der Waals interaction and atomically thin nature facilitate versatile and fantasy device properties in memristor architectures[20–22]: 1) 2DMs as electrode: for example, graphene with its high in plane carrier mobility and van der Waals interface (dimensional anisotropic, in other words) leads to both high mobility ($10^3 cm^2V^{-1}s^{-1}$) and high on-off ratio (10^7) [23], and also a high thermal stability up to 340 °C[24,25]; 2) 2DMs as insertion layer: via well controlled defect density of graphene layer, the memristor could be switched between fast threshold switching (TS) mode with high on-state current and resistive switching (RS) memory mode of low power dissipation[5]; 3) 2DMs as switching layer: the atomic thin two dimensional insulator, such as perovskite and h-BN, could largely suppressed the leakage current in a metal/insulator/metal (MIM) structure, enable ultra-low operating current[18,26]; moreover, the surface native oxide of 2DMs uniform interfaces, such as SnO_x/SnSe/SnO_x, could also facilitate a random number generation for realization hardware-based Markov chain algorithm[27]; 4) 2DMs based photonic memristor: the supreme surface-to-volume ratio, strong photonic interactions and photo-generated charge trapping of 2DMs lead to non-volatile photonic memristor[28]. Among the 2DMs family, the new emerging layered bismuth oxyselenide (Bi_2O_2Se) have recently aroused lots of attentions in nano-electronic area due to its remarkable environmental stability, suitable band gap and high carrier mobility[29,30]. Determined with theoretical prediction and ARPES mapping, the Bi_2O_2Se exhibited very low in-plane electron effective mass (m^*= 0.14±0.02 m_0 where m_0 is the free-electron mass). This value is much lower than other semiconductor materials including traditional Si (0.26m_0) as well as two dimensional MoS_2 (0.4-0.6 m_0) or black phosphorus (0.15 m_0 for m_x^* and 1.18 m_0 for m_y^*), and thus suggested the promises to achieve ultra-high electron mobility. Experimentally, an ultrahigh mobility of 18500-28900 $cm^2V^{-1}s^{-1}$ at 1.9K has been exhibited in Hall measurements. Moreover, high field-effect mobility up to 1500 $cm^2V^{-1}s^{-1}$ as well as large on/off ratio (10^6), and nearly ideal subthreshold swing of 65 mV dec^{-1} has been realized in transistor architecture. Those outstanding properties indicate Bi_2O_2Se could be a promising material for constructing high speed, low power electronic devices[31]. While, a Bi_2O_2Se based RS device is yet to be experimentally

demonstrated[32,33]. The role of the layered two-dimensional lattice structure Bi_2O_2Se in the RS type devices remain elusive.

In this work, a Bi_2O_2Se based MAGIC (Memristor Aided loGIC) has been proposed and characterized[34]. In the high contact voltage region, a slightly effective Schottky barrier was found at the Pd and Bi_2O_2Se interface. Due to this energy barrier, a small back electrode voltage is requisite for resistive switching to supply sufficient carrier densities injection. Moreover, via carefully modulating the electric field polarities, reconfigurable logic applications could be realized. To provide more knowledge on the Bi_2O_2Se-Pd interfaces and the mechanism of resistive switching, conductive atomic force microscopy and kinetic Monte Carlo simulation have been carried out. Specifically, the logical function realized in Bi_2O_2Se based memristor do not demand additional devices, which largely reduces the fabrication cost and circuit complexity. Thus the Bi_2O_2Se based MAGIC is a promising component toward practical in-memory logic computing and next generation nano-electronic applications.

2. Results and Discussion:

To prepare Bi_2O_2Se based memristor, low pressure chemical vapour deposition (LPCVD) process was carried out to synthesis Bi_2O_2Se (more synthesis details in Experiment), as shown in **Figure 1(a)**, where Bi_2O_3 and Bi_2Se_3 powders were placed in the center and upstream of the chamber to generate vapour sources. Since the freshly cleaved mica exhibits a strong interaction with Bi_2O_2Se, it is a suitable substrate for lateral 2D growth[35]. After synthesis, transferring process was subsequently carried out, where the Bi_2O_2Se experienced including PMMA (poly (methyl methacrylate)) and PDMS (polydimethylsiloxane) coating, baking, water detaching , attaching to SiO_2/Si substrate, and finally acetone and IPA (isopropanol) cleaning (Figure 1 (b)). To check the material phonon vibration, the Bi_2O_2Se have been probed via Raman spectra. As shown in Figure 1 (d), the characteristic A1g peak was observed at 159 cm^{-1} via Raman spectrum probing, which is consistent with previous reports. The Bi_2O_2Se nanosheet is about 15 layers thick considering the theoretical thickness of 0.61 nm. The grain size is around 35 μm, which is sufficient for the subsequent device fabrication. The Bi_2O_2Se crystal in a tetragonal phase (I4/mmm, a =3.891Å, c = 12.21 Å and Z = 2) is shown in Figure 1(c). Within the crystal cell the Bi atom is covalently bonded with O atom to form a Bi_4O tetrahedron, then the tetrahedrons share edges and arrange together to form $[Bi_2O_2]_n^{2n+}$ layers, which are alternately sandwiched with the negatively charged $[Se]_n^{2n-}$ layers. To further confirm its lattice structure, high resolution transmission electron microscope (HRTEM) was carried out. As shown in Figure 1 (f), the Bi_2O_2Se lattice in a cross sectional view, is in highly crystallized as theoretical prediction. After carefully transfer toward SiO_2 substrate, subsequently an Al/AlO_x/Bi_2O_2Se memristor was fabricated, as demonstrated in Figure 1 (d) and the optical microscope image in Figure 1 (g) (more fabrication details in Experiment). 7 nm AlO_x was prepared via pre-deposition of thin seeding Al layer combining with native oxide of top Al electrode. The AlO_x served as a resistive switching medium, and the Al and Bi_2O_2Se serve as top and bottom electrode (TE and BE for short) respectively. Pd is chosen as the metal contact for Bi_2O_2Se due to its similar work function (5.1 eV) with Bi_2O_2Se (5.0 eV). Additional Pd contact leads to three-terminal memristor architecture, enabling more electrical measurements and device functions based on the Pd/Bi_2O_2Se interface.

Figure 2 demonstrated the basic properties of Bi_2O_2Se based memristor. For generic RS memristor, the voltage was applied from TE side vertically and the BE side was normally grounded. While for the Bi_2O_2Se based memristor, the voltage given at the BE side is found requisite and highly related to the RS behaviours, as illustrated in the Figure. Started from the forming process, this initialization step is to create a conductive path to bridge the Al TE and Bi_2O_2Se BE, where compliance current was set as 10 μA to prevent permanent oxide hard breakdown. With two different voltages applied to the BE terminal (V_{BE} for short), the different forming processes reflect on different IV curves, where the high V_{BE} brings high injection current (from 10^{-7} A) of the BE terminal and leads to smaller set voltage 1.76 V, while the low V_B leads to much lower injection current (initial from 10^{-11} A) and a much higher set voltage located at 3.36 V. Since the BE voltage is applied to the Pd contact, it is necessary to understand the electrical characteristics of the Pd-Bi_2O_2Se interface. Figure 2(b) shows the IV sweeping curves of the two Pd contacts. The voltage sweeping was ranged from -1 V to 1 V, and no hysteresis effect is found during the voltage sweeping, indicating good interface properties in the system. In the low voltage region from – 100 mV to 100 mV, the current is linearity, which is consistent with previous reports. But for the higher voltage region (e.g. from ± 100 mV to ±500 mV), the IV curve becomes slightly nonlinearity. As illustrated in Figure 2 (a), the nonlinearity could be originated from thermionic emission, thermionic field emission and field emission (direct tunnelling)[36]. The effective Schottky barrier height (SBH) could be fitted with the following equation:

$$I = AA^{*}T^{2}e^{\frac{\emptyset_B}{k_BT}}, \quad (1)$$

where A is the effective area, A^{*} is the Richardson constant, T is the temperature (300K), and k_B is the Boltzmann constant. Effective Schottky barrier height $\emptyset_B$ could be derived as 0.078 eV and 0.066 eV for negative and positive branches respectively. After considering lattice structures, work function matching and the SBH, the transition from linearity to slightly nonlinear IV curve could be explained as following: in the small voltage region (within ± 100 mV), the current was concentrated at the surface Se layer and the ohmic contact was formed due to the work function matching between the interfacial Se layer of Bi_2O_2Se and the Pd contact. As for the higher voltage region (± 100 mV to ± 1 V), the current flow is not only limited within the interfacial Se layer but also penetrated into Bi_2O_2 layer. Then the current flow encountered the intrinsic energy barrier

between Se layer and Bi_2O_2 layer, leading to the formation of nonlinear IV curve in both negative and positive branches. The derived effective SBH is much smaller than the band gap of Bi_2O_2Se is due to the edge contact structure between Bi_2O_2Se with the Pd contact, which compensates most of the current rectification effect induced by the SBH.

Based on the knowledge of the Bi_2O_2Se interface, the influence of the V_B bias on the RS behaviour has been explored, including the -0.5 V, -0.1 V, 0 V and 0.5 V, as exhibits in Figure 2 (c, e-g). As for the case of 0 V V_{BE}, significant unstable tunnelling current during the set process has been obtained, which has not been found in other conditions. It indicated that the V_{BE} bias is requisite for guaranteeing sufficient carrier densities for RS process. In this scenario, -0.1 V V_{BE} is chosen for a normal case of the Bi_2O_2Se based memristor to analysis its RS phenomenon and explore the memory characteristics. A typical IV curve containing set and reset process is shown in Figure 2 (c), where the set voltage located at 2.38 V. Through analysis the electrical behaviour before set, more knowledge of the conduction within oxide layer and the interface of Bi_2O_2Se and AlO_x layer could be derived. There are three typical conduction modes within the oxide layer, which is based on the relationship between injected carriers (n_I), free carriers in thermal equilibrium (n_0, assuming T=300 K), and intrinsic defects or trap (n_T)[27,37]: the first region (approximately from 0 to 2 V) is in the Ohmic conduction ($I \propto V$), where $n_I+n_0<n_T$, followed with two short regions (approximately from 2 to 2.2 V and from 2.2 to 2.3V) in space-charge-limited-current conduction (SCLC, $I \propto V^2$) and trap-filled limited (TFL, $I \propto V^3$) conduction regions, where $n_I+n_0>n_T$, and $n_I>n_0$, $n_I>>n_0$ respectively. The low HRS current (in the 10^{-11} A level) could be attributed to both the good quality of AlO_x layer to suppress the leakage current and also the two dimensional interface of Bi_2O_2Se and AlO_x layer. Note that Bi_2O_2Se demonstrates obvious characteristics of 2D materials, but different from vdW layered materials such as graphene and MoS_2, the interaction between $[Bi_2O_2]_n^{2n+}$-$[Se]_n^{2n-}$ layers is electrostatic force instead of vdW force. Thus the unique strong injection region in other two dimensional material based memristor has not been found in the current study. Then reliability test were carried out including static reset current and power distribution (ranged from 100nA (nW) to 1μA (nW)), retention up to 1800s for both HRS/ LRS (Figure 2 (d)), and endurance up to 100 DC resistive switching cycles (Figure 2 (e)). Those characteristics guarantee its robustness for the following logical operations. The key to realize the logical operation is to configurable control the set

voltage. As demonstrated in the Figure 2 (e,g), via providing two different V_{BE} bias (±500 mV), two distinct RS IV curve has been obtained. The dynamically tuning switching window is the key to realize logical operations in the current study, which will be analysis in the following study.

Based on electrical measurements, BE voltage was found to highly related with the Set behaviour. To support this scenario and obtain more knowledge on the Bi_2O_2Se and Pd interface, a conductive atomic force microscopy (C-AFM, NT-MDT Solver P47, SP-47) was carried out in this section, as illustrated in **Figure 3 (a)**. To match with the CAFM probe stations, additional sample preparation were taken including cm-level electrode pre-pattering and Pd contact pad deposition, where the tip is physical contact with the Bi_2O_2Se sample and the metal pad connect with the sample holder. When a potential difference is applied between the tip and the sample, the currents across the sample can be recorded[38]. Different voltages, ranging from ±1 V, ±0.5 V, ±0.3 V, ±0.1 V, were applied on the Pd side and the top electrode probe on the Bi_2O_2Se surface to collect tunnelling current, where the scanning area is 3×3 μm^2 with 512 by 512 points (figure 3 (b, e-l)). Based on the current mapping, the current was found negatively and linearly related with the applied voltages. While for the local range from -0.5 V to -0.1 V and 0.1 V to 0.5 V, there is some non-linearity. This slightly non-linearity is in highly consistent with the electrical measurement, where small SBH exhibits in small voltage range in both negative and positive branches. The arithmetical mean deviation Ra and the root mean squared Rq are also obtained via current mapping. As exhibited in Figure 3 (c-d), the Ra and Rq values are in highly uniform, revealing that the two-dimensional Bi_2O_2Se surface is highly homogeneity and uniform. Moreover, the repetitive scanning at the atmosphere environment did not invoking detrimental effects onto the Bi_2O_2Se surface.

In this section, the Bi_2O_2Se based MAGIC has been experimentally demonstrated, containing a kinetic Monte Carlo simulation. The two resistant states of the Bi_2O_2Se based memristor, HRS and LRS, could be naturally seen as the out binary state (Y), “1” and “0” after logical operations, as shown in **Figure 4 (a)**. To realize logical operation, conditional inputs correlated with different output resistant states are requisite. Based on the above electrical measurements and materials analysis, the set window could be dynamically tuned by the V_{BE} bias. Thus the different V_{BE} and

V_{SET} values could be seen as two conditional inputs, “A” and “B”, where the ± 0.5 V V_{BE} and 2.5 V/0 V V_{TE} could be seen as binary “1” and “0” for “A” and “B”. After carefully chosen the V_{BE} and V_{TE} values, a NAND operation could be realized in the Bi_2O_2Se based memristor, where the truth table and operation algorithm are exhibited in Figure 4 (b). Considering the NAND gate is a universal gate, more logical functions could be realized via cascading NAND gates[8]. The current Bi_2O_2Se based MAGIC exhibits in-memory computing fashion, which owns at least three unique advantages as list below: i) zero static power dissipation because no power supply is needed to maintain its logical states[39]; ii) reconfigurable and stable, as demonstrated in Figure 4 (c); iii) no additional selecting devices are needed. As for the traditional silicon based one-diode-one-resistor structure, to fabricate the epitaxial silicon based selecting device, additional high temperature process is requisite. To provide more understanding on the logical operations, a kinetic Monte Carlo (KMC) simulation based on trap-assisted-tunnelling (TAT) model has been carried out[40,41]. The physical models including oxygen vacancy generation, injection, hopping, dynamic migration, recombination, and temperature updating, are described in the supporting information in detail[42]. As demonstrated in Figure 4 (d-m), the comparison of different V_{BE} polarity are visualized including the revolution and distribution of oxygen vacancies, electric fields, current densities, and temperatures. Under same V_{TE} value (1.7 V), different V_{BE} (± 0.5 V) lead to different resistive switching behaviours. These simulation results consistent with the electrical measurements, supported the logical operation algorithm, as well as provided more knowledge of the filament formation under different electric filed polarity at atomic level.

3. Conclusion

Briefly, Bi_2O_2Se based MAGIC has been proposed and experimentally demonstrated in the current study. The small SBH in the interface of Bi_2O_2Se and Pd contact and related the V_{BE} bias are found influential on the resistive switching behaviour. Via carefully chosen the V_{BE} and V_{TE} values, an in-memory logical computing algorithm has been realized. The surface probing via CAFM and a KMC simulation results consistent with the electrical measurements and also provide more knowledge on the Bi_2O_2Se surface as well as the resistive switching process. The current Bi_2O_2Se based MAGIC enables in-memory computing with reconfigurable and stable

logical operations, as well as zero static power dissipations, which facilitate constructing the field programmable circuit fabric, and is also highly desired in the areas including edge computing, wearable sensors, and the Internet of Things (IOT).

4. Experiment

***CVD synthesis of Bi_2O_2Se on Mica*:** The 2D Bi_2O_2Se nanosheets were synthesized in a low-pressure CVD furnace equipped with a 3 inch diameter horizontal quartz tube and three temperature controlled zones. Powders of Bi_2O_3 and Bi_2Se_3 as precursors were placed in the central zone and upstream of the chamber with a distance of 8 cm, respectively. Ar gas was used as the carrier gas to transport the vaporized precursor to the targeting growth location of mica with a distance of 12 cm downstream. The tube was sealed, evacuated, and flushed with pure Ar gas to provide an oxygen-free environment. Typical growth conditions are described below. The temperature of Bi_2Se_3 source was 500 ℃. The system pressure was controlled at 100 Torr and the flow rate of the carrier gas was 200 sccm. Growth time ranged from 10 to 40 min. After the deposition was complete, the furnace was cooled naturally to room temperature and the quartz tube was refilled with Ar gas to reach atmospheric pressure.

Characterization of the Bi_2O_2Se nanosheets: After the material synthesis and transferring, A RAMaker confocal Raman spectrum with 100x objective lens with 473 nm excitation laser was carried out to probe its lattice information, where the spot size was approximately 0.5μm. A focused ion beam (FIB) in a dual beam microscope was employed to obtain the cross sectional images of the Bi_2O_2Se. The following lattice detecting was obtained via a high resolution transmission electron microscope (TEM, JEM-2100F, acceleration voltage 200 kV).

Fabrication of the Bi_2O_2Se based electronic device. Initially, a poly (methyl methacrylate) (PMMA) and polydimethylsiloxane (PDMS) assisted transfer was carried out to detach the Bi_2O_2Se nanosheet from mica substrate and assemble on the targeted SiO_2/Si substrate. In each step, the sample was sequentially cleaned with acetone, isopropyl alcohol (IPA), and deionized (DI) water. After the transferring process, the Bi_2O_2Se sample was defined the metal contacts (50 nm Pd) and top dielectric and electrode (7 nm naturally formed AlO_x and 50 nm Al), utilizing LED lithography. The deposition was via thermal evaporator and the deposition rate was confined within 1 Å at 10^{-6} Torr to ensure the film uniformity and quality..Electrical properties were all measured in Agilent B1500 Semiconductor Device Parameter Analyzer.

Author contribution

Bo Liu and Chao-Sung Lai generated the idea and designed the work. Dharmendra Verma prepared the sample. Bo Liu, Hanyuan Liang, Hui Zhu measured the device. Bo Liu, Lain-Jong Li, Tuo-Hung Hou, Chao-Sung Lai analysis the experiment results. Yudi Zhao carried out the Monte Carlo simulation. Bo Liu and Le An Wang prepared the manuscript, and Chao-Sung Lai revised it.

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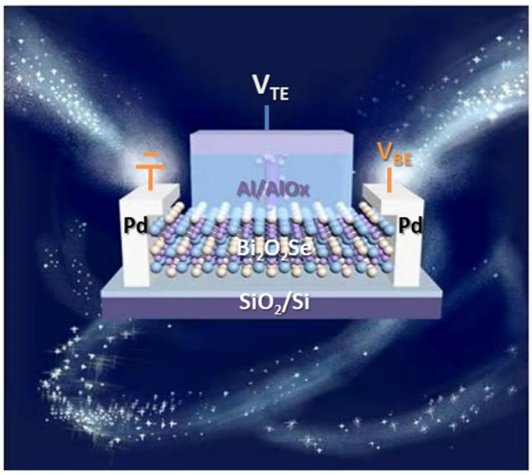

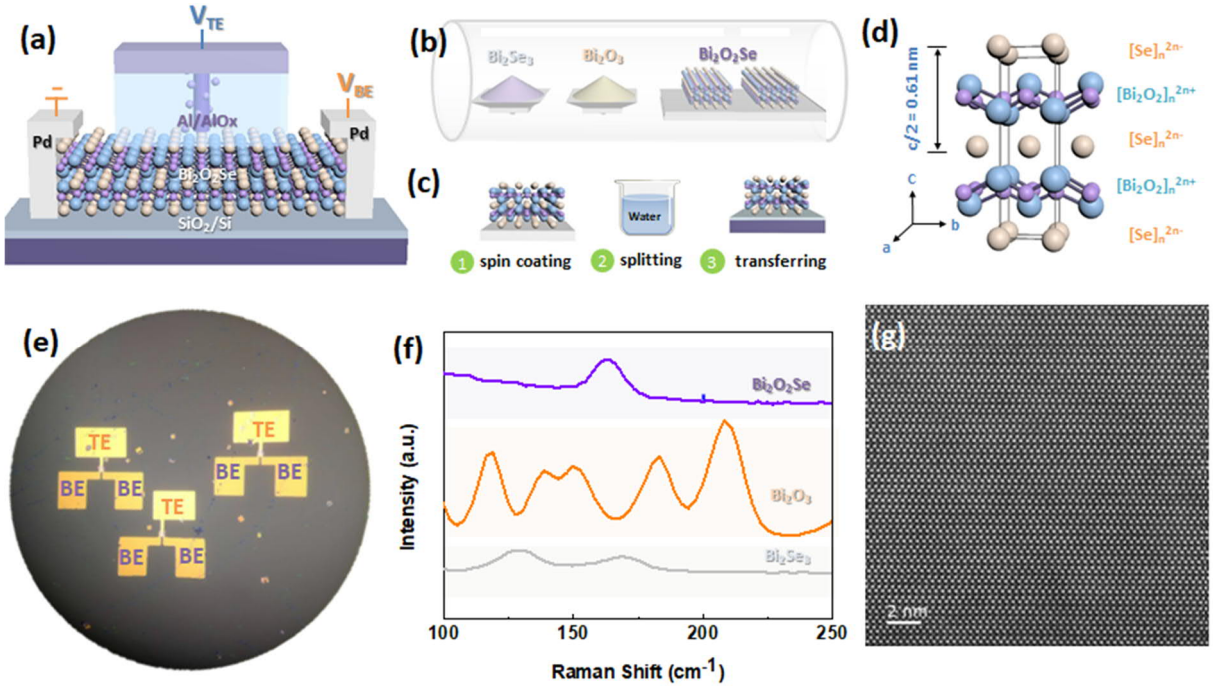

Figure 1 Illustration of the device architecture of Bi_2O_2Se based memristor, fabrication process and material analysis. (a) the device structure of Bi_2O_2Se based memristor, (b) low pressure chemical vapour deposition of Bi_2O_2Se in a furnace, (c) transfer process of Bi_2O_2Se from mica substrate to SiO_2/Si substrate, (d) the lattice structure of Bi_2O_2Se, (e) Optical Image of Bi_2O_2Se based memristor device, (f) Raman spectrum of Bi_2O_2Se as well its precursor Bi_2O_3, Bi_2Se_3, (g) HR-TEM image of the Bi_2O_2Se in cross section view, where the scale bar is 2 nm.

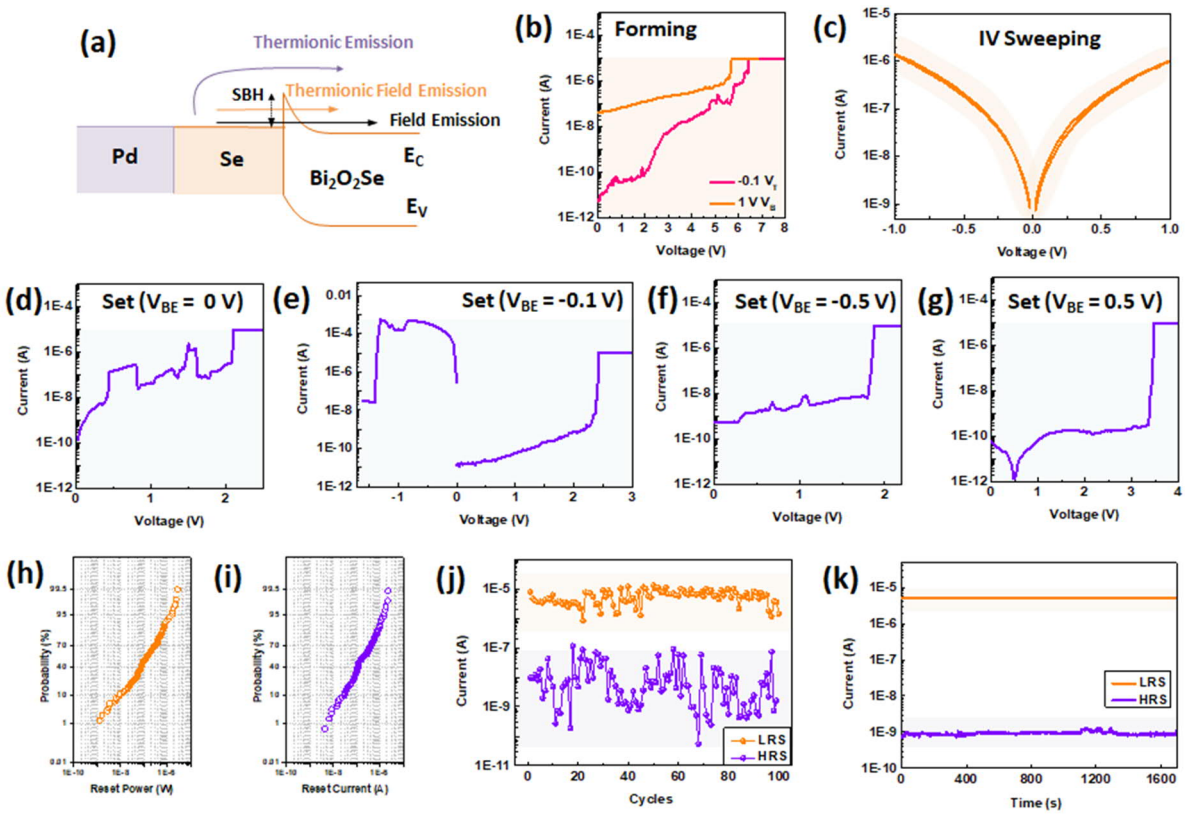

Figure 2 Basic electrical measurements of Bi_2O_2Se based Memristor. (a) Illustration of the band diagram of the interface between Pd contact and Bi_2O_2Se, as well as the current injection mechanisms, (b) forming process of the Bi_2O_2Se based memristor under different V_{BE} bias, (c) IV sweeping curve between the two contact Pd pads, (d, f-g) set process under V_{BE}= 0, -0.5 0.5V, (e) set and reset process under V_{BE} = -0.1 V, (h-i) reset power and reset current distribution, and reliability test of (j) endurance and (k) retention, where the reading voltage is 0.1 V.

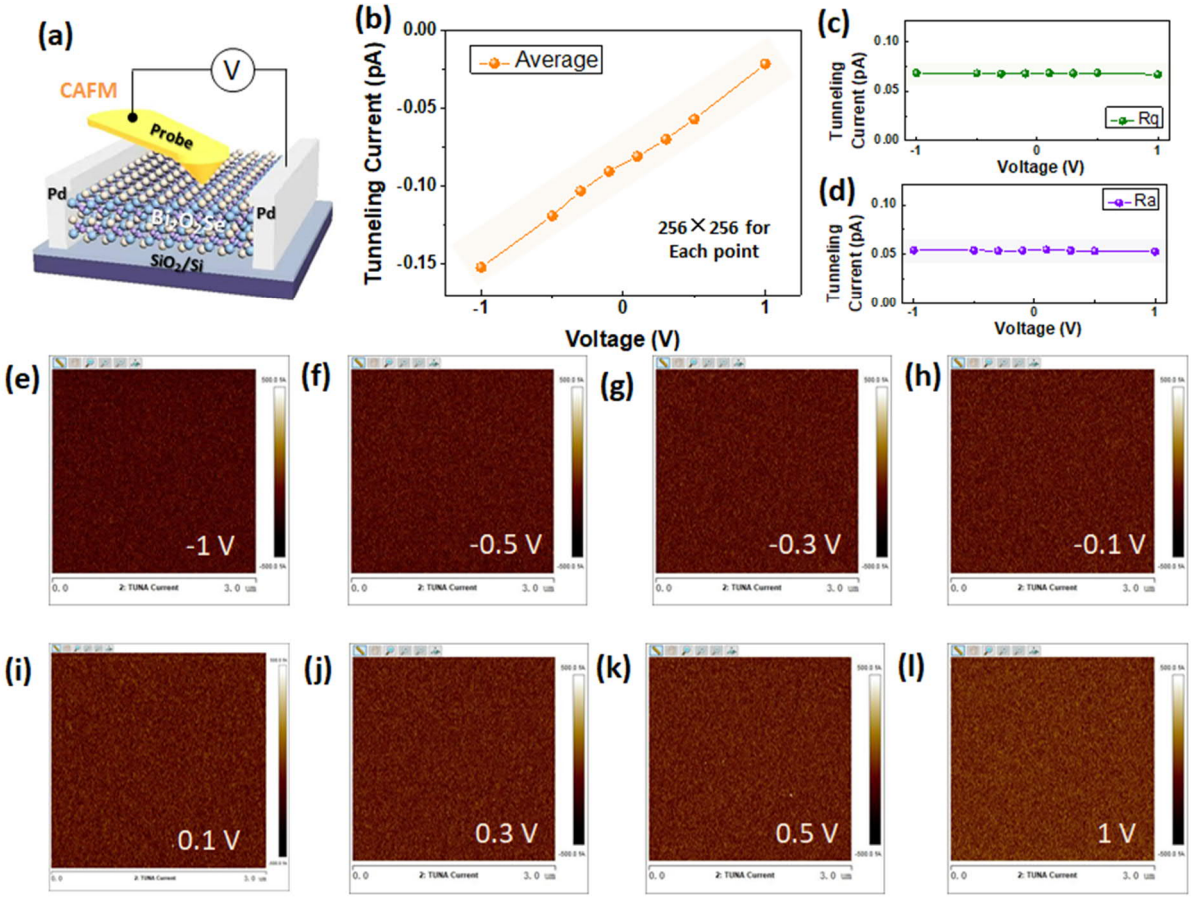

Figure 3 CAFM measurements of Bi_2O_2Se surface. (a) Illustration of the CAFM probe station, (b-d) Average, Rq and Ra values of the tunnelling currents, (e-l) the current mapping of CAFM in 3 × 3 μm^2 with 512 by 512 points, under the sweeping bias ranging from -1 (e), -0.5 (f), -0.3 (g), -0.1 (h), 0.1 (i), 0.3 (j), 0.5 (k), 1 V (l).

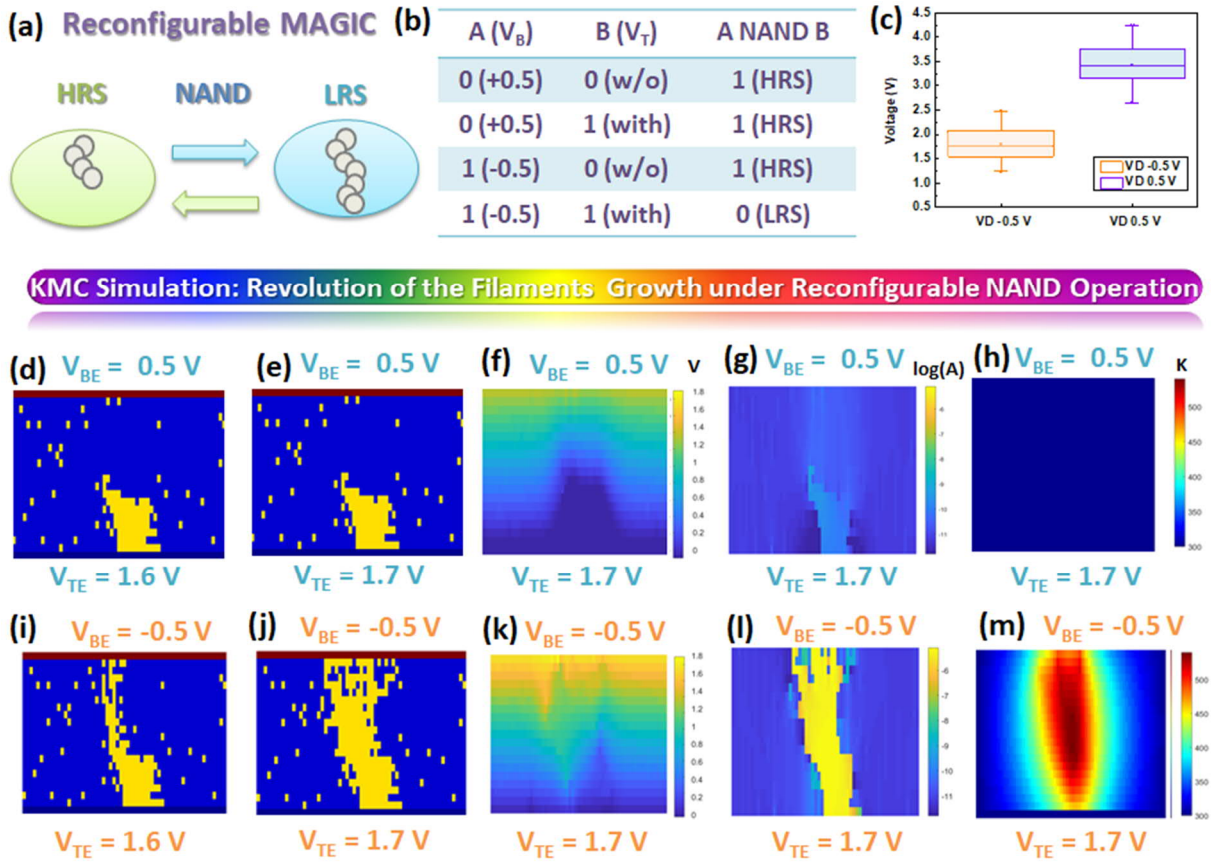

Figure 4 the demonstration of Bi_2O_2Se based MAGIC and kinetic Monte Carlo simulation. (a-b) the illustration figure and truth table of the MAGIC operations, (c) reconfigurable logical operations: each error bar contains 20 cycles; Monte Carlo simulation including filament revolution (d-e, i-j), distribution of electric field (f, k), current (g, l) and temperature (h, m) with different V_{BE} bias.

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