A simple and inexpensive circuit for emission and capture deep level transient spectroscopy

C. V. Reddy, S. Fung, and C. D. Beling
Department of Physics, The University of Hong Kong, Hong Kong

A simple and inexpensive circuit for deep level transient spectroscopy is described, which allows rapid characterization of emission as well as capture activation energies of deep levels. This flexibility of making capture activation studies affords more information on defect morphology than the more standard emission activation studies. This is demonstrated by making a representative capture activation energy measurement on the EL6 level in undoped *n*-type GaAs of 0.484 ± 0.005 eV. Also the spectrometer has shown better performance than earlier reported systems by its ability to resolve the side peaks of the EL6 level, for which emission activation energies of 0.29 and 0.4 eV are assigned. Constructed around a commercially available capacitance meter and pulse generator, the control circuitry is designed and developed using inexpensive and off-the-shelf integrated circuits. © *1996 American Institute of Physics.* [S0034-6748(96)03601-7]

I. INTRODUCTION

Deep level transient spectroscopy (DLTS), introduced by Lang,[1] characterizes deep level traps present in semiconductors by determining their position, concentration, and capture cross-section. It has long been realized, however, that important additional defect coordinate configuration information can be obtained if an accurate measure of the capture activation energy can be made.[2] Such information, while being useful in identifying the structure of deep level defects, is hard to obtain, requiring by conventional methodology the determination of capture cross-section at different temperatures using fast filling pulse circuitry. Recently, however, Ghosh and Kumar[3] and Lu *et al.*[4] have shown that such tedious work is unnecessary, and the systematic errors associated with it avoidable, by making simple observations of the capacitance transient during trap filling. DLTS instrumentation that allows capacitance transients to be analyzed both on carrier capture and emission is thus highly desirable.

The basic principle of the DLTS technique is that of observing as a function of temperature capacitance transients which result from the emission (capture) of charge carriers from (into) the deep level traps. This is normally accomplished by passing the transient signal through some form of rate-window circuitry. The boxcar averager, which has been widely used for this purpose, requires critical settings for the width of the gate pulse, the integrator response time, and the rate-window time constants, if it is to be used correctly.[5] An improper selection of these parameters results in the DLTS peak shifting toward either the low or high temperature side of its correct position. Moreover, such instrumentation is expensive. Similarly, when a lock-in amplifier is used to set the rate-window, the initial gate-off period and phase setting are two important operating conditions requiring critical adjustment and even when set correctly the system is far from optimised for DLTS.[6,7] A few DLTS systems have been described in the literature which employ laboratory built circuits instead of boxcars or lock-in amplifiers to process the capacitance transients.[8,9] However, these systems suffer from the disadvantage that there is considerable signal loss due to the complexity associated with the signal averaging circuits. Several other systems have been suggested which require logging the transient data with computers. It is observed that the DLTS spectra appeared to be more noisy when a computer fitted with a data acquisition system is used to analyze the capacitance transients. This is due to the fact that the noise level in the signal is increased almost by a factor of 10, as observed on an oscillograph, leading to the degradation of the sensitivity of the system with a poor signal-to-noise ratio. Finally, fast measuring digital volt meters (DVM) are also commercially available for the transient signal analysis. However, these meters are not so convenient to use in DLTS, since they require control signals for each data sampling, averaging and transferring. A computer or some kind of control circuit is required to completely utilize their functions. Moreover, these are often disproportionately expensive for the simple task of storing and sorting the transient data.[10,11]

Keeping in mind the advantages and disadvantages associated with the above-mentioned DLTS systems, a simple and less expensive DLTS system has been developed which allows the straightforward determination of emission and capture activation energies. Apart from a commercially available capacitance meter and pulse generator the remainder of the system comprises of some simple circuitry constructed using inexpensive and off-the-shelf integrated circuits (ICs). Although the system is low cost, we show that it has a sensitivity and resolution comparable to, if not better than, present commercially available instruments.

II. THE EXPERIMENTAL SETUP

The DLTS spectrometer consists of a simple homemade cryostat, a capacitance meter (Boonton 72B), a pulse generator (HP 8112A), an *X-Y* recorder, and the laboratory built signal processor (SP) which is detailed in the next section. The block diagram of the spectrometer is shown in Fig. 1. The SP unit sets the rate-window, does the signal averaging, and provides the necessary time synchronization to the rest of the equipment in the DLTS system thus resulting in an automatic measurement with minimal human intervention.
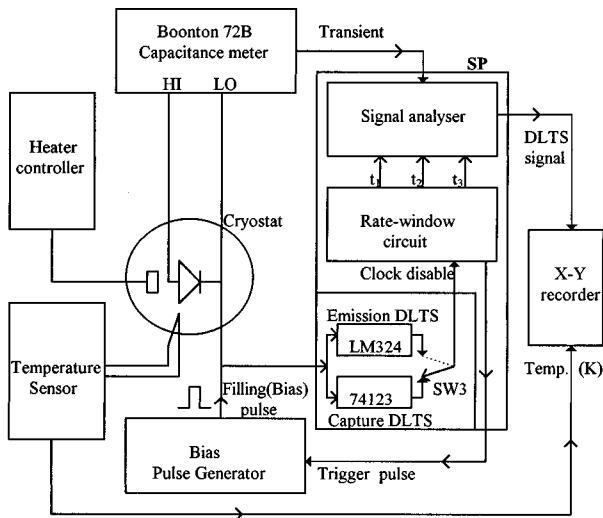
FIG. 1. Block diagram of the DLTS system.

On receiving a trigger pulse from the SP unit, the pulse generator (PG) provides the filling pulse to the sample with a preset pulse width and height. The SP unit takes the analog output of the capacitance meter as its input and outputs the DLTS signal to the X-Y recorder. The sample is kept inside a homemade cryostat, which is made of an aluminum block with relatively large thermal mass to minimize fluctuations in the sample temperature. A Rh–Fe resistor is used as the temperature sensor, which can measure the temperature to an accuracy of ± 0.1 K.

III. CIRCUIT DETAILS

The SP unit consists of the following subunits: (A) a rate-window circuit, (B) a signal analyzer, and (C) a clock synchronizing circuit, which are described as follows.

A. The rate-window circuit

The rate-window circuit provides the basic timebase for the entire DLTS system, sets the rate-window timings, and controls the sequence of events that take place in a typical DLTS experiment, as shown in the Fig. 2. The timebase is derived from a stable and accurate 1 MHz crystal oscillator, whose output is fed to a divider chain constructed using decade and binary counters which in turn produce pulse trains with different clock periods ranging from 1 ms to several seconds. The oscillator output first undergoes a pre-set division of 100 using two decade counters 74LS90, and then a variable division using three decade counters and one binary counter 74LS93. The outputs of the three decade counters of the variable division are connected to a switch SW1 and this switch selected value again undergoes a simultaneous division by a factor of 2, 4, 8, 16 at four different outputs of the binary counter, which are again connected to another switch SW2, as shown in Fig. 2. The SW2 switch selected value finally determines the basic timebase of the DLTS system. Thus the timebase can easily be calculated now by reading the respective values selected by the two switches SW1 and SW2, which are designated by T_1 and T_2, and is given by $T_B = T_1 \times T_2$. The minimum timebase that can be selected is 2 ms.

Controlling the sequence of events is done with the help of a binary counter 74LS93 and a decoder/demultiplexer 74LS154. At the set timebase frequency the 16 outputs of the decoder go sequentially active-low, starting from 0 to 15 and then returning to 0 for the start of another sequence. Any of these outputs, which are designated as $0T_B$, $1T_B$, $2T_B$, and so on for the corresponding outputs of O_0 to O_{15}, may now inturn be connected to the respective instruments in the DLTS apparatus as per the measuring sequence. The measuring sequence begins by $0T_B$ triggering the pulse generator to apply a bias pulse to the sample. This is followed by gener-
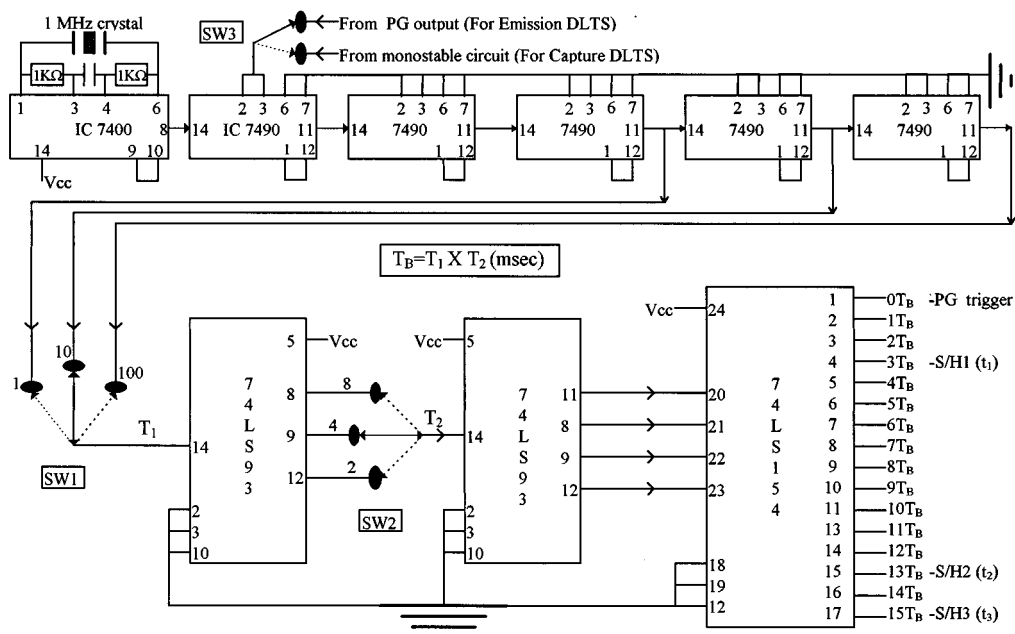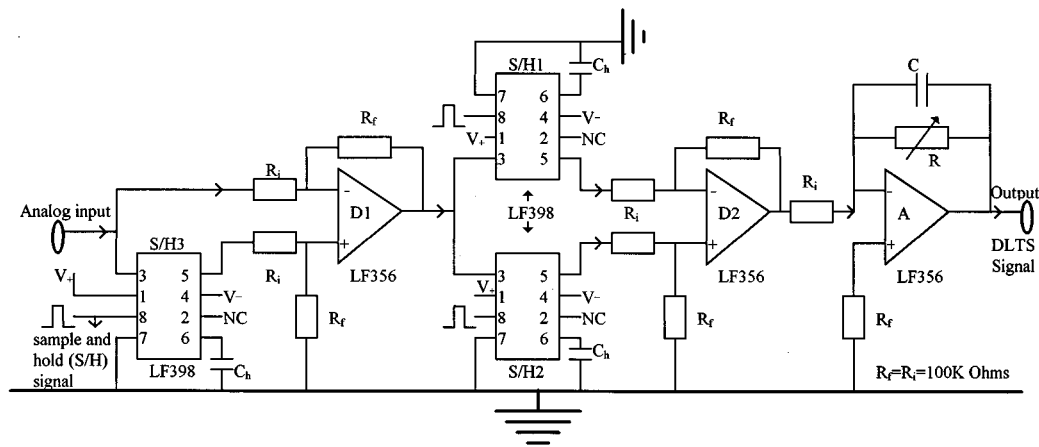

FIG. 2. Rate-window circuit diagram.

FIG. 3. Circuit diagram of the signal analyzer.

ating sampling pulses for the S/H1 and S/H2 amplifiers at the rate-window times t_1 and t_2 and ends with a third sampling pulse at t_3 for the S/H3 amplifier which is required for carrying out baseline correction for the DLTS signal. The relative positions of the sampling gates t_1, t_2, and t_3 are fixed at $3T_B$, $13T_B$, and $15T_B$ respectively. The rate-window, as derived from capacitance samplings at t_1 and t_2, is proportional to the switch selectable timebase T_B (2, 4, 20, 40, 200, 400 ms) and is given by

$$t_w = \frac{t_2 - t_1}{\ln(t_2/t_1)} \cong 6.82 T_B .$$

Since the trap filling pulse is applied at $0T_B$, t_1 could also be taken at $1T_B$ or $2T_B$ instead of at $3T_B$. There are two reasons for this. The first being that it is always advisable to keep the first sampling gate away from the end of the filling (bias) pulse in order to avoid systematic errors due to the slow response time and the initial recovery transient due to the bias pulse overloading effect of the capacitance meter. The second reason is that by fixing the ratio, r, of t_2 over t_1 ($r = t_2/t_1 = 4.33$) at around four, the sensitivity and resolution of the system are optimized for better performance. It is important to note here that the sensitivity of the system can be further improved by increasing the ratio, r. However, the gain in sensitivity is at the expense of the resolution of the system. The resolution in a DLTS system, as in any other spectroscopic technique, is equally important to separate the signatures due to different deep levels. The sensitivity of the present DLTS system is, however, determined in terms of the ratio $\Delta C/C$ as 1×10^{-4}, which corresponds to a detection limit for the trap concentration N_t of $10^{-5} N_D$ (or N_A) when the capacitance meter is selected in 10 or 30 pF range. It should be noted that the sensitivity will be reduced by a factor of 10 when the capacitance meter is operated in either 100 or 300 pF range. However, it is unlikely that a junction can be prepared outside this range.

B. The signal analyzer

The circuit diagram of the signal analyzer is shown in Fig. 3. Its effective function is to extract the information which is hidden in a series of capacitance transients. It is constructed using three sample-and-hold (S/H) amplifiers (LF 398) and two differential amplifiers (LF 356). The S/H amplifier samples the input signal when its logic input is in the HI state and holds the sampled value across the hold capacitor (C_h) when its logic goes LO. A polypropylene capacitor with a value of 0.1 μF/100 V is used as a hold capacitor in this circuit. In developing this circuit it was found that the fast rise time logic signal at pin 8 of the S/H amplifier could induce noise in the hold signal (analog input). To minimize this problem, the logic signal was kept as far as possible from the analog input while developing the PCB for this circuit and grounded guarding traces were used around the input.

The capacitance transient is first sampled near its end point (t_3) by the S/H3 amplifier in order to eliminate the dc baseline shift. The dc shift comes mainly from the temperature-dependent capacitance of the sample and since it can become quite high (typically a few volts) it is best eliminated so that systematic errors in signal amplification are minimized. This is accomplished by taking the sampled value S/H3 and subtracting it from the next transient using the differential amplifier D1.

The baseline restored capacitance transient is now sampled at t_1 and t_2 using S/H1 and S/H2 and the held voltages fed to the inverting and noninverting inputs of the second differential amplifier D2. The output of this amplifier gives the DLTS signal, which is further amplified using an LF356. The gain of this final stage is switch selectable from the front panel of the RSC unit.

C. The clock synchronizing circuit

The clock synchronizing circuit provides the necessary time synchronization between the pulse generator (PG), which provides the filling pulse to the sample, and the SP unit, which sets the rate-window timings. In other words, this circuit facilitates the exact determination of the emission or capture time constants of any given deep level. In an emission DLTS measurement, the rate-window timings t_1 and t_2 have to be measured exactly from the end (falling edge) of the filling pulse in order to correctly analyze the emission transient. The necessary time synchronization between the
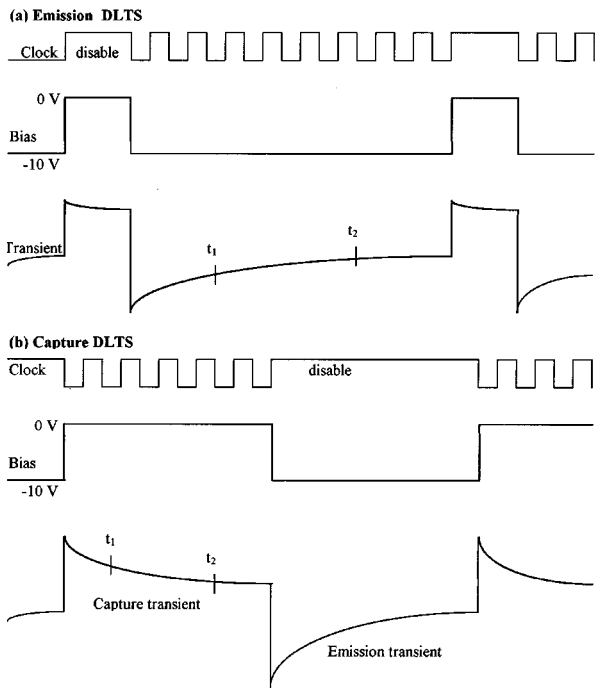
FIG. 4. Timing diagram for a typical emission or capture DLTS measurement.

FIG. 5. (a) Emission DLTS spectra taken on an undoped n-GaAs sample with six rate-window time constants: 13.64 ms, 27.28 ms, 136.4 ms, 272.8 ms, 1.364 s, and 2.728 s corresponding to peaks from right to left, respectively. (b) Capture DLTS spectra recorded with 13.64, 27.28, and 54.56 ms rate-window time constants.

falling edge of the filling pulse and the timings, t_1 and t_2, can only be accomplished if the clock is disabled during the filling pulse, and then restarted immediately afterward. Since the output of the pulse generator is not TTL compatible it cannot be directly used to disable the clock. A comparator circuit, constructed using LM324, thus converts the filling pulse to a corresponding TTL pulse of the same width, which is then fed to the clock circuit in order to disable it. This is achieved in practice by connecting to pins 2 and 3 of the first two 74LS90 ICs of the fixed-division section, as shown in Fig. 2.

In the capture DLTS measurements, t_1 and t_2 have to be measured from the beginning (rising edge) of the trap filling pulse in order to observe the capture transient. The emission pulse, which is kept long enough to empty the traps, is generated immediately after the filling pulse. The width of the emission pulse is decided by the RC time constant of a monostable multivibrator circuit 74LS123. Since in a capture transient measurement sampling times t_1 and t_2 are relative to the end of the emission pulse, the synchronization is achieved by simply switching over SW3 so as to disable the clock during the emission pulse rather than the trap filling pulse. The synchronization achieved in both emission and capture DLTS can easily be understood through the timing diagram as shown in Fig. 4.

The ± 12 V supplies for the signal analyzer (analog) circuits and the $+5$ V supply for the rate-window and clock synchronizing circuits were designed with a residual ripple of 7 mV. The two power supplies are isolated from each other and developed on two different printed circuit boards so as to prevent the fast switching of the digital circuits producing large transient load currents causing spurious effects in the signal analyzer. The analog circuits were, in addition,
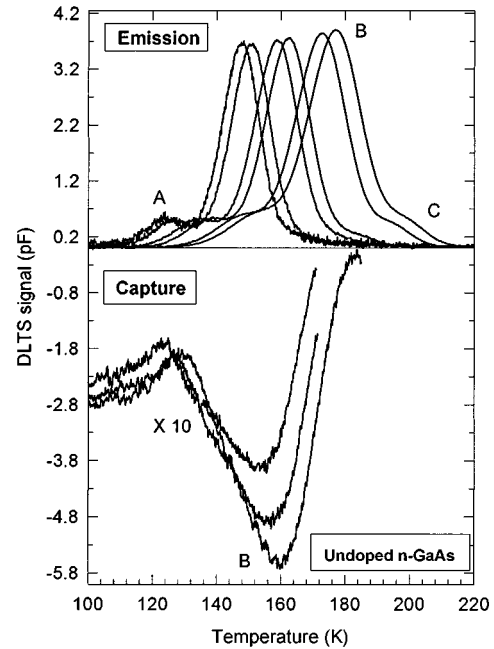
isolated from the digital circuits with the help of a thick grounded aluminum sheet. The ground points of all the individual circuits and the power supplies were star grounded in order to eliminate ground loops between the various circuits. With all these precautions, the noise level in the DLTS signal was minimized to as low as 7 mV (peak-to-peak). This is certainly an improvement of our system compared to those built around computers where the noise level is at least 10 times higher.

IV. RESULTS

The emission and capture DLTS spectra obtained on undoped n-GaAs Schottky barrier diode are shown in Fig. 5, and the corresponding Arrhenius plots are shown in Fig. 6. All the emission DLTS spectra are recorded with a 10 ms saturating filling pulse, while the capture DLTS spectra is recorded with a 120 ms emission pulse. A longer emission pulse in the capture DLTS measurement is very much needed to observe a decent capacitance transient due to the capture process. It is observed in the present investigation that the emission transients are about ten times larger in magnitude than those corresponding capture transients for any given deep level. The reason for this is that the capture time constants are much smaller than the emission time constants. However, due to the limitation associated with the capacitance meter, whose response time is of the order of 1 ms, the shortest timebase that can be selected with our system is 2 ms. Therefore, only for the peak B, the capture activation energy is determined as 0.484 ± 0.005 eV. However, due to the noisy spectra of the deep levels A and C, there was some difficulty in deciding the peak maximum position at higher rate-window time constants and hence they are not included
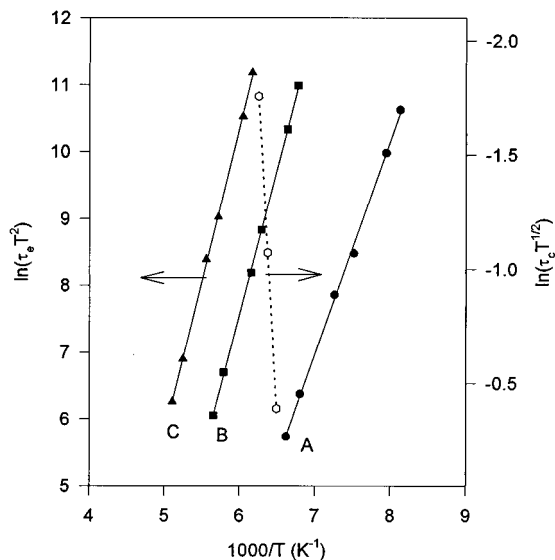
FIG. 6. Arrhenius plot for deep levels *A*, *B*, and *C*; (—) for the emission activation energies, (···) for the capture activation energy.

in the present work. The emission activation energies for the deep levels *A*, *B*, and *C* are determined as 0.276±0.006, 0.375±0.003, 0.4±0.004 eV, respectively. These are identified as EL8, EL6, EL5 according to the classification of Martin *et al.*[12] The spectra clearly demonstrate that our DLTS system is well optimized for better sensitivity and resolution, which make it possible for resolving the peaks *A* and *C* from peak *B*, as shown in Fig. 5, at slightly higher rate-window time constants.[13,14] This is definitely the merit of our system over the others, which are constructed using computers, lock-in amplifiers, and so on.

ACKNOWLEDGMENT

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