

SEMINAR ON

CIRCUITS AND SYSTEMS

Tuesday, July 31, 1979.



ELECTRICAL ENGINEERING DEPARTMENT,
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Dr. R. L. Huang
The Vice-Chancellor

Vice-Chancellor's Welcoming Speech for
Seminar on Circuits and Systems on
Tuesday, 31st July 1979.

It gives me great pleasure to welcome you all, this morning, to the opening of our Seminar on Circuits and Systems. Some of you are newcomers to the University of Hong Kong or even to Hong Kong itself. To them I would extend my good wishes for a very interesting and pleasant visit. But to all of you may I wish you a rewarding day with us here.

Today's Seminar focuses on an area of considerable interest to the modern Electrical Engineer, not least because the subject itself has reached a turning point. After a decade of abstraction, the field of circuits and systems, I understand, is being re-appraised and directed towards a more practical path. This Seminar, therefore, is both timely and pertinent. Amongst us this morning, we are particularly fortunate in having distinguished scholars of international repute, renowned for their pioneering work in the field and the publications arising therefrom. Their contributions to the Seminar will be extremely valuable and will provide us with food for thought for sometime to come. Their presence here will give us the benefit of personal contact and exchange of views - and this is a rare opportunity of which we will take full advantage.

Hong Kong is often considered by some as suffering from academic isolation. This criticism may have been more justified in the past, but now, with sophisticated communication and transportation networks, we are much better able to keep abreast of new trends and developments elsewhere. However, there can be no real substitute for direct discussion and debate, for "the meeting of minds". This Seminar,

therefore, will serve in bringing practising engineers and academicians in Hong Kong closer to experts from overseas, and thus closer to the pulse of ideas. Some of our distinguished visitors have just returned from international conferences, on the same subject, in Tokyo and Taipei. With them they bring a wealth of new information for us to learn and ponder over. May I say how much we appreciate their presence here.

A warm welcome, too, to our colleagues from the Hong Kong industries. We are very glad indeed to have you with us. Your experience and expertise and your support for our work at the University, have long been valued by us, and we hope that this Seminar will strengthen the ties between us and that you will find time to visit us often.

The University is now embarking on new building projects for the Engineering Faculty. Do not judge us too harshly when we show you our present facilities, for in a few years we hope to proudly welcome you to our new Engineering building and to the rapid developments which by then will have taken place.

May I wish you all a very stimulating and enjoyable Seminar.

A ONE-DAY SEMINAR ON CIRCUITS AND SYSTEMS

July 31, 1979

University of Hong Kong

Morning Session

1. *"Topological Analysis of Networks
Some Recent Developments"*
Dr. Shu-Park Chan
Professor and Chairman
Dept. of Elec. Engr. & Comp. Sci.
University of Santa Clara
Santa Clara, California 95053
2. *"Graphs and Feedback Amplifier Theory"*
Dr. Wai-Kai Chen
Distinguished Professor
Dept. of Electrical Engineering
Ohio University
Athens, Ohio 45701
3. *"Some Concepts for Hierarchical Layout
of VLSI Circuits"*
Dr. D. A. Mlynski
Professor
Dept. of Electrical Engineering
University of Karlsruhe
Karlsruhe, Germany
4. *"Fuzzy Potentials in Network Problems"*
Dr. K. Onaga
Professor
Department of Circuits & Electrical
Systems Engineering
Hiroshima University
Hiroshima City, Japan
5. *"Relevance of Network Theory to Models
of Distributed/Parallel Processing"*
Dr. T. Murata
Professor
Dept. of Information Engineering
University of Illinois at Chicago Circle
Chicago, Illinois 60680

Afternoon Session

6. *"Accessibility of Large-Scale Elec-
tronic Circuits"*
Dr. R. W. Liu
Professor
Dept. of Electrical Engineering
University of Notre Dame
Notre Dame, Indiana 46556
7. *"Block Implementation of Recursive
Digital Filters"*
Dr. S. K. Mitra
Professor
Dept. of Electrical Engineering
University of California
Santa Barbara, California 93106
8. *"A Characterization of the Invariance
of Positivity for Functional Dif-
ferential Equations"*
Dr. I. W. Sandberg
Bell Laboratories
600 Mountain Avenue
Murray Hill, New Jersey 07974
9. *"Linear Power Amplifiers in Microwave
Radios"*
Dr. C. C. Hsieh
Manager
Microwave Integrated Circuits Dept.
Farion Electric Co.
San Carlos, California 94070
10. *"Complete Stability of Non-reciprocal
Nonlinear Networks"*
Dr. Leon O. Chua
Chaire de theorie des circuits et
systems
Ecole Polytechnique Federale de
Lausanne
16 Chemin de Bellerive
CH-1007 Lausanne
Switzerland

SHU-PARK CHAN

TECHNICAL BIOGRAPHY



Shu-Park Chan was born in Canton, China, on October 10, 1929. He received his B.S. degree in electrical engineering from the Virginia Military Institute (V.M.I.) in 1955, the M.S. and Ph.D. degrees, both in electrical engineering, from the University of Illinois (U. of I.), Urbana-Champaign, in 1957 and 1963, respectively.

From 1957 to 1963, he taught at V.M.I. first as Instructor in Electrical Engineering and Mathematics and then as Assistant Professor of Mathematics.

On leave of absence from V.M.I., he was awarded a University Fellowship by U. of I. from 1959 to 1960 while studying toward the Ph.D. degree in electrical engineering at the University. He taught as Instructor in Electrical Engineering in that Department from 1960-61, and worked in the Coordinated Science Laboratories as Research Associate from 1961 to 1963 at the University.

Since February 1963, he joined the faculty in the Electrical Engineering and Computer Science Department at the University of Santa Clara, where he is presently Professor and Chairman. His major interests and publications have been in network and system theory, topological analysis and synthesis, computer-aided circuit design, and applied mathematics. He is author of *Introductory Topological Analysis of Electrical Networks* (Holt, Rinehart and Winston, 1969), co-author of *Analysis of Linear Networks and Systems: A Matrix-Oriented Approach with Computer Applications* (Addison-Wesley 1972) and *Introduction to the Applications of the Operational Amplifier* (Academic Cultural Co., 1974), and editor and major contributor of *Network Topology and Its Engineering Applications* (National Taiwan University Press, 1975).

Dr. Chan is a member of Tau Beta Pi, Eta Kappa Nu, Pi Mu Epsilon, Phi Kappa Phi, and Sigma Xi honorary societies and a member of American Association of the Advancement of Science, and of the American Society of Engineering Education. He is a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE) and a past chairman of the Circuit Theory Group of the San Francisco Section IEEE. He is listed in *American Men and Women of Science*, *Who's Who in America*, *International Scholars Directory*, *Dictionary of International Biography* and *Who's Who in the World*.

Professor Chan is also president of the Chinese Arts and Culture Institute, and has been actively involved in promoting and organizing activities and projects relative to Chinese arts and culture in the Bay Area.

TOPOLOGICAL APPLICATIONS TO IC LAYOUT PROBLEMS

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ABSTRACT

A topological approach based on oriented line segments is used to implement a set of logical and topological operations for IC layout manipulations which are useful in IC layout design rule check, IC layout resizing, and IC consistency check between the layout and the circuit/logical schematic.

INTRODUCTION

Conventional integrated circuit (IC) design consists of preparing an initial circuit schematic and performing a circuit analysis using the computer simulation method. Once the designer is satisfied with the simulated performance, the circuit is transformed to an IC layout which is then digitized to obtain its computerized layout data base. The layout data base will be used to generate IC mask for fabrication. During the IC layout design, the size of transistors, resistors and capacitors are scaled and converted into area definition based on nominal circuit parameter values used for the circuit simulation. The sizes of the circuit components are adjusted to fit the IC layout design rules based on minimum spacing or width, relative element positions, and size requirements.

The design of an IC mask is time consuming and expensive because of the extensive checkings of the IC circuit and layout. Moreover, the amount of work to perform checkings will grow rapidly because the complexity of IC increases very rapidly as shown in figure 1. Thus, computer aids have been used extensively in the design and checking of IC masks to reduce the tedium involved in the consistency check between the layout and the circuit /logic schematic and the design rule check. Many computer-aided IC layout processing programs have been developed or developing in various type of companys such as semiconductor manufacturing companys, computer manufacturing companys, graphic application companys and data processing / service companys. Most of the programs are to implement a set of elementary operations from which a complete IC check can be generated. The elementary operations are listed as follows:

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1. Design Rule Check [1-6]

- (i) Spacing Check - Internal Spacing Check, External Spacing Check, Enclosure Spacing Check, and Relational Spacing Check etc.
- (ii) Logical Operations - OR, AND, ANDNOT, and XOR etc. (see figure 2.)
- (iii) Minimum Area Check
- (iv) Layout Resizing - Expansion and Contraction.

2. IC Consistency Check between the Layout and the Circuit / Logic Schematic [9-12]

- (i) Logical Operations - OR, AND, ANDNOT, and XOR etc.
- (ii) Topological Operations: (see figure 3.)
 - (a) Identify regions - each region may consist of a set of joint polygons.
 - (b) Recognize two regions in two different layers are connected through contact(s), and
 - (c) Recognize a region in one layer is surrounded (CONTAINED) by a region in the other layer, etc.
- (iii) Device Recognition - recognize devices such as transistors, resistors and capacitors etc.
- (iv) Layout Resizing - Expansion and Contraction.
- (v) Circuit Parameter Calculation - resistances, capacitances and w/l's of transistors etc.

According to the basic data item that the elementary operations operate on, there are several possible approaches shown below to implement these elementary operations.

- (1) Polygon approach - the polygons in the IC data base are directly used for data manipulations [1].
- (2) Trapezoid (or Rectangle) approach - the polygons are splitted into trapezoids (or rectangles) for data manipulations [6].
- (3) Vertex approach - the vertices of polygons are used for data manipulations [3].
- (4) Line segment approach - the polygons are splitted into line segments for data manipulations [5, 9].
- (5) Bit map approach - the polygons are transformed into a bit map such that each bit corresponds

to a unit of area and the areas enclosed by the polygons are represented by '1' and that not enclosed by '0' [2].

- (6) Symbolic approach - the IC layout data base composed of a set of symbols such that each symbol represents a component or part of component. The data manipulations can be on the symbols [7-8].

In this paper, we are to present a topological approach based on oriented line segments to implement the algorithms for the logical operations and the topological operations.

II. DEFINITION

We shall first introduce the definition of oriented line segment (OLS).

For each of line segments (v_i, v_{i+1}) , between vertices $v_i = (x_i, y_i)$ and $v_{i+1} = (x_{i+1}, y_{i+1})$, of an $(n-1)$ -vertex clockwise polygon where $i = 1, 2, \dots, n-1$, the OLS is defined as follows:

$$\text{OLS} \hat{=} \begin{cases} (v_i, v_{i+1}) \text{ with orientation 'up' if } y_i < y_{i+1} \\ (v_{i+1}, v_i) \text{ with orientation 'down' if } y_i > y_{i+1} \\ (v_{i+1}, v_i) \text{ with orientation 'horizontal-left' if } y_i = y_{i+1} \text{ and } x_i > x_{i+1} \\ (v_i, v_{i+1}) \text{ with orientation 'horizontal-right' if } y_i = y_{i+1} \text{ and } x_i < x_{i+1} \end{cases}$$

In the (v_i, v_k) of an OLS, vertex v_i is called the first vertex and v_k the second vertex of the OLS.

Hereafter, we will use \uparrow -OLS, \downarrow -OLS, \leftarrow -OLS, and \rightarrow -OLS to denote the OLS's with orientations 'up', 'down', 'horizontal-left', and 'horizontal-right' respectively. Moreover, for \uparrow -OLS and \downarrow -OLS, the y ordinate of the first vertex is always smaller than that of the second vertex. Thus, for convenience we will use (x_l, y_l) and (x_u, y_u) to denote the (x, y) coordinates of the first and the second vertex respectively.

III. ALGORITHM OVERVIEW

The logical operations (OR, AND, ANDNOT, and XOR) operate on two layers (input layers) to generate another layer (output layer) and the topological operations operate on one, two or three layers to identify or recognize some topological properties. The algorithms for the logical operations and the topological operations are outlined in the following:

Step 1. For each of the input layers, create an OLS file which contains all the \uparrow -OLS and \downarrow -OLS of the polygons of the layer. Then sort the OLS file according to the ascending order of y_l , if the y's are equal, sort according to their ascending order of x_l .

Step 2. Create a horizontal line $y = h$ where h will start from the minimum y_l , go through all y_l 's, y_u 's and the y ordinates of the intersection points of OLS's, to the maximum y_u of the sorted OLS file. For each h , the set S , which contains all the OLS's intersecting with the line $y = h$ and whose $y > h$, is sorted according to the following rule:

Sorting Rule at $y = h$

- (1) Sort the OLS's in S according to the ascending order of their x ordinates at $y = h$; or
- (2) If their x ordinates at $y = h$ are equal, sort the OLS's according to the ascending order of the (smallest) angle θ measured in the clockwise direction from line $y = h$ to the OLS's; or
- (3) If their x ordinates at $y = h$ and θ are both equal, then sort the OLS's according to the orientation; i.e., \uparrow -OLS's are ordered before \downarrow -OLS's.

Then, the logical operations perform the following two operations on the sorted S to generate the output layer.

- (1) Grouping operation - this operation find the OLS pairs of the output layer between $y = h$ and $y = h'$ where $h' \hat{=} \text{minimum} \{y \mid y \text{ is the ordinate of an intersection point or } y_u \text{ of } S, \text{ or the } y \text{ of an OLS in the sorted OLS file whose } y_l > h\}$
- (2) Linking operation - this operation link the OLS pairs to form the polygons of the output layer.

The topological operations operate on the sorted S to find the topological properties listed in the Introduction.

In the following, we will discuss the Grouping operation, the Linking operation and the operations to identify the topological properties in detail.

IV. LOGICAL OPERATIONS

We will use the two variables I and J for counting and N identifying the OLS's pairs.

1. OR operation

- (i) Set $I = 0$ and $N = 0$, Then, start to scan the sorted S .
- (ii) Fetch one OLS from the sorted S and perform $I \leftarrow I+1$ if it is a \uparrow -OLS or $I \leftarrow I-1$ if it is a \downarrow -OLS. Then,

Case 1. If it is a \uparrow -OLS and $I = 1$, perform $N \leftarrow N + 1$ and assign it as the \uparrow -OLS of OLS pair N of the output layer.

Case 2. If it is a \downarrow -OLS and $I = 0$, assign it as the \downarrow -OLS of OLS pair N .

For those cases other than the above two cases, go to (iii).

- (iii) If all OLS's in S are fetched, stop; otherwise, go to (ii).

2. AND operation

- (i) Set $I = 0$, $J = 0$ and $N = 0$, Then, start to scan the sorted S.
- (ii) Fetch one OLS from the sorted S. Perform $I \leftarrow I+1$ or $I \leftarrow I-1$ if it is a \uparrow -OLS or a \downarrow -OLS of the first input layer respectively, and perform $J \leftarrow J+1$ or $J \leftarrow J-1$ if it is a \uparrow -OLS or \downarrow -OLS of the second input layer respectively. Then,

Case 1. If it is a \uparrow -OLS of the first input layer, and $I = 1$ and $J \neq 0$; or it is a \uparrow -OLS of the second layer, and $I \neq 0$ and $J = 1$; then perform $N \leftarrow N + 1$ and assign it as the \uparrow -OLS of OLS pair N.

Case 2. If it is a \downarrow -OLS of the first input layer, and $I = 0$ and $J \neq 0$; or it is a \downarrow -OLS of the second input layer, and $I \neq 0$ and $J = 0$; then assign it as the \downarrow -OLS of OLS pair N.

For those cases other than the above two cases, go to (iii).

- (iii) If all OLS's in S are fetched, stop; otherwise, go to (ii).

3. ANDNOT operation

- (i) Set $I = 0$, $J = 0$ and $N = 0$. Then start to scan the sorted S.
- (ii) Fetch one OLS from the sorted S. Perform $I \leftarrow I+1$ or $I \leftarrow I-1$ if it is a \uparrow -OLS or \downarrow -OLS of the first input layer respectively, and perform $J \leftarrow J+1$ or $J \leftarrow J-1$ if it is a \uparrow -OLS or \downarrow -OLS of the second input layer respectively. Then,

Case 1. If it is a \uparrow -OLS of the first input layer, $I = 1$ and $J = 0$; then perform $N \leftarrow N+1$ and assign it as the \uparrow -OLS of OLS pair N.

Case 2. If it is a \uparrow -OLS of the second input layer and $I \neq 0$ and $J = 1$, then assign it as the \downarrow -OLS of OLS pair N.

Case 3. If it is a \downarrow -OLS of the second input layer and $I \neq 0$ and $J = 0$, then perform $N \leftarrow N+1$ and assign it as the \uparrow -OLS of OLS pair N.

Case 4. If it is a \downarrow -OLS of the first input layer and $I = 0$ and $J = 0$, then assign it as the \downarrow -OLS of OLS pair N.

For those cases other than the above four cases, go to (iii).

- (iii) If all OLS's in the sorted S are fetched, stop; otherwise, go to (ii).

4. XOR operation

- (i) Set $I = 0$, $J = 0$ and $N = 0$. Then start to scan the sorted S.
- (ii) Fetch one OLS from the sorted S. Perform $I \leftarrow I+1$ or $I \leftarrow I-1$ if it is a \uparrow -OLS or \downarrow -OLS of the first input layer respectively, and

and perform $J \leftarrow J+1$ or $J \leftarrow J-1$ if it is a \uparrow -OLS or \downarrow -OLS of the second input layer respectively. Then,

Case 1. If it is a \uparrow -OLS of the first input layer and $I = 1$ and $J = 0$, or it is a \uparrow -OLS of the second input layer and $I = 0$ and $J = 1$; then perform $N \leftarrow N+1$ and assign it as the \uparrow -OLS of OLS pair N.

Case 2. If it is a \uparrow -OLS of the first input layer and $I = 1$ and $J \neq 0$, or it is a \uparrow -OLS of the second input layer and $I \neq 0$ and $J = 1$; then assign it as the \downarrow -OLS of OLS pair N.

Case 3. If it is a \downarrow -OLS of the first input layer and $I = 0$ and $J \neq 0$, or it is a \downarrow -OLS of the second input layer and $I \neq 0$ and $J = 0$; then perform $N \leftarrow N+1$ and assign it as the \uparrow -OLS of OLS pair N.

Case 4. If it is a \downarrow -OLS of the first or second input layer and $I = 0$ and $J = 0$, then assign it as the \downarrow -OLS of OLS pair N.

For those cases other than the above four cases, go to (iii).

- (iii) If all OLS's in the sorted S are fetched, stop; otherwise, go to (ii).

V. LINKING OPERATION

Let S' be the set that contains all the OLS pairs at the current h and the previous h from the grouping operation. First, S' is sorted according to the Sorting Rule at $y = h$, then the Linking Operation will link the OLS's in S' at $y = h$ as follows:

Let N be a variable for identifying the link pair, then,

- (i) Set $N = 1$ and start to scan the sorted S' .
- (ii) Fetch two OLS's from the sorted S' and assign them to link pair N . The link pair are linked either by a common vertex or by a horizontal line segment of $y = h$.
- (iii) Set $N \leftarrow N + 1$
- (iv) If all OLS's in the sorted S' are fetched, stop; otherwise, go to (ii).

VI. TOPOLOGICAL OPERATIONS

1. Identify the regions in a layer

The OR operation can be applied to merge the joint polygons of the layer so that each polygon corresponds to a region.

Suppose that for each of the two input layers the operation to identify the regions in a layer has been performed such that each polygon corresponds to a region and is assigned a unique number. Then the operations for Recognizing the connections of two regions in two layers through contact(s) and Recognizing the CONTAIN relationship are as follows:

2. Recognize the connections of two regions

Let I , J and K be the three variables for counting and p_1 and p_2 are for identifying the polygon num-

bers of the first and second input layers respectively .

- (i) Set I, J and K equal to 0 . Then start to scan the sorted S .
- (ii) Fetch one OLS from the sorted S . Perform $I \leftarrow I+1$ or $I \leftarrow I-1$ if it is a \uparrow -OLS or \downarrow -OLS of the first input layer respectively; or $J \leftarrow J+1$ or $J \leftarrow J-1$ if it is a \uparrow -OLS or \downarrow -OLS of the second input layer respectively ; or $K \leftarrow K+1$ or $K \leftarrow K-1$ if it is a \uparrow -OLS or \downarrow -OLS of the contact layer. Then ,

Case 1. If it is a \uparrow -OLS of the first input layer , set p_1 equal to the polygon number from which it comes. Then if $J \neq 0$ and $K \neq 0$, polygon p_1 of the first input layer and polygon p_2 of the second input layer are connected through contact.

Case 2. If it is a \downarrow -OLS of the second input layer , set p_2 equal to the polygon number from which it comes . Then if $I \neq 0$ and $K \neq 0$, polygon p_1 of the first input layer and polygon p_2 of the second input layer are connected through contact .

Case 3. If it is a \uparrow -OLS of the contact layer and $I \neq 0$ and $J \neq 0$, then polygon p_1 of the first input layer and polygon p_2 of the second input layer are connected through contact .

For those cases other than the above three cases , go to (iii) .

- (iii) If all OLS's in the sorted S are fetched , stop ; otherwise , go to (ii) .

3. Recognize the CONTAINED relationship

Assume that any region in the first input layer is surrounded (CONTAINED) by a region in the second layer. We are to recognize which region in the first input layer is contained by which region in the second input layer.

- (i) Set $I = 0$ and $J = 0$. Then start to scan the sorted S .
- (ii) Fetch one OLS from the sorted S . Perform $I \leftarrow I+1$ or $I \leftarrow I-1$ if it is a \uparrow -OLS or \downarrow -OLS of the first input layer , or perform $J \leftarrow J+1$ or $J \leftarrow J-1$ if it is a \uparrow -OLS or \downarrow -OLS of the second input layer respectively. Then

Case 1. If it is a \uparrow -OLS of the first input layer , set p_1 equal to the polygon number of the fetched OLS .

Case 2. If it is a \downarrow -OLS of the second input layer and $I = 0$, then the polygon from which it comes is contained by polygon p_2 of the first input layer .

For those cases other than the above two cases , go to (iii)

- (iii) If all OLS's in the sorted S are fetched , stop ; otherwise , go to (ii) .

VII. CONCLUSION

The oriented line segment approach has the following advantages :

1. The algorithm is simple because the well estab-

lished topological properties of polygons and its oriented line segments is applied . The algorithm implementation to handle the practical LSI layout is not difficult because each OLS is represented by a fixed length record and the system SORT can be used to pre-sort the OLS's in the sequence that is easy to be manipulated.

3. It is straight forward to obtain OLS's from the polygons and the Linking algorithm provides the backward capability to form polygons from the OLS's , thus the OLS approach can easily interface with the existing softwares such as pattern generation programs .

Even there are a great number of companies developing the layout processing programs , it is hard to find a paper that describes the algorithm in deep . The authors hope that this paper will stimulate the readers interesting in the area and becoming appreciated the concept of oriented line segments .

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FIGURES

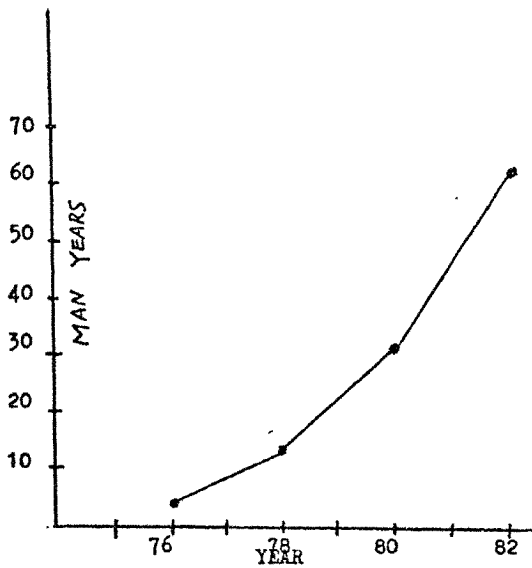


Figure 1. Man years for Planning Drawing, Changing and Checking of Random Logic

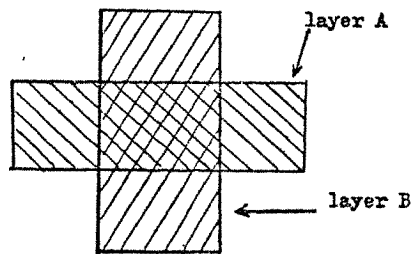


Figure 2(a)

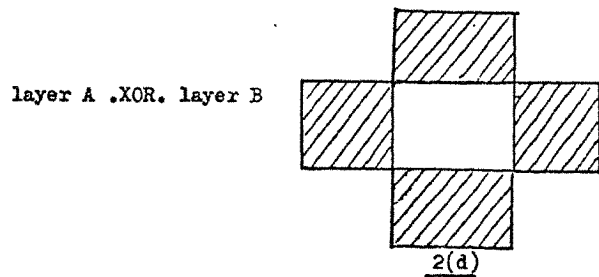
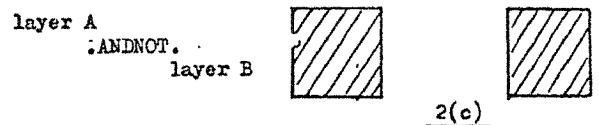
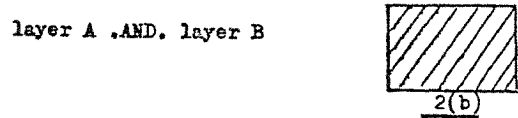
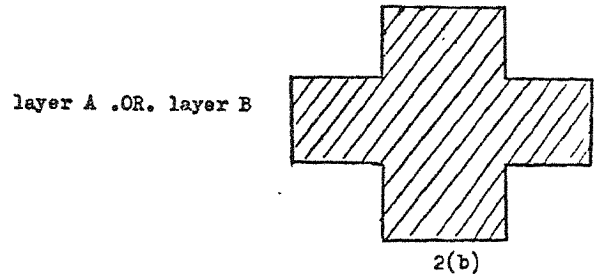


Figure 2. Logical Operations

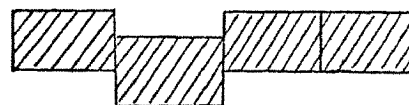


Figure 3(a) A region consists of joint polygons

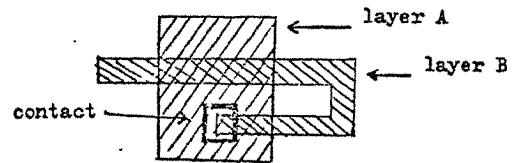


Figure 3(b). Two regions in two layers are connected by contact.

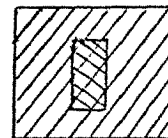
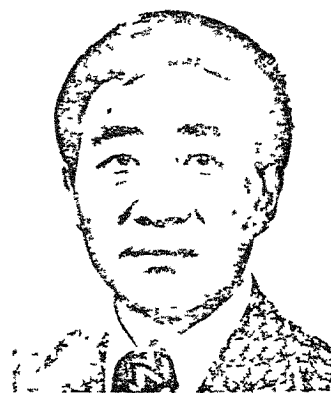


Figure 3(c). A region in one layer is surrounded by a region in the other layer

WAI-KAI CHEN
TECHNICAL BIOGRAPHY



Wai-Kai Chen (S' 61, M '61, SM '71, F '77) was born on December 23, 1936. He received the B.S. and the M.S. degrees in electrical engineering from Ohio University in 1960 and 1961, and the Ph.D. degree from University of Illinois in February 1964.

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Dr. Chen is a recipient of the 1967 Lester R. Ford Award of the Mathematical Association of America. He received a Research Institute Fellow Award from Ohio University in 1972, an Outstanding Educator of America Award in 1973, and a Baker Fund Award in 1974 and also in 1978 from Ohio University. In 1975, he received an Excellence in Teaching Award from College of Engineering and Technology. He is a Fellow of American Association for the Advancement of Science. In 1978, he received the Distinguished Professor Award from Ohio University. He was Program Chairman of the 1979 International Colloquium on Circuits and Systems, Taiwan. Current, he is a Distinguished Professor of Electrical Engineering, Ohio University, and an Associate Editor of the IEEE Transactions on Circuits and Systems. For the Fall semester, 1979-1980, he is a Visiting Professor of Electrical Engineering, University of Hawaii at Manoa.

GRAPHS AND FEEDBACK AMPLIFIER THEORY

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ABSTRACT

The paper presents a unified summary of the relationships between network topology and feedback amplifier theory. Topological formulas for the evaluation of the elements of the return difference and the null return difference matrices are given.

INTRODUCTION

It is well known that Bode's concept of return difference plays an important role in the design of feedback amplifiers (1-3). Among the many important properties, it can be shown that the return difference is a generalization of the concept of the feedback factor of the ideal feedback model, that the sensitivity function of the amplifier is closely related to the return difference, and that the return difference is basic to the study of the stability of the feedback amplifier and to the determination of its transmission and driving-point properties.

Several important extensions and generalizations of Bode's return difference concept have been reported (4-7). Tasny-Tschiasny (4) introduced the concept of return-difference matrix. The results so obtained are applicable to linear feedback networks that possess a multiplicity of physical feedback loops. Truxal (6) introduced the concept of the null return difference, which is shown to be useful in measurement situations and in the computation of the sensitivity. The extension of the null return difference to the concept of the null return-difference matrix was given by Sandberg (5) and Hakim (7), who demonstrated its use in the evaluation of the closed-loop gain and the driving-point impedance of a multiple-loop feedback network. Needless to say, these concepts have been modified and elaborated upon by many workers (8-17).

It was shown by Chen (18, 19) that although the return difference and the null return difference are not invariant with respect to the general transformations of the reference frame, they are invariant for the most common and important types of feedback networks. These results have been extended and generalized to the multiple-loop feedback networks by Elsherif and Chen (20).

In the present paper, we present a unified summary of many of these results, and indicate how the elements of the return-difference and the null return-difference matrices can be expressed in terms of the directed-tree and directed-two-tree admittance products in the associated digraph.

THE FIRST- AND SECOND-ORDER COFACTORS

Let \underline{Y} be the indefinite-admittance matrix of a feedback amplifier N . Denote by \underline{Y}_{ij} the submatrix obtained from \underline{Y} by deleting the row i and column j . In a similar way, $\underline{Y}_{rp,sq}$ denotes the submatrix derived from \underline{Y} by deleting the rows r and s and columns p and q . The first-order cofactors of the elements of \underline{Y} , which is of order n , are the scalar quantities defined by

$$Y_{ij} = (-1)^{i+j} \det \underline{Y}_{ij}, \quad (1)$$

$$Y_{rp,sq} = \text{sgn}(r-s) \text{sgn}(p-q) (-1)^{r+p+s+q} \cdot \det \underline{Y}_{rp,sq} \quad (2)$$

respectively, where $r, s, p, q \leq n$; and $\text{sgn } u = +1$ if $u > 0$, $\text{sgn } u = -1$ if $u < 0$, and $\text{sgn } 0 = 0$. It is well known that \underline{Y} is an equicofactor matrix (21) meaning that

$$Y_{ij} = Y_{uv} \quad (3)$$

for all i, j, u and v .

In a feedback network N , the general return difference $F_k(x)$ of N with respect to a network element x for a general reference value k is defined as the ratio of the two functional values assumed by the network determinant under the condition that the element x assumes its nominal value and the condition that the element x assumes the value k . This gives

$$F_k(s) = Y_{ij}(x)/Y_{ij}(k), \quad (4)$$

where we have exhibited the importance of the element x by writing $Y_{ij} = Y_{ij}(x)$. For $k = 0$, we write $F_0(x) = F(x)$, which becomes the ordinary return difference.

The concept of null return difference is found to be very useful in measurement situations and in the computation of the sensitivity for the feedback amplifiers (2, 6).

In the literature, the null return difference $\hat{F}(x)$ with respect to a voltage-controlled current source $I = xV$ for the zero reference value is defined to be one plus the negative voltage appearing at the controlling branch of the controlled source when the controlled source is replaced by an independent current source of x amperes and when the input current of the feedback amplifier is adjusted so that its output current is identically zero. Referring to the general configuration of a feedback amplifier as shown in Fig. 1, let us designate the input and output terminals as shown. As demonstrated by Chen (22), the null return difference

can be expressed as the ratio of the two functional values assumed by a second-order cofactor of the elements of the indefinite-admittance matrix \underline{Y} under the condition that the element x assumes its nominal value and the condition that the element x assumes the value k , that is

$$\hat{F}_k(x) = Y_{rp,sq}(x)/Y_{rp,sq}(k), \quad (5)$$

where, as before, we write $Y_{rp,sq}$ as $Y_{rp,sq}(x)$. Since

$$Y_{rp,sq}(x) = -Y_{sp,rq}(x) = -Y_{rq,sp}(x), \quad (6)$$

the null return difference $\hat{F}_k(x)$, as given in (5), is independent of the choice of the reference potentials for the input and output ports. In other words, there is no need to specify the terminal labels of the input and output ports; only the identification of these ports is required for the computation of $\hat{F}_k(x)$.

MULTIPLE-LOOP FEEDBACK NETWORKS

The extension of the scalar return difference and null return difference for a single loop feedback amplifier to the return-difference matrix and the null return-difference matrix for a multiple-loop feedback amplifier will be considered in this section.

In a multiple-loop feedback network N_m , let the elements of interest be represented by a rectangular matrix \underline{X} , which can either be a transfer-admittance matrix or a driving-point admittance matrix characterized by

$$\underline{I}_\alpha = \underline{X}\underline{V}_\beta, \quad (7)$$

where \underline{X} is of order q by p . If \underline{X} is a transfer-admittance matrix of the controlling parameters of the voltage-controlled current sources, \underline{V}_β represents a p -dimensional vector of the controlling voltages and \underline{I}_α a q -dimensional vector of controlled current sources. If \underline{X} represents a driving-point admittance matrix, \underline{I}_α and \underline{V}_β are of the same dimension, $p = q$, and they represent current and voltage vectors of a p -port network. The matrix \underline{X} is important in terms of its effects to the whole system and is imbedded in the rest designated by \tilde{N}_m as shown in the block diagram of Fig. 2, where I_s denotes the input current and V_o the output voltage of N_m . Since the network \tilde{N}_m is linear, it can be characterized by

$$\underline{V}_\beta = \underline{A}\underline{I}_\alpha + \underline{B}\underline{I}_s, \quad (8a)$$

$$\underline{V}_o = \underline{C}\underline{I}_\alpha + \underline{D}\underline{I}_s, \quad (8b)$$

where \underline{A} , \underline{B} , \underline{C} and \underline{D} are transfer-impedance matrices of order $p \times q$, $p \times 1$, $1 \times q$, and 1×1 , respectively.

Denote by $\underline{1}_p$ the identity matrix of order p . Then the square matrix

$$\underline{F}(\underline{X}) = \underline{1}_p - \underline{A}\underline{X} \quad (9)$$

is called the return difference matrix of N_m with respect to the matrix \underline{X} , and is a direct generalization of Bode's scalar return difference (1) with respect to a single element x .

The null return difference matrix of N_m with

respect to \underline{X} is defined by the square matrix

$$\hat{\underline{F}}(\underline{X}) = \underline{1}_p - \hat{\underline{A}}\underline{X}, \quad (10)$$

where

$$\hat{\underline{A}} = \underline{A} - (1/D)\underline{B}\underline{C}, \quad (11)$$

provided that $D \neq 0$.

As shown by Kuh (9), the closed-loop transfer impedance $w(\underline{X})$, defined as the ratio of the output voltage V_o to input current I_s , can be expressed in a very compact way by making use of the return difference and null return difference matrices:

$$w(\underline{X}) = [w(0) \det \hat{\underline{F}}(\underline{X})] / [\det \underline{F}(\underline{X})]. \quad (12)$$

The sensitivity function $S(x_{ij})$, which is defined as the ratio of the fractional change in a transfer function $w(\underline{X})$ to the fractional change in an element x_{ij} of \underline{X} , can be written as

$$S(x_{ij}) = \frac{\det \underline{F}(\underline{X})|_{x_{ij}=0}}{\det \underline{F}(\underline{X})} \left[1 - \frac{w(\underline{X})|_{x_{ij}=0}}{w(\underline{X})} \right]. \quad (13)$$

TOPOLOGICAL FORMULAS

In this section, we present topological formulas for the evaluation of feedback parameters in terms of the products of admittances associated with the directed trees and directed two-trees in the associated digraph of the feedback amplifier.

The Digraph

For a given feedback amplifier N , let $G(\underline{Y})$ be the n -node directed graph, called the digraph of N associated with its indefinite-admittance matrix

$$\underline{Y} = [y_{ij}], \quad (14)$$

which is of order n , as follows. There is an edge directed from node i to node j with weight $-y_{ij}$, $i \neq j$, in $G(\underline{Y})$ if and only if $y_{ij} \neq 0$. We remark that the diagonal elements of \underline{Y} have no direct bearing on the construction of $G(\underline{Y})$. A careful study of this rule indicates that $G(\underline{Y})$ can be greatly simplified if we agree that an undirected edge stands for a pair of oppositely directed edges such that the weight (admittance) associated with each directed edge in the pair is the same as that of the undirected edge. With this simplification, it is clear that the resulting $G(\underline{Y})$ is a composite graph, and for most practical and commonly used networks, $G(\underline{Y})$ can easily be obtained from the equivalent network of the feedback amplifier N by inspection. For a detailed account of this result and all the variations and ramifications, the reader is referred to Chen (21). We shall further agree that the directed edges in the composite graph $G(\underline{Y})$ will be called the active edges, and the undirected edges the passive edges.

A directed tree with reference node r in $G(\underline{Y})$ denoted by t_r , is a tree in which each of its active edges, if they exist, is directed toward the reference node r in the unique path defined by the active edge in the tree. In particular, trees consisting only of passive edges are also directed trees. A directed two-tree with reference nodes i and j , denoted by $t_{i,j}$, is a two-tree separating

the nodes i and j , each of its components being a directed tree with reference node i or j in some subgraph of $G(\underline{Y})$. Also, denote by $t_{iu,jv}$ a directed two-tree $t_{i,j}$ in which nodes i and u are in one component and nodes j and v in the other component; the first subscripts i and j being the reference nodes. For a subgraph g of $G(\underline{Y})$, denote by $f(g)$ the product of the weights associated with the edges of g with $f(\emptyset) = 0$, \emptyset being the null graph.

With these preliminaries, we can now state the following known results, whose proof can be found in Chen (21):

$$Y_{uv} = T_k = \sum_{t_k} f(t_k), \quad (15)$$

$$Y_{rp,sq} = W_{rp,sq} = T_{rp,sq} - T_{rq,sp}, \quad (16)$$

where the choice of the reference node k is arbitrary and

$$T_{rp,sq} = \sum_{t_{rp,sq}} f(t_{rp,sq}). \quad (17)$$

The Return Difference

Substituting (15) in (4) yields the desired formula for the return-difference function

$$F_k(x) = T_1(x)/T_1(k), \quad (18)$$

where $T_1 = T_1(x)$.

The Null Return Difference

Combining (5) and (16) gives

$$\hat{F}_k(x) = W_{rp,sq}(x)/W_{rp,sq}(k), \quad (19)$$

where $W_{rp,sq} = W_{rp,sq}(x)$.

The Return Difference Matrix

In this section, we present topological formulas for the evaluation of the elements of the return difference matrix.

Referring to the general configuration of Fig. 3, the controlled sources can be represented by the equation

$$\begin{bmatrix} I_{\alpha 1} \\ I_{\alpha 2} \\ \vdots \\ I_{\alpha q} \end{bmatrix} = \begin{bmatrix} x_{11} & x_{12} & \cdots & x_{1p} \\ x_{21} & x_{22} & \cdots & x_{2p} \\ \vdots & \vdots & \ddots & \vdots \\ x_{q1} & x_{q2} & \cdots & x_{qp} \end{bmatrix} \begin{bmatrix} V_{\beta 1} \\ V_{\beta 2} \\ \vdots \\ V_{\beta p} \end{bmatrix}. \quad (20)$$

As indicated in (8a), A is the matrix relating the controlling voltage vector V_{β} to the controlled current vector I_{α} after the input excitation I_s has been set to zero. Under this situation, the (i,j) -element of \underline{AX} is equal to the voltage $\tilde{V}_{\beta i}$ appearing at the i th controlling branch of Fig. 3 when the controlled current sources $I_{\alpha k}$ ($k = 1, 2, \dots, q$)

have been replaced by the independent current sources of strengths x_{kj} , as depicted in Fig. 4. Thus, with

$$\underline{F}(\underline{X}) = [F_{ij}] \quad (21)$$

we have for the j th column elements of $\underline{F}(\underline{X})$

$$F_{ij} = -\tilde{V}_{\beta i}, \quad i \neq j, \quad (22a)$$

$$= 1 - \tilde{V}_{\beta i}, \quad i = j. \quad (22b)$$

Since the network is linear, the voltage $\tilde{V}_{\beta i}$ due to the independent current sources x_{kj} can be obtained by considering each source separately, and the result is given by

$$Y_{uv}(0)\tilde{V}_{\beta i} = \sum_{k=1}^q x_{kj} Y_{d_k a_i, c_k b_i}(0). \quad (23)$$

Appealing to (15) and (16), we have for $i \neq j$

$$T_m(0)F_{ij} = \sum_{k=1}^q x_{kj} W_{d_k b_i, c_k a_i}(0); \quad (24)$$

and for $i = j$

$$T_m(0)F_{ii} = T_m(0) + \sum_{k=1}^q x_{ki} W_{d_k b_i, c_k a_i}(0). \quad (25)$$

In the special situation where \underline{X} is diagonal, which occurs most often in practice, (24) and (25) reduce to

$$T_m(0)F_{ij} = x_{jj} W_{d_j b_i, c_j a_i}(0) \quad (26)$$

for $i \neq j$, and

$$\begin{aligned} T_m(0)F_{ii} &= T_m(0) + x_{ii} W_{d_i b_i, c_i a_i}(0) \\ &= T_m(\underline{X}^{ii}), \end{aligned} \quad (27)$$

where \underline{X}^{ij} is the matrix derived from \underline{X} by setting all of its elements to zero except x_{ij} . Thus, \underline{X}^{ij} is the matrix consisting only of zeros except the i th row and j th column element, which is x_{ij} .

We remark that directed trees and two-trees in (24)-(27) are to be evaluated in the digraph obtained from $G(\underline{Y})$ by setting to zero all the weights corresponding to the elements of \underline{X} . If \underline{X} is the matrix of the controlling parameters, the resulting digraph is simply the graph representing the feedback network when the input excitation and all the controlled sources have been removed, and the directed trees and two-trees become the ordinary trees and two-trees.

The Null Return Difference Matrix

The null return difference matrix is found to be very useful in measurement situations and in the computation of the sensitivity for the multiple-loop feedback amplifiers (2, 23). In the following, we present topological formulas for the evaluation of its elements.

The null return difference matrix $\hat{\underline{F}}(\underline{X})$, as defined in (10), is the return difference matrix with respect to \underline{X} when the input excitation I_s is adjusted so that the output voltage V_o of Fig. 4 (I_s is not explicitly shown) is identically zero. Thus, $\hat{\underline{A}}$ is the matrix relating the controlling volt-

age vector V_{β} to the controlled current vector I_q when the input excitation I_s is adjusted so that the output voltage V_o is identically zero. Under this situation, to compute the j th column elements of $\hat{A}X$, we replace the controlled current sources I_{ck} ($k = 1, 2, \dots, q$) in Fig. 3 by the independent current sources of strengths x_{kj} , as depicted in Fig. 4, and then adjust the input excitation I_s so that the output voltage V_o is identically zero. The voltage $\tilde{V}_{\beta i}$ appearing at the i th controlling branch is the (i, j) -element of $\hat{A}X$. Let the desired input excitation be designated by I_{sj} ($j = 1, 2, \dots, p$). Applying the principle of superposition, the output voltage V_o is given by

$$Y_{uv}(0)V_o = I_s Y_{rp, sq}(0) + \sum_{k=1}^q x_{kj} Y_{d_k p, c_k q}(0). \quad (28)$$

Setting $V_o = 0$ and using (16), the desired input excitation can be computed by the formula

$$I_{sj} = \sum_{k=1}^q x_{kj} W_{d_k q, c_k p}(0) / W_{rp, sq}(0). \quad (29)$$

The voltage appearing at the i th controlling branch is found to be

$$Y_{uv}(0)\tilde{V}_{\beta i} = I_{sj} Y_{ra_i, sb_i}(0) + \sum_{k=1}^q x_{kj} Y_{d_k a_i, c_k b_i}(0). \quad (30)$$

Let

$$\hat{F}(X) = [\hat{F}_{ij}]. \quad (31)$$

Then from (30) in conjunction with (15) and (16), we obtain

$$T_m(0)\hat{F}_{ij} = \sum_{k=0}^q x_{kj} W_{d_k b_i, c_k a_i}(0), \quad i \neq j, \quad (32)$$

$$T_m(0)\hat{F}_{ii} = T_m(0) + \sum_{k=0}^q x_{ki} W_{d_k b_i, c_k a_i}(0), \quad (33)$$

where $x_{0j} = I_{sj}$, $c_0 = s$ and $d_0 = r$.

In the special situation where X is diagonal, (32) and (33) reduce to

$$T_m(0)\hat{F}_{ij} = I_{sj} W_{rb_i, sa_i}(0) + x_{jj} W_{d_j b_i, c_j a_i}(0) \quad (34)$$

for $i \neq j$, and from (29) and (30)

$$\begin{aligned} \hat{F}_{ii} &= 1 - [I_{si} Y_{ra_i, sb_i}(0) + x_{ii} Y_{d_i a_i, c_i b_i}(0)] / Y_{uv}(0) \\ &= 1 + x_{ii} \dot{Y}_{rp, sq}(0) / Y_{rp, sq}(0), \end{aligned} \quad (35)$$

where $\dot{Y}_{rp, sq}(0)$ denotes the partial derivative of $Y_{rp, sq}(X)$ with respect to the element x_{ii} evaluated at $X = 0$. Using \dot{x}^{ii} as defined in (27), it is not difficult to show that $Y_{rp, sq}(X^{ii})$ can be expanded as

$$Y_{rp, sq}(X^{ii}) = Y_{rp, sq}(0) + x_{ii} \dot{Y}_{rp, sq}(0). \quad (36)$$

Substituting (36) in (35) yields

$$\hat{F}_{ii} = W_{rp, sq}(X^{ii}) / W_{rp, sq}(0). \quad (37)$$

CONCLUSIONS

In the paper, we have presented a unified summary of the relationships between network topology and feedback amplifiers. Topological formulas for the evaluation of the elements of the return difference matrix and the null return difference matrix in terms of the sums of the directed-tree and directed-two-tree admittance products are given. The significance of these formulas is that it not only provides a short-cut for the evaluation of the feedback matrices, but also gives an insight into the behavior of the feedback amplifier under consideration.

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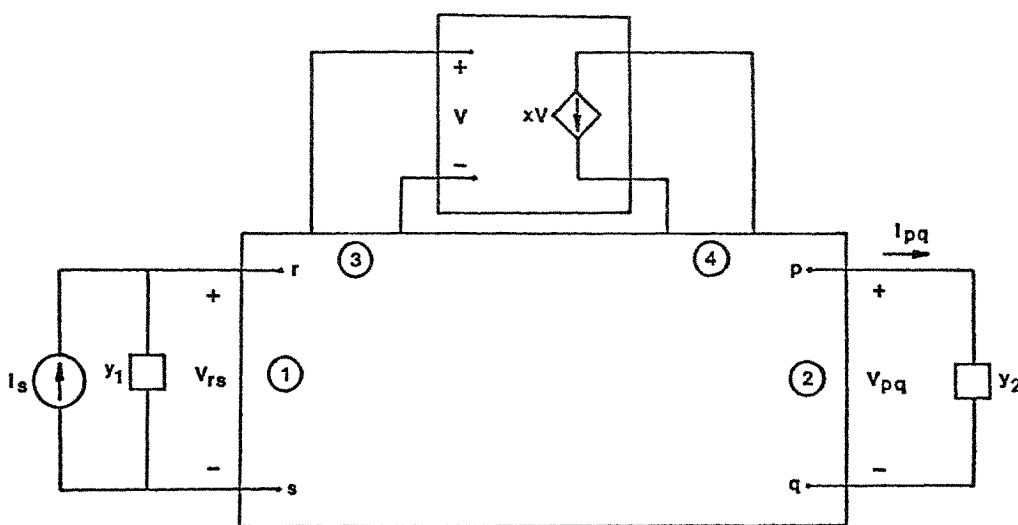


Fig. 1. General Configuration of a Feedback Amplifier Network.

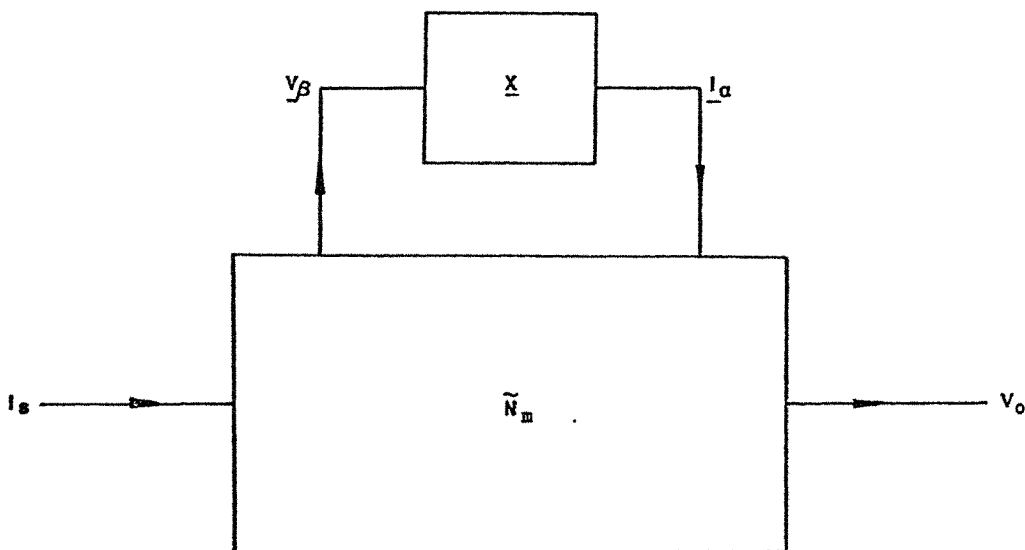


Fig. 2. The General Configuration of a Multiple-Loop Feedback Amplifier.

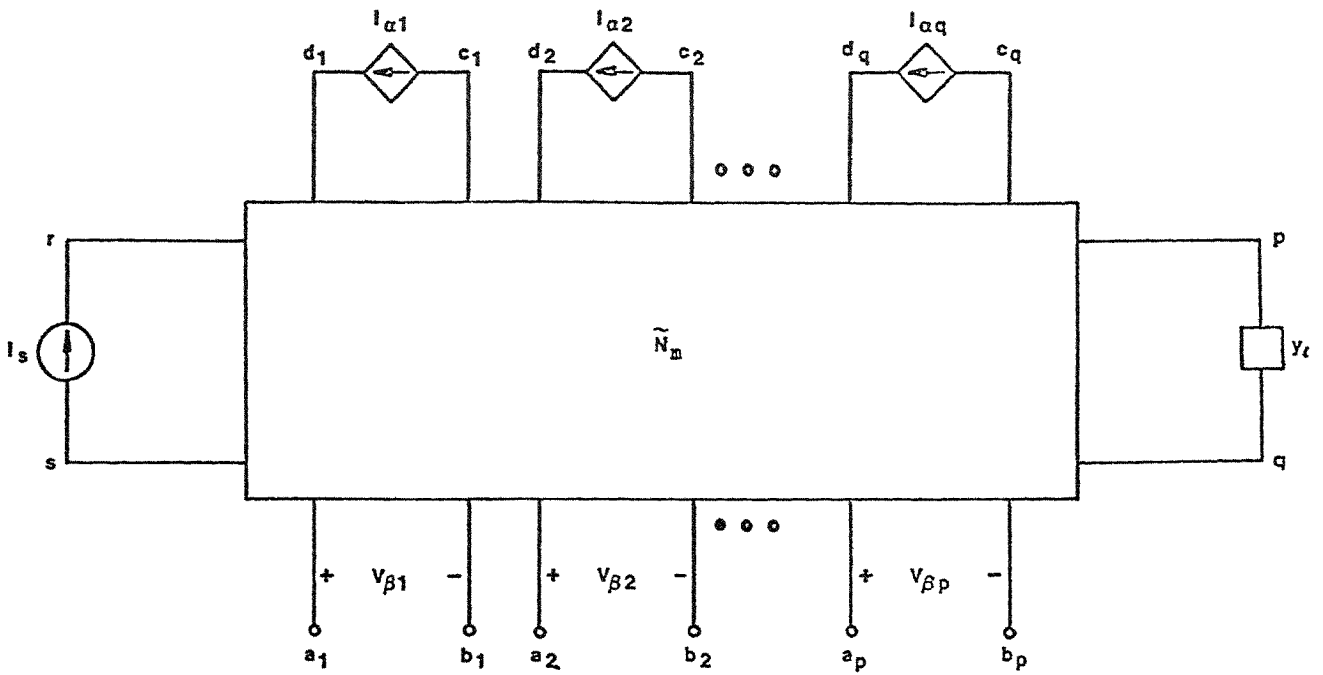


Fig. 3. The General Representation of the Voltage-Controlled Current Sources in a Multiple-Loop Feedback Amplifier.

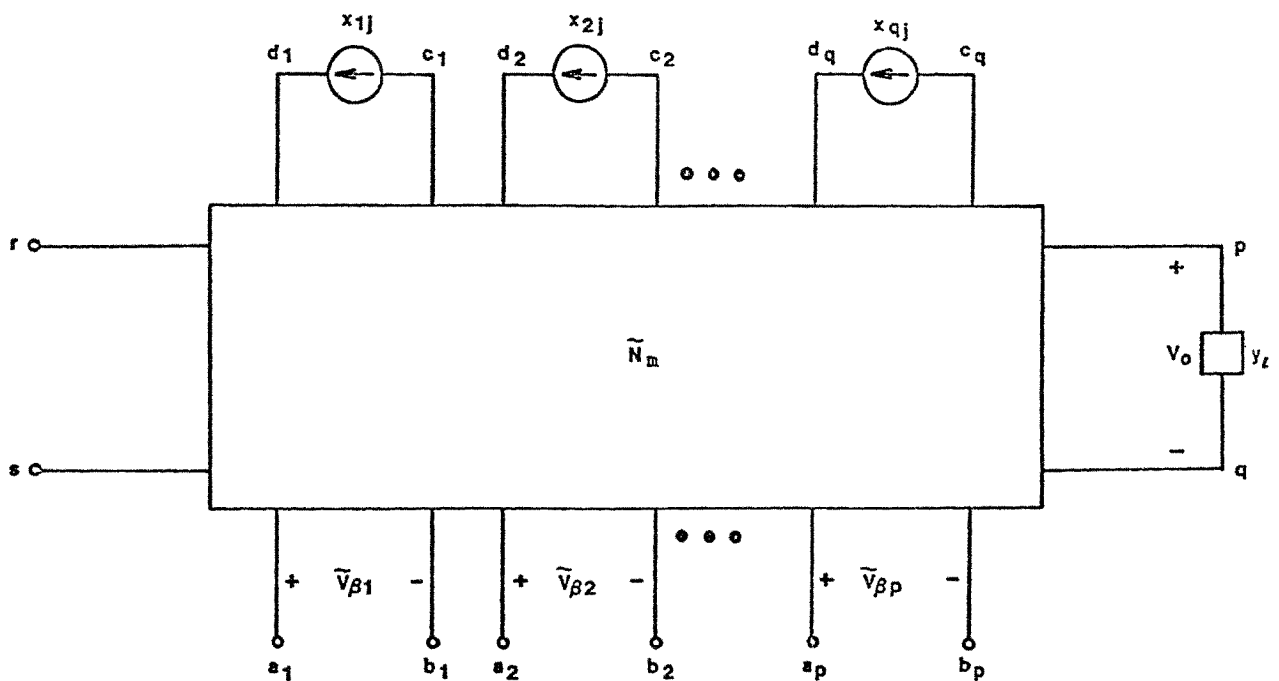


Fig. 4. The Physical Interpretation of the Elements of the Return Difference Matrix with Respect to the Controlling Parameters of the Voltage-Controlled Current Sources.

TECHNICAL BIOGRAPHY - D.A. MLYNSKI

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ABSTRACT

Existing layout concepts as used by electronic industry for LSI circuit layout are compared with the demands of VLSI circuit layout. The hierarchical layout approach is discussed and also the following new concepts: Maximal partitioning using cliques, multilayer planarization using Boolean equations, geometrical placement using a contour language and multilayer routability test using logical operations.

INTRODUCTION

System designers are used to a top-down definition of different functional levels, e.g. key building blocks or subsystems, gates and basic circuit elements (Table 1).

Functional Level	Layout Level
System	Chip
Subsystem	Macro
Gate	Cell
Circuit Element	Device

top-
down
↓

 ↑
Bottom-
up

Table 1. Hierarchical Levels

However, since the early years of LSI the layout philosophy has been based rather on a bottom-up definition of layout levels. Moreover, on the cell level two gate array concepts are in use which do not provide macro levels (Table 2):

- (i) master slice concept
- (ii) standard cell concept

Cell Concept	Cell Constraint	Array
Master Slice	Rectangles of uniform size and shape	Matrix array
Standard Cell	Rectangles of uniform height	Line array
General Cell	Rectangular polygons	Arbitrary

Table 2. Cell Concepts for LSI and VLSI

The main advantage of these concepts is that the algorithmic difficulties of layout problems, especially of placement, are considerably reduced because of the more or less regular gate array. Efficient heuristic algorithms for placement (1-2) and for channel routing (3-5) are available and have been implemented in computer aided layout systems (6-7).

The main drawbacks are that channel-routing tends to long routing paths in parallel and, hence, to higher signal propagation times and signal crosstalk, and, still more important, that without availability of macro levels the gate array approach hardly allows for a hierarchical layout. Obviously, these disadvantages become more serious with increasing scale of integration.

A third layout method in use is the general cell concept or custom design (Table 2). This provides a greater degree of freedom for shape and position of cells and position of pins on cell periphery. The advantages of this concept are more design flexibility, minimal chip area and, perhaps most important for VLSI, the availability of macros and hierarchical layout (8-9).

Hence, the general cell concept avoids the disadvantages of the more standardized gate array, however, on the expense that the algorithmic problems are much more complex and difficult. Many problems are still unsolved. So far, there is no working computer aided layout system based on this concept. Custom design method is in use only for manual design of LSI circuits on the device level for handling the necessarily less uniform devices and on the cell level if the single chip is produced in millions and consequently, design time does not dominate the overall production costs.

Nevertheless, it is a strong feeling of many in the field that making the general cell concept accessible to computer aided design it will be of optimal use to different design levels -- device, cell and macro level --, to different technologies and to both digital and analog circuits. Therefore it will be especially optimal for VLSI systems housing analog and digital circuits, random and regular logic and different technologies on a single chip.

HIERARCHICAL LAYOUT APPROACH

A hierarchical layout approach consists of three main steps:

1) Partitioning.

The given system has to be partitioned hierarchically on a given number of levels. Usually, this will be based on a functional top-down definition of building blocks, gates etc., but also should be adequate to layout considerations by proper mapping between functional units and layout units.

When partitioning has been done properly, the remaining two steps apply to each hierarchical level. In the following the functional terms circuit/component and the layout terms chip/cell, respectively, are used to represent any hierarchical level.

2) Topological layout.

The given circuit schematic diagram of components and interconnections is converted into a schematic layout or stick layout. This is only a first pass of approximate layout which provides a global chip planning by proper top-down algorithms. It does not take care of any geometrical constraints (e.g. dimensions of cells and wire routes) but only of topological constraints (global placement and wirability). Hence, the resulting schematic layout does not include accurate geometrical dimensions and positions.

3) Geometrical layout

The schematic layout is converted into the actual layout. Only in this final pass all the geometrical requirements and design constraints are taken into account. Top-down or bottom-up placement algorithms or combinations of both may be used. Routing still may be split into two steps: Routability tests during the steps of placement improvement and actual routing after placement is finished.

Finally, it should be mentioned that interactive methods are necessary in all three parts of this approach at proper intermediate steps for the efficient handling of special technological design-rules and unforeseen constraints.

The following sections give a discussion of some of the problems encountered in a hierarchical layout approach and possible solution methods and algorithms. They all are aimed to an implementation on a minicomputer with interactive graphics.

PARTITIONING USING CLIQUES

Heuristic partitioning usually is done by bottom-up techniques of growing components from "seeds." For a good decision on the number Γ of seeds a knowledge of the upper bound Γ_{\max} is

necessary. It can be found by maximum partitioning. However, this should not be based on devices but rather on the preceding top-down definition of functional units.

Each functional unit incident to n distinct interconnection nets is mapped into a complete graph on n nodes, i.e. into a clique (10). Hence, a graph representation of the given circuit is an aggregation of cliques. Clique aggregations have special properties which benefit the partitioning procedure. Especially, a clique is the only type of graph which does not possess an articulation set, i.e. cannot be partitioned.

The problem can be now restated as follows: Given a circuit with clique aggregation C . Find a

minimum articulation set of C with maximum articulation degree Γ_{\max} .

The algorithm for maximal partitioning of graphs based on this clique concept is described in (10) and has been implemented on a DEC-computer PDP 11/60.

MULTILAYER PLANARIZATION

A main problem of topological layout is to find a schematic layout with an approximate placement of cells that optimally benefits the routing.

Definition 1. Given an undirected bipartite graph G representing the given circuit. A minimum set of branches B such that $G-B$ is planar is called a minimum planarizing set of G .

The assignment of the elements of B to proper layers depends on technology. Different planarizations, i.e. different minimum planarizing sets, may cause different parasitic effects. Therefore, it is worthwhile to find the family $\{B_v\}$ of all minimum planarizing sets B_v in order to allow for an optimum choice.

In (11) a Boolean planarity function F has been introduced based on the following definition.

Definition 2. A binary variable u_{λ}^j is associated with branch j in layer λ such that:

$$u_{\lambda}^j = \begin{cases} 0 & \text{if branch } j \text{ is placed in layer } \lambda \\ 1 & \text{if branch } j \text{ is NOT placed in layer } \lambda. \end{cases}$$

A necessary and sufficient condition for planar multilayer layout of a circuit with planarity function $F(u)$ of its associated circuit graph is (L = number of layers):

$$\sum_{\lambda=1}^{L-1} F(u_{\lambda}) + F(\prod_{\lambda=1}^{L-1} \bar{u}_{\lambda}) = 0,$$

where π denotes the Boolean AND and Σ the OR operator, as usually. The planarity function $F(u)$ of the given circuit graph can be found by detection of wreathes (11).

For $L = 2$ the planarity equation reduces to:

$$F(u) + F(\bar{u}) = 0.$$

The set of solution vectors u corresponds to the family $\{B_v\}$. Each single solution vector u represents a planar schematic layout which is found by planar embedding of G according to the values of the elements in the solution vector u . The method is well-adopted to computer implementation. Well-known minimization techniques of Boolean algebra can be used to optimize the solution.

GEOMETRICAL PLACEMENT

The topological placement using multilayer planarization is a top-down technique. Hence, it

seems appropriate to combine this with a bottom-up geometrical placement. The procedure starts with a first cell and adds a single cell in each step of the procedure. Well-known constructive placement algorithms can be used for this step (12-13). However, they shall not be based on the circuit schematic diagram but rather on the schematic layout as represented by the planarized circuit graph.

Each single cell to be started with or to be added is a rectangular polygon of any complexity, i.e. of any number of rectangular corners. Consequently, the same holds for the resulting layout in all intermediate steps of the constructive placement.

Since the inner layout of cells is to be done in a different level of the hierarchic layout approach a description of layout contours is sufficient on the cell level. This can be most efficiently done by a layout language using 12 different corner types (14). They differ from each other by two informations:

- (i) in which direction a corner is approached and
- (ii) change of direction from horizontal to vertical and vice versa at the corner.

(Supposed is a mathematical positive passage along the contour.) The complete description of a layout structure is given by an ordered corner sequence:

$$\begin{pmatrix} C1 \\ D1 \end{pmatrix} \begin{pmatrix} C2 \\ D2 \end{pmatrix} \begin{pmatrix} C3 \\ D3 \end{pmatrix} \dots \dots \begin{pmatrix} Cn \\ Dn \end{pmatrix},$$

where C_i is the type of corner i and D_i its distance to the next corner in order.

Integer numbers can be associated with the corner types. Then, basic layout operations, e.g. rotations by multiples of 90° and flipping of layout structures, can be done efficient by INTEGER operations.

MULTILAYER ROUTABILITY TEST

Routerability has to be tested at proper steps of the hierarchical layout procedure based on the approximate or final placement of cells. The problem can be stated as follows: Given an order of nets and layout structures in the different layers (cells and routing paths). Test whether the next net is routable and find layer assignment and vias.

A strict automatic multilayer routerability test (15) has been based on a set theoretic description and processing of the given layout structures in all layers. The following two concepts are essential:

- (i) Domain is the union of all points in a single layer, which are planar routable within this layer.
- (ii) Two domains in adjacent layers are called incident if their intersection is not empty.

Technologically the incidence of two domains opens the possibility of a via between adjacent layers. Since the basic concept is free of any

metric it is independent of technology. It can be adjusted to any technology by implementing metric constraints.

The routerability test is based on the following:

Theorem. A net with m pins is routable on n layers if and only if the following holds: An ordered sequence of domains $\{A, B, C, \dots, Z\}$ exists for each pin pair $\{a, z\}$ in a set of $(m-1)$ independent pairs of pins of the net such, that $a \in A$ and $z \in Z$ and adjacent domains in the sequence are incident.

The routerability test is described in (15). It only needs logical operations and is independent of the choice of a starting pin.

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FUZZY TENSIONS AND POTENTIALS IN
QUALITATIVE ANALYSIS OF NETWORK PROBLEMS

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ABSTRACT

A new concept of fuzzy tension and fuzzy potential is proposed as a mathematical tool for qualitative analysis of network problems. In this paper we first describe modeling of curriculum networks and fail-safe networks in which the concept of fuzzy tension appears naturally as an well-balanced curriculum plan or reliability assignment. Algebraic properties of fuzzy tensions and potentials are thoroughly investigated and consistency of specifications is shown to be expressible by a simple condition on circuits.

MODELING OF CURRICULUM AND FAIL-SAFE NETWORKS

1. Curriculum Networks

A curriculum of an educational institute or program is an interconnection of course works and can be modeled by a weighted directed graph $G=(V,E)$ of the node set V and edge set E . A node x represents a state of education and an edge $e=(x,y)$ represents a course work whose teaching starts from state x and ends at state y . Course e possesses educational contents: maximum goal $\beta(e)$ and minimum requirement $\alpha(e)$. $\alpha(e)$ is a list of teaching items to be covered by the teacher and associated grades of the student's knowledge level. An actual scholastic achievement $t(e)$ gained from course work e lies somewhere inbetween

$$\alpha(e) \leq t(e) \leq \beta(e).$$

Here we express α (or β , t) by a vector

$$\alpha(e) = (\alpha_1(e), \alpha_2(e), \dots, \alpha_L(e))$$

where component value $\alpha_i(e)$ represents the grade of knowledge level or scholastic gain on teaching item $\#i$ from course work e . The component value may be 1 or 0 if knowledge level or scholastic gain is yes or no type nature, but often assumes a real number in $[0,1]$. Note that these quantities are regarded as fuzzy sets.

We assume the following notations and conventions.

- (1) $\alpha \leq \beta$ iff $\alpha_i \leq \beta_i$ for all i
- (2) $\alpha \vee \beta = \gamma$, $\gamma_i = \max(\alpha_i, \beta_i)$
- (3) $\alpha \wedge \beta = \gamma$, $\gamma_i = \min(\alpha_i, \beta_i)$
- (4) $\alpha \sim \beta = \gamma$, $\gamma_i = \begin{cases} \alpha_i & \text{if } \alpha_i > \beta_i \\ 0 & \text{otherwise} \end{cases}$

$$(5) \text{ } \emptyset = (0, 0, \dots, 0), \quad I = (1, 1, \dots, 1).$$

When the component value is 1 or 0 type, α (or β , t) is just the characteristic value representation of a subset of a finite teaching item set $U = \{\#1, \#2, \dots, \#L\}$ and the above notations are reduced to the ordinary set theoretic notations, $\subset, \cup, \cap, -$.

A node x represents a state of knowledge level at node x of the curriculum network $N=(G, \alpha, \beta)$ where graph G represents a precedence relation among course

works. A quantitative measure of the student's knowledge level at node x is denoted by a fuzzy set $\pi(x)$. π and t are assumed to obey the following rule.

- (a) For each edge $e=(x,y)$ in E
 $\alpha(e) \leq t(e) \leq \beta(e)$, $\pi(y) = \pi(x) \vee t(e)$,
- (b) If two edges $a=(x,z)$ and $b=(y,z)$ are incident to node z , we require a balancing condition
 $\pi(x) \vee t(a) = \pi(y) \vee t(b)$
to hold.

Reasons behind these rules are as follows (no generality is lost even if discussion is made on a single teaching item, say $\#i$): Rule (a) expresses nature of learning. Understanding of $\#i$ is hierarchical so that gain $t_i(e)=0.5$ does not contribute to an increase in knowledge if the initial knowledge level is already higher, say $\pi_i(x)=0.6$, but does contribute when the initial level is lower, say $\pi_i(x)=0.4$. Hence our assumption is that learning takes place only when the gain exceeds the initial level. Rule (b) expresses balanced teaching of well-coordinated curriculum. Suppose unbalance $\pi(x) \vee t(a) \neq \pi(y) \vee t(b)$ has taken place in Fig.1

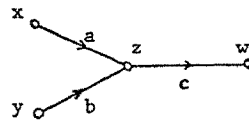


Fig.1 Explanation of rule (b), the balancing condition at node z .

For course work $c=(z,w)$, the teacher must base his teaching on students' common knowledge level at node z . Some students take a.c combination with $\pi(x) \vee t(a)$ and others b.c combination with $\pi(y) \vee t(b)$. Hence

$$\pi(z) = [\pi(x) \vee t(a)] \wedge [\pi(y) \vee t(b)].$$

This unbalance may be viewed as loss and can be avoided by good coordination among courses by imposition of rule (b).

Good coordination is expressed more rigorously by Kirchhoff's voltage law on fuzzy sets,

$$\text{FKVL: } \sum_{e \in L^+} t(e) = \sum_{e \in L^-} t(e)$$

for all circuits $L=L^+ \cup L^-$ where L^+ (or L^-) is the set of forward (or backward) edges whose edge direction agrees (or disagrees) with the circuit orientation. Scholastic gain t satisfying FKVL is called a fuzzy tension on the curriculum network N . It is quite natural to expect some progress from any course work, hence

$$\text{Monotonicity: } \pi(x) \leq \pi(y)$$

holds for all $e=(x,y)$ in E . In general a mapping from the node set V into fuzzy set is called a fuzzy potential of G if it satisfies the monotonicity. A curriculum is a fuzzy tension satisfying

$$\text{Admissibility: } \alpha(e) \leq t(e) \leq \beta(e)$$

for all edges in E.

Problems immediately confronting us are

- feasibility condition of existence of admissible tensions in N (consistency of requirement $\alpha(e)$ and goal $\beta(e)$).
- construction of an admissible tension in N.
- maximum scholastic achievement of the program.

In this paper we will present answers to these questions by means of thorough investigation of algebraic properties of fuzzy tensions and potentials.

2. Fail-Safe Networks

Functional interconnection of a system is conveniently expressed by a directed graph $G=(V,E)$ where a node represents a subsystem and an edge represents a functional connection between associated nodes. To each edge $e=(x,y)$ there is a weight $\beta(e)$ which is a list of failure susceptibility $\beta_i(e)$ (not necessarily probability) of node x affecting node y with regard to failure cause #i in the failure cause set $U=\{\#1, \#2, \dots, \#F\}$. Larger value $\beta_i(e)$ more susceptible to failure cause #i.

If two edges $a=(x,y)$ and $b=(y,z)$ are in tandem, the failure cause accumulates and a higher susceptibility dominates a lower one for the same cause. Hence letting $\pi(x)$ denote the failure potential at node x, we have

$$\pi(z) = \pi(x) \vee \beta(a) \vee \beta(b).$$

In the network, incidence of two edges $a=(x,z)$ and $b=(y,z)$ into node z means a fail-safe mechanism operating at z such that, for failure cause #i, the mechanism chooses the smaller susceptibility for $\pi(z)$

$$\pi(z) = [\pi(x) \vee \beta(a)] \wedge [\pi(y) \vee \beta(b)].$$

In designing a fail-safe network, we have some control over distribution of available resources to realizing failure susceptibility of each interconnection. Realized susceptibility of interconnection e, $t(e)$, is bounded above by the network specification $\beta(e)$ and below by technology $\alpha(e)$. Therefore susceptibility assignment t satisfies the admissibility $\alpha(e) \leq t(e) \leq \beta(e)$ on each e in E. Since unbalanced assignment is waste of resources, we should require the balancing condition $\pi(x) \vee t(a) = \pi(y) \vee t(b)$.

We proceed as before in the case of the curriculum network and conclude that well-balanced reliability assignment may be adequately modeled by an admissible fuzzy tension in the fail-safe network $N=(G, \alpha, \beta)$.

DEFINITIONS OF FUZZY TENSIONS AND POTENTIALS

Let $N=(G, \alpha, \beta)$ be a fuzzy network. A mapping $t: EXU \rightarrow [0,1]$ satisfying fuzzy Kirchhoff's voltage law $FKVL; \forall e \in L^+ t(e) = \forall e \in L^- t(e)$

on every circuit $L=L^+ \cup L^-$ of G is said a fuzzy tension on G. Furthermore it is called admissible on N if the admissibility $\alpha(e) \leq t(e) \leq \beta(e)$ holds on every e in E. Here U is some set of interests (finite or infinite, such as teaching item or failure cause). α and β are mapping: $EXU \rightarrow [0,1]$ and $\alpha(e), \beta(e), t(e)$ are mappings: $U \rightarrow [0,1]$, often called fuzzy sets.

A mapping $\pi: VXU \rightarrow [0,1]$ is called a fuzzy potential on G if it satisfies the monotonicity $\pi(x) \leq \pi(y)$ for all $e=(x,y)$ in E and is said admissible on N if Admissibility: $\alpha(e) \vee \pi(x) \leq \pi(y) \leq \beta(e) \vee \pi(x)$

holds on every $e=(x,y)$ in E.

We assume the following operations on fuzzy sets A, B, C

$$1^\circ A \leq B \text{ iff } A(u) \leq B(u)$$

$$2^\circ A \vee B = C, \quad C(u) = \max(A(u), B(u))$$

$$3^\circ A \wedge B = C, \quad C(u) = \min(A(u), B(u))$$

$$4^\circ A \sim B = C, \quad C(u) = \begin{cases} A(u) & \text{if } A(u) > B(u) \\ 0 & \text{otherwise} \end{cases}$$

$$5^\circ \theta \text{ is the minimum fuzzy set, } \theta(u) = 0 \text{ and } I \text{ is the maximum fuzzy set, } I(u) = 1$$

for all u in U.

The ordinary set is a special case of the fuzzy set. That is, mapping $A:U \rightarrow \{0,1\}$ is a characteristic function of subset A of U where $A(u)=1$ if u is in A and $A(u)=0$ if otherwise. We should note that our operations on fuzzy sets are natural extensions of the set theoretic operations $\subseteq, \cup, \cap, -$ and that θ corresponds to the empty set and I to the universal set U. Although discussion and theorems are described in terms of fuzzy sets, they are completely valid for the ordinary set.

ALGEBRAIC PROPERTIES OF FUZZY TENSIONS

The edge set of a circuit L, closed edge sequence J, cutset K, and cut C generated by node set W is decomposed into the forward edge set (+) and backward edge set (-).

$$L = L^+ \cup L^-, \quad J = J^+ \cup J^-$$

$$K = K^+ \cup K^-, \quad C = (W, \bar{W})^+ \cup (\bar{W}, W)^-$$

Here (W, \bar{W}) is the set of edges $e=(x,y)$, x in W and y in \bar{W} . When $L=J=K=(\bar{W}, W)=\emptyset$, we use adjective "directed" and notation $\vec{L}, \vec{J}, \vec{K}, \vec{C}$.

[1] Let t, t_1, t_2 be fuzzy tensions on $G=(V,E)$.

(a) For a closed edge sequence $J=J^+ \cup J^-$

$$\forall e \in J^+ t(e) = \forall e \in J^- t(e).$$

(b) $\delta \wedge t, t_1 \vee t_2$ are also fuzzy tensions on G where δ is a fuzzy set.

(c) $t(e) = \theta$ for all edges e on a directed circuit \vec{L} .

(d) A mapping $t_k: EXU \rightarrow [0,1]$ defined by

$$t_k(e) = \begin{cases} 1 & \text{if } e \text{ is in } K \\ \theta & \text{otherwise} \end{cases}$$

becomes a fuzzy tension on G if K is a directed cutset $\vec{K} = K^+ \cup \emptyset$.

(e) For every e_0 in E, the following identity holds

$$t(e_0) = \bigvee_{\vec{K} \in \vec{K}_{e_0}} \bigwedge_{e \in \vec{K}} t(e)$$

where \vec{K}_{e_0} is the class of all directed cutsets containing e_0 . More precisely for each u_* in U there exists a directed cutset \vec{K}_{u_*} containing e_0 such that $t(e_0, u_*) \leq t(e, u_*)$ for all e in \vec{K}_{u_*} .

Proofs are straight forward but tedious and hence omitted.

[2] A mapping $t: EXU \rightarrow [0,1]$ is a fuzzy tension on $G=(V,E)$ iff it possesses the following decomposition.

$$t = \bigvee_{\vec{K} \in \vec{K}} [\delta_{\vec{K}} \wedge t_{\vec{K}}]$$

where \vec{K} is the family of all directed cutsets of G, $t_{\vec{K}}$ is the tension defined in (d) of [1], and $\delta_{\vec{K}}$ is any fuzzy set.

[proof] The "if" part is obvious from properties in [1]. To prove the "only if" part, define a mapping g by

$$g = \bigvee_{e \in E} \bigvee_{\vec{K} \in \vec{K}_e} [\delta_{\vec{K}} \wedge t_{\vec{K}}]$$

$$\delta_{\vec{K}} = \bigwedge_{e \in \vec{K}} t(e).$$

Then we have

$$g(e_0) = \bigvee_{e \in E} \bigvee_{\vec{K} \in \vec{K}_e} [\delta_{\vec{K}} \wedge t_{\vec{K}}(e_0)]$$

$$\begin{aligned}
&= \bigvee_{\vec{K} \in \vec{K}_0} \delta_{\vec{K}} \\
&= \bigvee_{\vec{K} \in \vec{K}_0} \bigwedge_{e \in \vec{K}} t(e) \\
&= t(e_0)
\end{aligned}$$

The last equality follows from (e) of [1].
QED

[3] < Construction of An Admissible Tension >

- 1° Start from any admissible tension t , say $t = \theta$.
- 2° Find edge e_0 satisfying $\alpha(e_0) \sim t(e_0) \neq \theta$. If none t is admissible and we are through.
- 3° Find a directed cutset \vec{K} containing $e_0 = (\bar{z}, z)$ whose increment is nonzero

$$\epsilon_{\vec{K}} = \alpha(e_0) \wedge \left[\bigwedge_{e \in \vec{K} - e_0} \beta(e) \right] \sim t(e_0) \neq \theta$$

by the following procedure.

- (a) Label node \bar{z} with mark (z).
- (b) Take any labeled node x and scan for unlabeled adjacent node y connected through e . If e is directed from y to x , or if e is directed from x to y and $\alpha(e_0) \sim \beta(e) \neq \theta$, then label node y with mark (x).
- (c) Let W be the set of labeled nodes. Then $\vec{K} = (W, \bar{W}) \cup \phi^-$ is the desired directed cutset.

- 4° Modify the tension

$$t \leftarrow t \vee [\epsilon_{\vec{K}} \wedge t_{\vec{K}}]$$

- 5° Return to 3° if $\alpha(e_0) \sim t(e_0) \neq \theta$ still holds. Else return to 2°.

We note that i) t never exceeds β , ii) $t(e_0, u)$ increases strictly for some u in U at each iteration, and iii) the same directed cutset is never used more than once for each e_0 . Hence the process is finite if fuzzy set operations \vee, \wedge, \sim are finite processes. The validity of the algorithm is proved in the next theorem.

[4] An admissible tension exists in $N=(G, \alpha, \beta)$ iff for every circuit $L=L^+ \cup L^-$ the following consistency condition holds

$$\begin{aligned}
\bigvee_{e \in L^-} \alpha(e) &\leq \bigvee_{e \in L^+} \beta(e) \\
\bigvee_{e \in L^+} \alpha(e) &\leq \bigvee_{e \in L^-} \beta(e)
\end{aligned}$$

Under this condition the algorithm [3] yields an admissible tension on N .

[proof] The "only if" part. Let t be an admissible tension on N . Combining admissibility and FKVL, we easily obtain

$$\bigvee_{e \in L^-} \alpha(e) \leq \bigvee_{e \in L^-} t(e) = \bigvee_{e \in L^+} t(e) \leq \bigvee_{e \in L^+} \beta(e)$$

as was to be proved.

The "if" part. We need only to show that under the stated condition the labeling procedure of 3° always yields a valid cutset $\vec{K} = (W, \bar{W}) \cup \phi^-$ so long as $\alpha(e_0) \sim t(e_0) \neq \theta$. This is equivalent to a fact that node z is not labeled, i.e. z not in W . Suppose otherwise. We trace the node mark one by one backward and find a circuit $L_0 = L_0^+ \cup L_0^-$ such that $e_0 \in L_0^+$, $\alpha(e_0) \sim \beta(e) \neq \theta$ for all e in L_0^- . Hence

$$\left[\bigvee_{e \in L_0^-} \alpha(e) \right] \sim \left[\bigvee_{e \in L_0^+} \beta(e) \right] \neq \theta$$

holds but this contradicts to the first consistency condition of the theorem. QED

MAX-PRESSURE MIN-DISTANCE THEOREM

[5] Admissible tension \hat{t} is said maximum on $e_0 = (\bar{z}, z)$ if all admissible t satisfy $t(e_0) \leq \hat{t}(e_0)$.

\hat{t} is obtained from any admissible t by successive modification $t \leftarrow t \vee [\epsilon_{\vec{K}} \wedge t_{\vec{K}}]$

$$\epsilon_{\vec{K}} = \left[\bigwedge_{e \in \vec{K}} \beta(e) \right] \sim t(e_0) \neq \theta$$

until $\epsilon_{\vec{K}} = \theta$ for all directed cutsets \vec{K} containing e_0 . Moreover

$$\text{Max } t(e_0) = \hat{t}(e_0) = \bigvee_{\vec{K} \in \vec{K}_0} \left[\bigwedge_{e \in \vec{K}} \beta(e) \right]$$

where \vec{K}_0 is the family of all directed cutsets containing e_0 .

The proof is obvious from the previous algorithm.

A $x \rightarrow y$ two terminal tension t is a restriction of a tension t^* of $N^* = (G^*, \alpha^*, \beta^*)$ onto $N = (G, \alpha, \beta)$ where N^* is an expansion of N by adding the terminal edge $\bar{e} = (x, y)$ with

$$\begin{aligned}
\alpha^*(e) &= \begin{cases} \alpha(e) & \text{if } e \text{ is in } E \\ \theta & \text{if } e = \bar{e} \end{cases} \\
\beta^*(e) &= \begin{cases} \beta(e) & \text{if } e \text{ is in } E \\ I & \text{if } e = \bar{e} \end{cases}
\end{aligned}$$

The value $t^*(\bar{e})$ is called $x \rightarrow y$ pressure $p(x, y)$ from x to y . The maximum pressure is denoted by $\hat{p}(x, y)$.

[6] (Max-pressure Min-distance Theorem) The max pressure $\hat{p}(x, y)$ of the network $N = (G, \alpha, \beta)$ is given by

$$\begin{aligned}
\hat{p}(x, y) &= \bigvee_{\vec{K} \in \vec{K}_{xy}} \left[\bigwedge_{e \in \vec{K}} \beta(e) \right] : \text{primal form} \\
&= \bigwedge_{Q \in Q_{xy}} \left[\bigvee_{e \in Q} \beta(e) \right] : \text{dual form}
\end{aligned}$$

where \vec{K}_{xy} is the class of all $x \rightarrow y$ directed cutsets $\vec{K} = \vec{K}^+ \cup \phi^-$ and Q_{xy} is the class of all $x \rightarrow y$ paths $Q = Q^+ \cup \bar{Q}$.

[proof] First we observe two points.

- i) It suffices to prove a scalar identity

$$\bigvee_{\vec{K} \in \vec{K}_{xy}} \left[\bigwedge_{e \in \vec{K}} \beta(e, u) \right] = \bigwedge_{Q \in Q_{xy}} \left[\bigvee_{e \in Q} \beta(e, u) \right]$$

for any u in U .

- ii) For any pair \vec{K} and Q from \vec{K}_{xy} and Q_{xy} , the intersection $\vec{K} \cap Q^+$ is not empty.

Hence taking a particular e_0 in $\vec{K} \cap Q^+$, we have

$$\bigwedge_{e \in \vec{K}} \beta(e, u) \leq \beta(e_0, u) \leq \bigvee_{e \in Q^+} \beta(e, u)$$

which implies

$$\bigvee_{\vec{K} \in \vec{K}_{xy}} \left[\bigwedge_{e \in \vec{K}} \beta(e, u) \right] \leq \bigwedge_{Q \in Q_{xy}} \left[\bigvee_{e \in Q^+} \beta(e, u) \right]$$

To prove the reverse inequality, define

$$F_Q = \left\{ e : \beta(e, u) = \bigvee_{e \in Q^+} \beta(e, u), Q = Q^+ \cup \bar{Q} \text{ in } Q_{xy} \right\}$$

Then we claim that there exists \vec{K}_0 in \vec{K}_{xy} wholly contained in F_Q . To prove this assertion, we suppose otherwise and lead to contradiction. That is, assume for each \vec{K} , $\vec{K} - F_Q$ is not empty. Let $B = \bigcup_{\vec{K} \in \vec{K}_{xy}} [\vec{K} - F_Q]$.

We proceed the following labeling operation.

- (1) Label node x with mark (*).
- (2) Take any labeled node w and scan adjacent unlabeled node z connected through e .
 - i) If e is directed from z to w , or
 - ii) if e is directed from w to z and e is in B ,
then label node z with mark (w).

We assert node y becomes labeled (if not, let X be the set of labeled nodes. Then cutset generated by $X, K = (X, \bar{X}) \cup (\bar{X}, X)$ satisfies

$$(\bar{X}, X) = \theta, (X, \bar{X}) \cap B = \theta.$$

This means K is a directed cutset wholly contained in F_Q , contradiction to the hypothesis). Backtracking the node label sequentially from y , we are able to trace $x \rightarrow y$ path $Q_0 = Q_0^+ \cup \bar{Q}_0$ with a property that $Q_0^+ \cap F_Q = \theta$. This is a contradiction to the fact that F_Q has at least one edge from every Q .

Hence we have established existence of $\vec{K}_0 \subset F_Q$. From this

- (1) $\bigwedge_{Q \in Q_{xy}} \bigvee_{e \in Q} \beta(e, u) = \bigwedge_{e \in F_Q} \beta(e, u)$
- (2) $\bigvee_{\bar{K} \in \bar{K}_{xy}} \bigwedge_{e \in \bar{K}} \beta(e, u) \geq \bigwedge_{e \in \bar{K}_0} \beta(e, u)$
- (3) $\bigwedge_{e \in \bar{K}_0} \beta(e, u) \geq \bigwedge_{e \in F_Q} \beta(e, u)$.

Combination of (1), (2), (3) yields the desired inequality, as was to be proved. QED

[7] The maximum pressure $\hat{p}(x, y)$ satisfies

- (1) $\hat{p}(x, z) \leq \hat{p}(x, y) \vee \hat{p}(y, z)$
- (2) $\hat{p}(x, z) = \{ \bigwedge_{y \in \Gamma^+(z)} [\hat{p}(x, y) \vee \beta(y, z)] \} \wedge \{ \bigwedge_{y \in \Gamma^+(z)} \hat{p}(x, y) \}$

where $\Gamma^+(z)$ is the set of immediate successor(+), predecessor(-) nodes of z.

PROPERTIES OF FUZZY POTENTIALS

[8] Let $\bar{K} = (W, \bar{W}) \cup \emptyset$ be a directed cutset generated by W. Then a mapping $\pi_W: V \times U \rightarrow [0, 1]$ defined by

$$\pi_W(x) = \begin{cases} \theta & \text{if } x \text{ is in } W \\ I & \text{otherwise} \end{cases}$$

is a fuzzy potential on $G = (V, E)$.

[proof] If $e = (x, y)$ is not in \bar{K} , then $\pi(x) = \pi(y) = \theta$ or I depending on whether x and y are both in W or \bar{W} . If e is in \bar{K} , $\pi(x) = \theta < I = \pi(y)$. Since K is a directed cutset, no possibility of x in \bar{W} and y in W occurs. Hence the monotonicity holds. QED

[9] A mapping $\pi: V \times U \rightarrow [0, 1]$ is a fuzzy potential on $G = (V, E)$ iff it possesses the following decomposition

$$\pi = \bigvee_{W \in \bar{W}} [\delta_W \wedge \pi_W]$$

where \bar{W} is a collection of node sets W producing directed cutsets, $(\bar{W}, W) = \emptyset$.

[proof] The "if" part is obvious.

Since π assumes the same value for nodes in the same strongly connected component, we may assume the graph acyclic without loss of generality. Let x be any node and Y_x be a set of nodes not reachable from x by directed paths. Define mapping g by

$$g = \bigvee_{x \in V} [\delta_x \wedge \pi_{Y_x}], \quad \delta_x = \pi(x).$$

Let us examine the value g(v) at node v.

$$g(v) = \bigvee_{x \in V} [\delta_x \wedge \pi_{Y_x}(v)]$$

$$= \bigvee_{x \in V, v \notin Y_x} \delta_x$$

$$= \bigvee_{x \in V} [\pi(x) : \text{there is } x \rightarrow v \text{ directed path}].$$

Since the monotonicity of π is transitive, existence of $x \rightarrow v$ directed path implies $\pi(x) \leq \pi(v)$,

$$= \pi(v).$$

Hence mapping g is exactly the desired decomposition. QED

[10] Let $G = (V, E)$ possess a single source block containing node z. If t is a fuzzy tension on G, then mapping π defined by

$$\pi(z) = \theta, \quad \pi(x) = \bigvee_{e \in \bar{Q}} t(e)$$

becomes a potential of G where \bar{Q} is any $z \rightarrow x$ directed path. Conversely if π is a fuzzy potential of G, then mapping t defined by

$$t(e) = \pi(y) \sim \pi(x), \quad e = (x, y) \text{ in } E$$

becomes a fuzzy tension on G.

[proof] The first half: π is well defined. That is the value of π does not depend on selection of $z \rightarrow x$ path \bar{Q} . For if \bar{Q}_1, \bar{Q}_2 are two $z \rightarrow x$ directed paths, then $L = \bar{Q}_1 \cdot \bar{Q}_2^{-1}$ is a closed edge sequence where \bar{Q}_2^{-1} is the reverse of \bar{Q}_2 . Here \bar{Q}_1 becomes the forward edge set and \bar{Q}_2 becomes the backward edge set of L. By FKVL, we have

$$\bigvee_{e \in \bar{Q}_1} t(e) = \bigvee_{e \in \bar{Q}_2} t(e)$$

as was to be proved. Note that concatenation of $e = (x, y)$ in E to the end of $z \rightarrow x$ directed edge sequence \bar{Q} produces $z \rightarrow y$ directed edge sequence $\bar{Q} \cdot e$. The monotonicity is verified by

$$\begin{aligned} \pi(x) = \bigvee_{a \in \bar{Q}} t(a) &\leq [\bigvee_{a \in \bar{Q}} t(a)] \vee t(e) \\ &= \bigvee_{a \in \bar{Q} \cdot e} t(a) = \pi(y). \end{aligned}$$

The second half:

Let $L = \bar{L} \cup \bar{L}$ be any circuit of G. Then L is consisted of the following directed paths.

- $x_0 \rightarrow x_1$ directed path Q_0 .
- $x_1 \leftarrow x_2$ directed path Q_1

⋮

- $x_{2k-1} \leftarrow x_k$ directed path Q_{2k-1}

where $\bar{L} = \bigvee_{i=\text{even}} Q_i, \bar{L} = \bigvee_{i=\text{odd}} Q_i$.

We calculate

$$\begin{aligned} \bigvee_{e \in \bar{L}} t(e) &= \bigvee_{i=\text{even}} \bigvee_{e \in Q_i} [\pi(y) \sim \pi(x)] \\ &= \bigvee_{i=\text{even}} [\pi(x_{i+1}) \sim \pi(x_i)] \end{aligned}$$

where we use a simple identity for a nondecreasing fuzzy set sequence $A_0 \leq A_1 \leq A_2$

$$(A_2 \sim A_1) \vee (A_1 \sim A_0) = A_2 \sim A_1.$$

Similarly

$$\begin{aligned} \bigvee_{e \in \bar{L}} t(e) &= \bigvee_{i=\text{odd}} \bigvee_{e \in Q_i} [\pi(y) \sim \pi(x)] \\ &= \bigvee_{i=\text{odd}} [\pi(x_i) \sim \pi(x_{i+1})]. \end{aligned}$$

Note that

$$\pi(x_{i-1}), \pi(x_{i+1}) \leq \pi(x_i)$$

holds for odd i and hence the next lemma can be applied to conclude FKVL. QED

[11] Let A_i, a_i ($i=0, 1, 2, \dots, k-1$) be two sequences of fuzzy sets satisfying

$$a_i, a_{i+1} \leq A_i \quad (i \text{ modulo } k)$$

Then identity

$$\bigvee_{i=0}^{k-1} [A_i \sim a_i] = \bigvee_{i=0}^{k-1} [A_i \sim a_{i+1}]$$

holds

The proof is omitted due to space limitation.

CONCLUSIONS

We have introduced a new concept of fuzzy tensions in a network as a mathematical tool of modeling well-coordinated curriculum or reliability assignment, and investigated its theoretical implications. Concrete applications to network problems are yet to be followed.

A dual of the fuzzy tension is the fuzzy flow upon which we have made some preliminary investigation[1]. The boolean flow is easily extended into the fuzzy flow.

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TECHNICAL BIOGRAPHY - T. MURATA (S'63 - M'67 - SM'77)

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RELEVANCE OF NETWORK THEORY TO MODELS OF
DISTRIBUTED/PARALLEL PROCESSING*

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ABSTRACT

This paper is concerned with the applicability of network theory to those aspects of distributed/parallel processing that can be modeled by marked graphs. First, several examples are given to illustrate that a wide variety of computation schemes can be modeled by marked graphs. Subsequently, the following topics are discussed: application of KVL to fault detection and isolation; KCL and Tellegen's Theorem applied to marked graphs; and the relationship between the maximum (minimum) storage requirement and the minimum (maximum) power.

I. INTRODUCTION

There is a similarity between distributed computing systems and electrical networks: both are physically and functionally interconnected systems with many components or resources interacting each other. There is also a contrasting difference between them: distributed computing is a young and more complicated field, whereas network theory is a comparatively mature field. Little formalism and few fundamental principles have emerged in the former, whereas highly developed techniques are available in the latter.

The purpose of this paper is to examine whether there are techniques of network theory that may be applicable to distributed/parallel processing. It goes without saying that network theoretic approaches alone are far from being sufficient for describing the complex behaviors of distributed/parallel processing. However, in view of the lack of a sound framework for distributed computing, it is worthwhile to search for methodologies which permit the use of results from a well-developed field such as network theory.

As the widespread interest in distributed computing has developed recently, there has been growing evidence in the literature that network theory is relevant to certain models of distributed/parallel processing. For example, it has been shown that an analogue of "Norton's theorem" is useful for analyzing queuing network models of multiprogrammed parallel processing [1,2]. For the control model of distributed processing proposed in [3], the max-flow min-cut theorem in network flow theory is used to minimize the sum of execution and inter-

process communication costs for a group of distributed program modules. The flowgraph model discussed in [4] is analogous to resistive networks, where analogies are drawn between resistance and the execution time of a program segment, and between current and the execution frequency of a program segment.

In the present paper, our discussion will be focused on the applicability of network theory to those aspects of distributed/parallel processing that can be modeled by marked graphs [5,6]. Section II provides several examples to illustrate that a wide variety of computation schemes can be modeled by marked graphs. Subsequently, the following topics are discussed: application of KVL to fault detection and isolation in Section III; KCL and Tellegen's theorem applied to marked graphs in Section IV; and the relationship between the maximum (minimum) storage requirement and the minimum (maximum) power in Section V.

II. COMPUTATION MODELS USING MARKED GRAPHS

In this section, several examples are given to illustrate that a wide variety of computation schemes can be modeled by marked graphs. Most of these examples appeared in the literature as Petri net models, but they possess the structure of marked graphs. To save space, it is assumed that the reader has some knowledge of Petri nets [7]. Marked graphs are a subclass of Petri nets, where each place has exactly one incoming arc and exactly one outgoing arc. Thus, signals or data passing through each arc come from a predetermined source (the initial node), and are sent to a predetermined destination (the terminal node). In this sense, marked graphs can model only decision-free and deterministic systems. More general Petri nets have greater modeling power (up to the power of Turing machine if the "zero testing" capability is added [8]), but their analysis tends to be computationally intractable if not undecidable. Since the emphasis of this paper is not on modeling itself but on those aspects which are relevant to network theory, we have chosen the marked graph model.

For distributed computing, it is necessary to communicate among many processes or processors. Communication protocols are used to initiate communications. The marked graph shown in Fig. 1 models a communication protocol between two processes A and B, and has been discussed, for example, in [9,10]. Each arc of this graph is labeled by a statement indicating a condition which holds while a token resides on it. For example, the token

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distribution in Fig. 1 indicates that process A is ready to send a message and that process B is ready to receive a message. After process A has sent a message (firing node 1), process B receives that message (firing node 2). At this time, there will be a token on the "wait for acknowledgement" arc and a token on the "message received" arc. The reader may easily follow the rest of token movements and the corresponding changes in conditions.

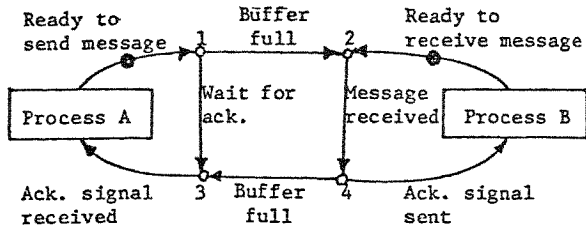


Fig. 1 A communication protocol

The second example is an n-stage pipelined operation shown in Fig. 2, where n stages of a computation can be performed concurrently as long as there is a steady stream of data coming from the input queue and taken out from the output queue.

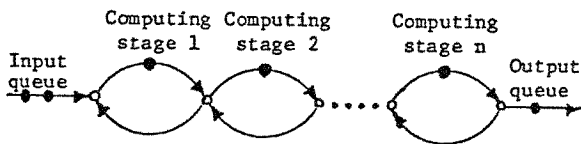


Fig. 2 N-stage pipelined operation

Note that two successive stages in Fig. 2 could be modeled in more detail by a marked graph similar to the one shown in Fig. 1, in order to show explicitly that each pair of successive processors communicates through ready and acknowledgement signals.

Parallelism is another important consideration in distributed computing. Fig. 3 illustrates the marked graph representation for the parallel activities between central processing (CP) and disc or I/O jobs as discussed in [11].

Data-flow or data-driven computations [12,13,14] are newly emerging concepts in computer architectures and languages. These computations exhibit a very high degree of concurrency since each program segment or elementary operation may be executed as soon as its input operands are present. Fig. 4 illustrates the main idea of a data-flow computation using a marked graph model, where each arc represents a first-in first-out data queue and each node a program segment performing the operation indicated in a circle. A sequence of data-flow snapshots are shown in Fig. 4(a), (b) and (c), where program segments f and g are executed concurrently between time t_0 and t_1 , and segments f,g,y, and p are executed concurrently between time t_1 and t_2 while data items a_3, b_3, c_3 , and d_3 arrive on the respective queues.

Another example of a computation scheme that can be modeled by marked graphs is the chaining operations in the GRAY-1 computer as pointed out

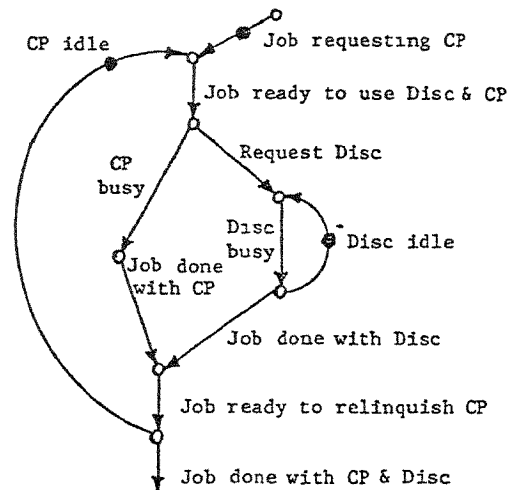


Fig. 3 Parallel CP and Disc activities

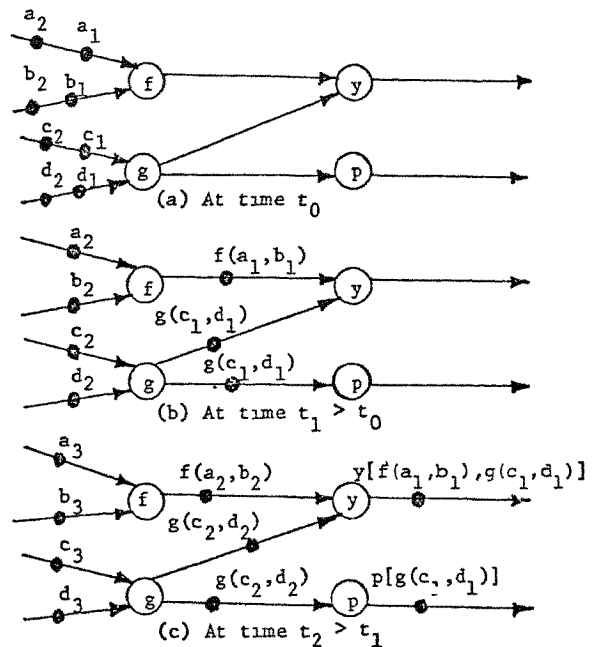


Fig. 4 Snapshots of a data flow computation

in [10].

Finally, it should be noted that marked graphs can be used for representing iterative numerical algorithms such as the parallel predictor-corrector algorithm for solving a class of non-linear differential equations [15].

III. FAULT DETECTION AND ISOLATION BY KVL

Throughout the paper, we assume that a marked graph G has t nodes and p arcs. Let $A = [a_{ij}]$ be the $t \times p$ incidence matrix of G , where $a_{ij} = 1$ (-1) if arc j is an outgoing (incoming) arc of node i , and $a_{ij} = 0$ otherwise. Let M_k be the $p \times 1$ marking

vector whose j th entry is the number of tokens on arc j at some stage (or time) k . When node i fires (execute an operation) once, one token is removed from each incoming arc j of node i , and one token is added to each outgoing arc j of node i . Thus, the firing of node i changes a marking vector M_0 to $M_1 = M_0 + A_i^T$, where A_i^T is the transpose (column vector) of the i th row of A . After node i fires v_i times for $i = 1, 2, \dots, t$, a marking vector M_0 changes to

$$M_k = M_0 + A^T V_k \quad (1)$$

where $V_k = [v_i]$ is a $t \times 1$ firing count vector and A^T is the transpose of A .

Eq. (1) can be written as

$$\Delta M = A^T V_k, \quad (2)$$

where $\Delta M = M_k - M_0$. When ΔM and V_k are interpreted, respectively, as the branch and node voltage vectors for an electrical network, (2) expresses the branch voltages ΔM in terms of the node voltages V_k . Thus (2) is equivalent to Kirchoff's voltage law (KVL) given by

$$B_f \Delta M = 0, \quad (3)$$

where B_f denotes a fundamental circuit matrix. It has been shown in [6] that (3) is a necessary and sufficient condition for reaching a marking M_k from an initial marking M_0 .

The KVL equations (2) or (3) can be used for fault detection and isolation as follows:

- 1) Store the initial marking M_0 and the incidence matrix A of a given marked graph model.
- 2) At each stage (or time) k , form $V_k = [v_i]$, where v_i is the number of times node i has fired for $i = 1, 2, \dots, t$.
- 3) At each stage (or time) k , form $M_k = [m_j]$, where m_j is the number of tokens on arc j for $j = 1, 2, \dots, p$.
- 4) Compute $\Delta X = M_k - M_0 - A^T V_k$, or $\Delta Y = B_f (M_k - M_0)$.
- 5) If the j th entry of ΔX is different from zero, then a subsystem involving arc j is at fault. If the q th entry of ΔY is different from zero, then there is a fault in a subsystem involving the q th fundamental circuit.

When it is known a priori that a given system has certain operations which will not be executed for a particular task, the initial marking M_0 need not be live and there may be token-free directed circuits [6]. Thus, for fault analysis, the marked graph can be reduced by coalescing each token-free directed circuit to a single node.

Example 1: The marking M_0' of the marked graph in Fig. 5(a) is not live, so the token-free directed circuit (e,f) can be reduced to a single node denoted by 1 as is shown in Fig. 5(b). Let M_0 , M_1 , and M_2 be the marking vectors of Fig. 5(b), 1(c), and 2(d), respectively. Suppose that after executing the operations represented by node 2 twice and node 3 once, the marking M_0 changes to M_1 . Then

$$\Delta X = M_1 - M_0 - A^T V_k$$

$$= \begin{matrix} a \\ b \\ c \\ d \end{matrix} \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \end{bmatrix} - \begin{matrix} 2 \\ 0 \\ 1 \\ 1 \end{matrix} \begin{bmatrix} 2 \\ 0 \\ -1 \\ 1 \end{bmatrix} - \begin{matrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 0 & -1 & 1 \\ 1 & 0 & -1 \end{matrix} \begin{bmatrix} 0 \\ 2 \\ 1 \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

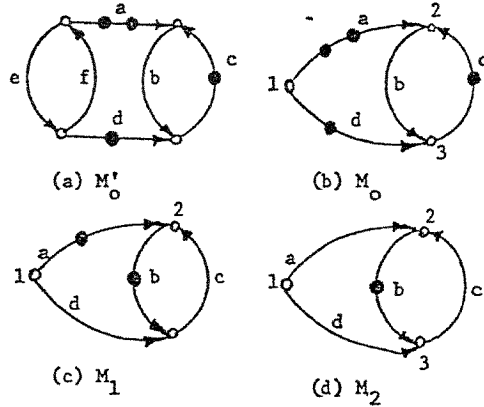


Fig. 5 Example 1

The entry of ΔX corresponding to arc a is not zero, which indicates that a subsystem involving arc a is at fault. Also, with respect to a tree (c,d), we have:

$$\begin{aligned} \Delta Y &= B_f (M_1 - M_0) \\ &= \begin{matrix} a & b & c & d \end{matrix} \begin{bmatrix} 1 & 0 & -1 & -1 \\ 0 & 1 & 1 & 0 \end{bmatrix} \left\{ \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \end{bmatrix} - \begin{bmatrix} 2 \\ 0 \\ 1 \\ 1 \end{bmatrix} \right\} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \end{aligned}$$

which indicates a fault in the fundamental circuit (a,c,d). For $V_k = [0 \ 2 \ 1]^T$, the correct marking reachable from M_0 is shown in Fig. 5(d). The reader can easily verify, in this case, that

$$\begin{aligned} \Delta X &= M_2 - M_0 - A^T V_k = 0 \\ \text{and } \Delta Y &= B_f (M_2 - M_0) = 0. \end{aligned}$$

IV. INVARIANT, KCL, AND TELLEGEN'S THEOREM

Let I be a $p \times 1$ vector satisfying

$$AI = 0, \quad (4)$$

where A is the $t \times p$ incidence matrix of a marked graph G . Due to the invariant property expressed by (5) below, I is called an invariant of G . If I is interpreted as the branch current vector, (4) represents Kirchoff's current law (KCL) in an electrical network whose incidence matrix is A .

From (2) and (4), we obtain

$$\Delta M^T I = V_k^T (AI) = 0 \quad (5)$$

$$\text{or } M_0^T I = M_k^T I. \quad (6)$$

Eq. (6) states that the inner product of vectors M_0 and I is equal to that of M_k and I , for any two mutually reachable (live) markings M_0 and M_k . In other words, the weighted sum of tokens for M_0 is the same as that for M_k , where the weight of each arc is defined by the corresponding entry of I . Eq. (5) or (6) can also be used for detecting faults, but not for isolating them since (5) or (6) yields a scalar quantity.

It should be noted that (5) is analogous to Tellegen's theorem in the following sense: the inner product of the branch voltage vector ΔM and the branch current vector I is equal to zero. Just as in electrical networks, the relation $\Delta M^T I = 0$ holds even if ΔM is taken from one marked graph and I from another, as long as both have the same incidence matrix. Since Tellegen's theorem is very useful for computer aided network design [16], and is applicable in many areas of electrical engineering [17], it can be expected that this theorem or its analogue may become equally useful for the analysis of distributed/parallel systems.

Example 2: For the marked graph shown in Fig. 5(b) and (d), $I = [1 \ 3 \ 2 \ -1]^T$ is an invariant since

$$AI = \begin{bmatrix} a & b & c & d \\ 1 & 0 & 0 & 1 \\ -1 & 1 & -1 & 0 \\ 0 & -1 & 1 & -1 \end{bmatrix} \begin{bmatrix} 1 \\ 3 \\ 2 \\ -1 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}$$

For the two mutually reachable markings M_0 and M_2 shown in Fig. 5(b) and (d) (M_2 reaches M_0 by firing node 1 twice and node 3 once), (6) is easily verified as follows:

$$M_0^T I = [2 \ 0 \ 1 \ 1] * [1 \ 3 \ 2 \ -1] = 3$$

$$M_2^T I = [0 \ 1 \ 0 \ 0] * [1 \ 3 \ 2 \ -1] = 3$$

where * denotes the inner product.

V. MAXIMUM STORAGE REQUIREMENT AND MINIMUM POWER

Let $R(M_0)$ denote the set of all possible markings reachable from M_0 , and $|M|$ denote the total number of tokens in a marked graph for a marking M . For a marked graph G with a bounded initial marking M_0 , it is known that $|M|$ is bounded for any M in $R(M_0)$ if and only if the underlying digraph of G is strongly connected. In this section, we are interested in the problems of finding the maximum and minimum values of $|M|$ for all M in $R(M_0)$ of a strongly connected marked graph G . To make these problems more general, we associate a nonnegative integer-valued weight function $w(e_i)$ to each arc e_i in G . $w(e_i)$ may represent the storage space or cost to accommodate a token on arc e_i . Let W be a $p \times 1$ column vector whose i th entry is $w(e_i)$. Then, the inner product $M^T W$ denotes the total weighted cost for a marking M . In particular, $M^T W = |M|$ if $w(e_i) = 1$ for all e_i .

Given a live initial marking M_0 with weight function W for a strongly connected marked graph G , we have

$$\text{Max } \{M^T W \mid M \in R(M_0)\} = \text{Min } \{M_0^T I \mid I \geq W\}, \quad (7)$$

and

$$\text{Min } \{M^T W \mid M \in R(M_0)\} = \text{Max } \{M_0^T I \mid I \leq W\}, \quad (8)$$

where I is an invariant of G .

Eqs. (7) and (8), which specify the maximum and minimum values of $M^T W$, was originally given in [18] and can be proved by using the duality theorem in linear programming [19]. The network theoretic interpretations of these equations are as follows. When M_0 is interpreted as the branch voltage source vector, $M_0^T I$ represents the power supplied by the voltage sources. Thus, (7) (and (8)) states that given M_0 with W for a strongly connected marked graph G , the maximum (minimum) total cost or storage space required is equal to the minimum (maximum) power supplied to G by a current distribution I such that $I \geq W$ ($I \leq W$).

Example 3: Consider the marked graph shown in Fig. 6, where $M_0 = [1 \ 0 \ 1 \ 0 \ 0]^T$ and $W = [1 \ 2 \ 1 \ 2 \ 1]^T$. The current distribution shown by the dotted lines in Fig. 6(a) is an invariant $I_1 = [2 \ 2 \ 2 \ 2 \ 4]^T \geq W$. Thus, the maximum storage required is equal to $M_0^T I_1 = 4$, which is attained with $M = [0 \ 2 \ 0 \ 2 \ 0]^T$. The current distribution shown by the dotted lines in Fig. 6(b) is an invariant $I_2 = [0 \ 1 \ 1 \ 0 \ 1]^T \leq W$. This yields the maximum (power), $M_0^T I_2 = 1$ under the constraint $I \leq W$. Thus, the minimum storage required is equal to $M_0^T I_2 = 1$, which is attained with $M = [0 \ 0 \ 0 \ 0 \ 1]^T$.

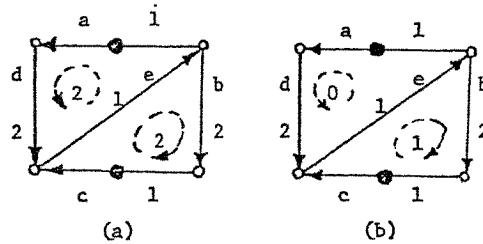


Fig. 6 Example 3

VI. CONCLUSION

We have shown that network theory is relevant to certain models of distributed/parallel processing. One notable application of the network theory as discussed in this paper is the method given in Section III for detecting and isolating faults. This method may be suitable for real-time fault analysis since it requires a very small amount of computation (essentially only one vector addition for each firing).

It is hoped that this paper motivates network theorists to investigate methods for applying their highly developed techniques to the areas of distributed/parallel processing.

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TECHNICAL BIOGRAPHY - Ruey-wen LIU

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ACCESSIBILITY OF LARGE-SCALE ELECTRONIC CIRCUITS

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ABSTRACT

The problem of fault diagnosis of large-scale analog circuit is studied. Any fault diagnosis procedure is limited by the number of circuit parameters to be diagnosed. When such limit is exceeded by large-scale circuits, some kind of tearing process has to be implemented before a fault diagnosis procedure can be applied. In this paper, a tearing process via accessibility of subnetworks is presented. The necessary and sufficient condition for accessibility is obtained. The implementation of this tearing process is discussed. The tearing process can be applied to nonlinear circuits.

I. INTRODUCTION

In the study of Large-Scale Dynamical Systems (LSDS), in order to simplify a problem we often reduce it from the level of the overall system to that of its components or subsystems. Tearing or Diakoptics [1] is such an approach for the analysis of large-scale networks. For the fault diagnosis of LSDS there is a technique which is equivalent to tearing. Existing methods of fault diagnosis (for example [3-6]) attack the problem at the LSDS level.

The easiest way to transfer the problem of fault diagnosis from the level of the overall system to that of the subsystems is to have direct access to the inputs and outputs of each subsystem. However, such direct access may not be available to us. In such a case if we can determine the inputs and outputs of the components of interest from the LSDS inputs and outputs, we have effectively accessed them. Intuitively, we can say that this would be possible if a mapping existed from the space of input-output waveforms of the LSDS to the space of input-output waveforms of the components. Such a map would be the basis of our tearing approach. In this paper, we explore these concepts and determine the necessary and sufficient conditions for the existence of such a map which takes as much advantage of the known information as possible. We then lay the intuitive basis for a strategy of tearing which simplifies the problem of fault diagnosis. The results presented are a generalization of an earlier work by Saeks, Singh and Liu [2] and Liu and Visvanathan [7].

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II. ACCESSIBILITY FROM INPUT/OUTPUT TERMINALS

The LSDS model consists of three parts, the masked subsystem, the unmasked subsystem and the connection-box as shown in Figure 1. The vectors u and y denote the input and output vectors of the LSDS, c and d of the unmasked subsystem and r and s of the masked subsystem. The connection-box consists of the connections between the above variables. The equations for the three parts are:

a) Unmasked Subsystems

We assume that the unmasked subsystem is a linear dynamical system described by:

$$\begin{aligned} \dot{x}(t) &= A x(t) + B c(t) \\ d(t) &= C x(t) + D c(t) \end{aligned} \quad (1)$$

where $A, B, C,$ and D are constant matrices and x is the state vector for the unmasked subsystem.

b) Connection Box

The connection box is described by [10]:

$$\begin{bmatrix} c \\ r \\ y \end{bmatrix} = \begin{bmatrix} L_{cd} & L_{cs} & L_{cu} \\ L_{rd} & L_{rs} & L_{ru} \\ L_{yd} & L_{ys} & L_{yu} \end{bmatrix} \begin{bmatrix} d \\ s \\ u \end{bmatrix} + \begin{bmatrix} R_{cc} & R_{cr} & R_{cy} \\ R_{rc} & R_{rr} & R_{ry} \\ R_{yc} & R_{yr} & R_{yy} \end{bmatrix} \begin{bmatrix} c \\ r \\ y \end{bmatrix} \quad (2)$$

The L 's and R 's are constant matrices. Note that d, s and u are inputs to the connection-box and c, r and y are the outputs.

c) Masked Subsystem

The inputs and outputs of the masked subsystem are related by some functional form

$$s = f \cdot r \quad (3)$$

which is assumed unknown. For example, the relation (3) could be a state equation or a zero-memory nonlinear function.

Equations (1), (2) and (3) completely describe the LSDS. The unmasked subsystem has been included in the LSDS model to provide us with a greater flexibility. Components that are known to be fault-free or have been independently diagnosed can be

included as part of the unmasked subsystem. We further assume that the LSDS is well-posed, i.e., the initial value solution $(x(t), c(t), d(t), r(t), s(t))$ exists and is unique for all admissible inputs $u(\cdot)$.

Definition 1.

The masked subsystem of the LSDS is said to be accessible from input/output terminals, or simply accessible, if $\forall t \in [0, \infty)$, $(r(t), s(t))$ can be uniquely determined from $(u(\tau), y(\tau))$ for $\tau \in [0, t]$ by use of equations (1) and (2) but not (3), with the initial state $x(0) = 0$ of the unmasked subsystem. It is said to be anticipatively accessible if $(r(t), s(t))$ can be uniquely determined from $(u(\tau), y(\tau))$ for $\tau \in [0, t + \delta]$ for some $\delta > 0$ but not for $\delta = 0$.

Theorem 1 [11]

The masked subsystem of the LSDS is accessible if and only if the matrix J

$$J = \begin{bmatrix} R_{cc} + L_{cd}D^{-1} & R_{cr} & L_{cs} \\ R_{rc} + L_{rd}D & R_{rr} - I & L_{rs} \\ R_{yc} + L_{yd}D & R_{yr} & L_{ys} \end{bmatrix}$$

has full column-rank.

Note that the accessibility only depends on the memoryless part of LSDS. The application of Theorem 1 to large-scale networks is considered next.

III. ACCESSIBILITY OF SUBNETWORKS

The above result can be applied to the diagnosis of subnetworks. A given network can be decomposed into three parts as shown in Figure 2. Those R-elements, which are known to be reliable, are placed in the resistive-network box. Those L,C-elements and/or (nonlinear) devices are placed in the masked box. The last box contains all the elements to be diagnosed.

Note that (u, y) and (r, s) are the port-voltages and the port-currents of the overall network and of the subnetworks in the masked box respectively.

The unmasked part has a state-equation representation (1),

$$\begin{aligned} \dot{x} &= Ax + Bc \\ d &= Cx \end{aligned}$$

where $A = 0$, $C = I$, and $B = \text{diag}(\frac{1}{C_i}, \frac{1}{L_j})$, $C = (i_C, v_L)$, $d = (v_C, i_L)$.

Associate each network in Figure 2, construct a LC-reduced network, or simply reduced network, by replacing each inductor by an open circuit and each capacitor by a short circuit as shown in Figure 3. Note that the reduced network is a resistive network.

Theorem 2. [11]

The masked subnetwork in Figure 2 is accessible if and only if (i_C, v_L, r, s) can be uniquely deter-

mined by (u, y) from its reduced resistive network.

IV. ACCESSIBILITY OF FURTHER REDUCED SUBNETWORK

For the purpose of testing the accessibility, it is possible to further simplify the network. In order to do this, more notations are needed. In this section, m-terminal masked box is decomposed into m-1 2-terminal X-devices and the set of X-devices-branches is denoted by G_X . Note that the knowledge of all X-devices completely describes the behavior at the terminals of the original masked box. Similarly, the set of all inductor-, capacitor-branches are denoted by G_L, G_C respectively. As for the resistor-branches, since some of them may be in a particular tree we choose in the network, we denote the set of them in the tree by G_R , and the rest in the corresponding cotree by G_C .

Now consider a network N satisfying the following assumptions.

- (1) The network N is a connected graph.
- (2) The sources, including voltmeters and ammeters, are considered as a set of branches with measurable voltages and currents. The symbol G_S is used to denote the set.
- (3) $G_S \cup G_C$ contains no loop, otherwise ammeters are inserted to break the loops.
- (4) $G_S \cup G_L$ contains no cut set.
- (5) All resistors have positive resistance.

These five conditions are assumed to be satisfied in the networks considered in this section.

Under above assumptions, there exists a tree (t) which contains (G_X, G_C, G_R) and does not contain (G_S, G_L, G_C) . Let the set of all such t be denoted by T. Then for each t in T, we have the following equations:

KCL:

$$\begin{bmatrix} I_X \\ I_C \\ I_R \end{bmatrix} = - \begin{bmatrix} F_{SX} & F_{SC} & F_{SR} \\ F_{LX} & F_{LC} & F_{LR} \\ F_{GX} & F_{GC} & F_{GR} \end{bmatrix}^T \begin{bmatrix} I_S \\ I_L \\ I_G \end{bmatrix} \quad (4a)$$

KVL:

$$\begin{bmatrix} V_S \\ V_L \\ V_G \end{bmatrix} = \begin{bmatrix} F_{SX} & F_{SC} & F_{SR} \\ F_{LX} & F_{LC} & F_{LR} \\ F_{GX} & F_{GC} & F_{GR} \end{bmatrix} \begin{bmatrix} V_X \\ V_C \\ V_R \end{bmatrix} \quad (4b)$$

Ohm's Law:

$$\begin{aligned} V_R &= R I_R \\ I_G &= G V_G \end{aligned} \quad (4c)$$

where R and G are diagonal matrices with positive

diagonal elements.

Define

$$W = \left[\begin{array}{c|c} \begin{matrix} F_{GR}^T & G & F_{GX} \\ \hline F_{SX} & & \end{matrix} & \begin{matrix} R^{-1} + F_{GR}^T & G & F_{GR} \\ \hline F_{SR} & & \end{matrix} \end{array} \right]$$

Then from Equation (4) and Theorem 2, the following lemma can be proved.

Lemma 1.

The X-devices in network N are accessible if and only if the associated matrix W has full column-rank.

Although the size of matrix W is smaller than the original matrices, that is only superficial because some of the submatrices cannot be determined without the knowledge of the original matrices. The following lemmas will provide a better solution.

Lemma 2.

In a network N, the associated matrix W has full column-rank in the generic sense [12] if the matrix F_{SX} has full column-rank.

Lemma 3.

The matrix F_{SX} of a network N has full column-rank if (1) there exists a tree $t \in T$ such that $G_R U_G S$ contains no loop in LC-reduced network of N and (2) the matrix W associated with N has full column-rank.

The second condition in Lemma 3 will be referred as Assumption (5) in the sequent paragraphs.

Note that not only the size of the matrix F_{SX} is smaller than W but also the matrix itself can be determined by the subgraph N'' constructed by shorting all resistor-branches in the particular tree and opening all resistor-branches in the corresponding cotree in the LC-reduced network N' . We call the subgraph N'' RLC-reduced network. Then Theorem 3 follows.

Theorem 3.

Let N be a network satisfying Assumptions (1) to (5), then X-devices in N are generically accessible if and only if the matrix F_{SX} in RLC-reduced network associated with t has full column-rank.

Remarks

1. Theorem 3 enables us to determine the accessibility of X-devices in a network by dealing with a considerably smaller subnetwork N'' with only sources and X-devices in this subnetwork.
2. From graph theory, F_{SX} has full column-rank if and only if G_S contains a tree in RLC-reduced network. Therefore, to achieve the accessibility of X-devices, we only need to add some voltmeter-branches into G_S to make it contain a tree in RLC-reduced network.
3. In this theory, in order to access all the X-devices in a network, the number of sources must be at least equal to the number of X-devices as can be seen from the required full column-rank of F_{SX} .
4. The choice of tree in a network is crucial in determining the minimal set of test points to obtain accessibility. Although the algorithm of

finding the tree is still under development, it is quite possible to pick the tree in a network of reasonable scale by inspection as shown in Example 1.

Example 1

Consider the accessibility of the two transistors in the two-stage amplifier circuit as shown in Fig. 4a. It is clear to see that $(C_1, T_1, C_2, T_2, C_3)$ form a loop. From Assumption (2), the loop can be broken by inserting an ammeter A in series with C_2 . Then, by choosing the tree consisting $(X_1, X_2, X_3, X_4, R_5)$ in Fig. 4b, the associated RLC-reduced network is shown in Fig. 4c. Apparently, the branches (E_1, E_2, E_3, A) contains a tree in Fig. 4c. Thus, (X_1, X_2, X_3, X_4) , so that (T_1, T_2) , are accessible after the insertion of the ammeter.

V. APPLICATION TO TEARING PROCESS

The purpose of diakoptic or tearing process [1] is to find a way of partitioning a large-scale network into smaller subnetworks so that the solution of the large-scale network can be obtained by solving the (decoupled) subnetworks. Clearly, this represents a reduction in computation time.

If fault diagnosis is of our interest instead of the network solutions, new tearing process should be developed so that it is compatible to fault diagnosis problem. The accessibility can fulfill such purpose. Let us consider the network in Figure 2. If each masked subnetwork is diagnosable from its input/output pair (r,s) and is accessible, then the entire network is diagnosable from its input/output pair (u,y) . This is because (r,s) can be obtained from (u,y) independently from the characteristics of masked subnetworks.

In summary, if accessibility is achieved, one can diagnose the entire network by diagnosing each of the (smaller and decoupled) masked subnetworks individually.

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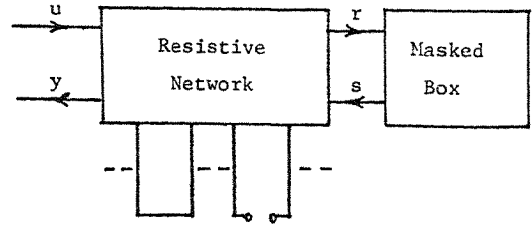


Figure 3

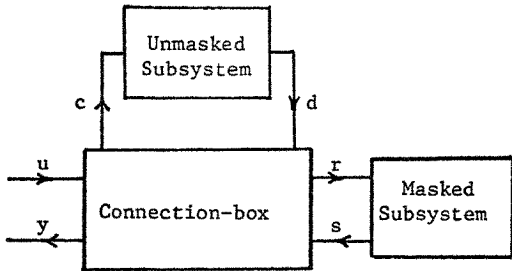


Figure 1

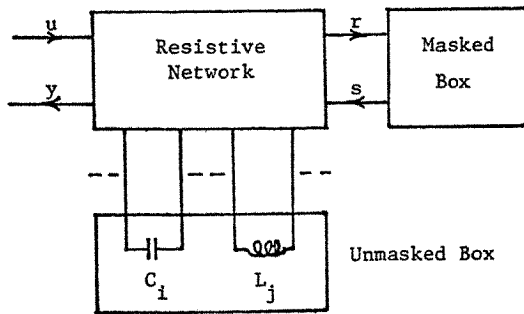


Figure 2

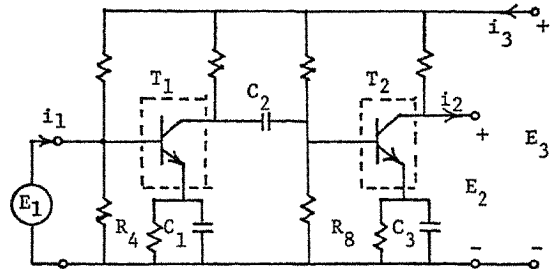


Figure 4a

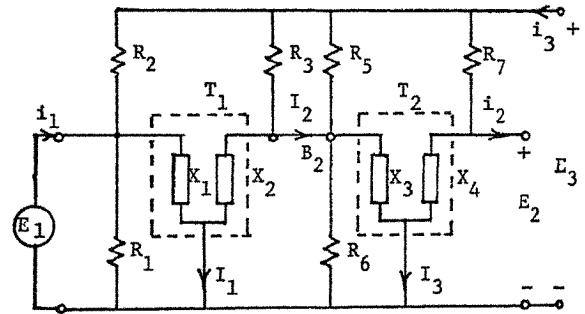


Figure 4b

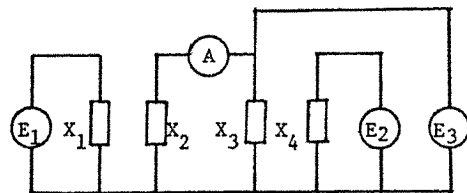


Figure 4c

TECHNICAL BIOGRAPHY - SANJIT KUMAR MITRA

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DESIGN AND IMPLEMENTATION OF HALF-PLANE TWO-DIMENSIONAL DIGITAL FILTERS

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ABSTRACT

This paper is concerned with the nonsymmetric half-plane (NSHP), recursive, two-dimensional (2-D) digital filters. Such a filter is characterized by a linear, shift-invariant (LSI), constant coefficient difference equation that is nonanticipatory in one index but is recursively computable for a fixed direction of recursion. A computer-aided iterative approach is described for the design of a stable, NSHP, 2-D digital filter approximating a specified magnitude response. This approach incorporates a nonlinear optimization procedure to converge to a (locally) optimum half-plane filter while the stability is checked at every iteration using the spectral factorization stability test of Ekstrom and Woods. A novel "penalty function" technique is used to satisfy the stability constraint. Next, the realization of a given NSHP digital transfer function using the basic building blocks (such as delay elements, advance elements, multipliers, and adders) is considered. A general technique which takes into account the restriction of a fixed direction of recursion is described.

INTRODUCTION

An LSI, 2-D digital filter operates on a 2-D input sequence $\{x(m,n)\}$ to develop a 2-D output sequence $\{y(m,n)\}$ in accordance with a linear constant-coefficient difference equation of the form

$$\sum_{k,l} b(k,l)y(m-k,n-l) = \sum_{k,l} a(k,l)x(m-k,n-l) \quad (1)$$

or equivalently, in the frequency domain by the digital transfer function $H(z_1, z_2)$ defined as

$$H(z_1, z_2) = \frac{\mathcal{Z}\{y(m,n)\}}{\mathcal{Z}\{x(m,n)\}} = \frac{\sum_{k,l} a(k,l)z_1^{-k}z_2^{-l}}{\sum_{k,l} b(k,l)z_1^{-k}z_2^{-l}} = \frac{A(z_1, z_2)}{B(z_1, z_2)} \quad (2)$$

where $\mathcal{Z}\{y(m,n)\}$ and $\mathcal{Z}\{x(m,n)\}$ denote the 2-D \mathcal{Z} -transforms of the output and the input sequences, respectively. The inverse \mathcal{Z} -transform of $H(z_1, z_2)$ is a 2-D sequence $\{h(m,n)\}$ known as the unit sample or impulse response of the 2-D filter. The output sequence can also be expressed as a convolution of the input sequence with the unit impulse response sequence

$$y(m,n) = \sum_{k=-\infty}^{\infty} \sum_{l=-\infty}^{\infty} h(k,l)x(m-k,n-l) \quad (3)$$

If the unit impulse response has nonfinite number of nonzero samples, the corresponding filter is called an infinite impulse response (IIR) 2-D digital filter. The output has then to be computed recursively from the input and a sufficient set of initial conditions by using some explicit form of (1). As a consequence this type of filter has also been called recursive. The general 2-D IIR digital filter is the so-called NSHP digital filter [1], which is nonanticipatory in only one index. But the filter algorithm is recursively computable in that it only uses output values which can be previously computed or are given as initial conditions.

HALF-PLANE DIGITAL FILTER DESIGN

Until recently, design techniques for 2-D recursive filters have emphasized the design of quarter-plane, or so-called "causal" filters with impulse response on only one quadrant. Murray [2] has recently shown, however, that the class of magnitude functions realizable by quarter-plane filters is quite restrictive. On the other hand, half-plane filters possess no such restrictions and are capable of realizing an arbitrary magnitude function. It is therefore understandable that increasing interest is being shown in design techniques for 2-D half-plane recursive filters.

One technique for designing half-plane filters via a spectral factorization procedure was proposed in [1]. That technique involved factoring the specification spectrum into its potentially infinite-order stable and unstable components and windowing the stable half-plane to finite order. Unfortunately, this technique tends to give severely suboptimal results.

A second approach to the design of half-plane recursive filters has recently been proposed by Chang and Aggarwal [3]. In their approach, an exponential weighting sequence is first applied to the autocorrelation sequence, which is the inverse Fourier transform of the specified magnitude squared function. A finite-order half-planar (or "semi-causal") form of the planar least squares inverse (PLSI) filter is then computed; a numerator polynomial is added when desired using a cepstral factorization and simple truncation. Two potential problems with this technique are 1) the resulting filter's response is in no way an optimal approximation to the desired response and 2) the half-

planar PLSI is not guaranteed to be semiminimum phase (and hence, stable) in general.

A third and evidently more powerful technique was first proposed by Twogood in [4]. This technique incorporates a nonlinear optimization procedure to converge to a (locally) optimum half-plane filter, while the stability constraint is satisfied via a "penalty function" approach which checks stability using the spectral factorization stability test of [1]. This design procedure has also been discussed in some detail in [5]. The steps of this all-pole design algorithm are shown in Fig. 1, where $b_{\oplus}(m,n)$ denotes the half-plane denominator

polynomial of the recursive filter, $B_{\oplus}(e^{j\omega_1}, e^{j\omega_2})$

is the 2-D DFT of $b_{\oplus}(m,n)$, and $|H(e^{j\omega_1}, e^{j\omega_2})|$ is the desired magnitude specification. The superscript i denotes the iteration number. Use of a modified Marquardt algorithm for the nonlinear optimization generally results in a converged solution after 5 or 10 iterations [4]. The three blocks in the center of Fig. 1 simply perform the following: the current half-plane filter $b_{\oplus}^i(m,n)$ is tested for stability; P is set to 0 if it is stable, otherwise, P is set to some large number M . The block on the right side of Fig. 1 is, of course, the computation of the magnitude squared response of the current half-plane filter and a comparison with the desired specification. Finally, the objective function to be minimized is just the sum of the magnitude errors plus the penalty function P . The algorithm is therefore simply a solution to a nonlinear optimization problem (i.e., find the half-plane filter $b_{\oplus}(m,n)$ whose magnitude response in some sense "best" approximates the given specification) with a nonlinear constraint (i.e., the constraint that $b_{\oplus}(m,n)$ is stable). The technique used is a standard one for such problems; namely, using a nonlinear optimization algorithm with a penalty function to enforce the constraint.

The design algorithm of Fig. 1 can be modified in a trivial manner to design filters with both a numerator and denominator; this only requires augmenting the $\{b(m,n)\}$, denominator coefficients being optimized with the $\{a(m,n)\}$, numerator coefficients, and computing the magnitude-squared response as $|A(e^{j\omega_1}, e^{j\omega_2})|^2 / |B_{\oplus}(e^{j\omega_1}, e^{j\omega_2})|^2$. This has been demonstrated in [6], where even better design results are achieved due to this numerator-denominator interaction. For instance, a 3×3 half-plane denominator with 4×4 numerator (41 total coefficients) has been designed in [6] using the above technique for an ideal fan filter specification. The magnitude-squared response of that filter is shown in Fig. 2. That result appears to be significantly superior to any other design result, recursive or nonrecursive, to be found in the literature, and is indicative of the power of this technique.

HALF-PLANE DIGITAL FILTER REALIZATION

A 2-D NSHP digital filter configuration can be

conveniently represented by block diagrams, the basic elements of which are: constant multipliers, multi-input adders, delay elements z_1^{-1} and z_2^{-1} , and advance elements z_1 and z_2 . Using these elements, a circuit-theoretic realization of a rational 2-D digital transfer function (with unit numerator) is outlined in this section. The aim is to obtain a single input, single output configuration with no delay-free loops which is admissible in the sense that for a fixed direction of recursion all the internal node variable values in the configuration are uniquely determined by previously computed node signal values. Consider the realization of the transfer function $H(z_1, z_2) = 1/B(z_1, z_2)$ using the configuration of Fig. 3, where

$$B(z_1, z_2) = \sum_{i=-M_b}^{-1} \sum_{j=1}^{N_b} b(i, j) z_1^{-i} z_2^{-j} + \sum_{i=0}^{M_b} \sum_{j=0}^{N_b} b(i, j) z_1^{-i} z_2^{-j}, \quad (4)$$

and $b(0,0) = 1$.

The blocks \mathcal{N}_p and \mathcal{N}_n are known LSI 1-D digital networks characterized by the transfer functions between the input and the (L_1+1) - and (K_1+1) -outputs: $g_{\ell}(z_1^{-1})$, $\ell=0,1,\dots,L_1$, and $f_k(z_1)$, $k=-K_1,\dots,0$, respectively. Likewise, the blocks \mathcal{N}'_p and \mathcal{N}'_n are known LSI 1-D digital networks characterized by the transfer functions between the (L_2+1) - and (K_2+1) -inputs and the output: $p_n(z_2^{-1})$, $n=0,1,\dots,L_2$, and $h_m(z_2^{-1})$, $m=0,1,\dots,K_2$, respectively. Thus f_k 's, g_{ℓ} 's, h_m 's, and p_n 's could all be polynomials in z_1 , z_1^{-1} , and z_2^{-1} . Note that an extra block of transfer function $z_2^{-1}z_1$ has been used preceding the \mathcal{N}_n block in order that the resulting realization be admissible. The blocks \mathcal{D}_n and \mathcal{D}_p are unknown K_1 - and (L_1+1) -input, (K_2+1) - and (L_2+1) -output networks consisting only of multipliers and adders. Let $d(q,r)$ $\{d(q,r)\}$ denote the constant transfer function between the q -th input and the r -th output of \mathcal{D}_n $\{\mathcal{D}_p\}$. Thus the realization of (4) using the configuration of Fig. 3 is equivalent to the determination of the constants $d(i,j)$ and $\tilde{d}(k,\ell)$.

Let us now assume that

$$f_k(z_1) = \sum_{\mu=0}^{M_b-1} \alpha(\mu, k) z_1^{\mu}, \quad k=-K_1, \dots, 0;$$

$$h_m(z_2^{-1}) = \sum_{\lambda=0}^{N_b-1} \beta(m, \lambda) z_2^{-\lambda}, \quad m=0, \dots, K_2;$$

$$g_{\ell}(z_1^{-1}) = \sum_{\epsilon=0}^{M_b} \gamma(\epsilon, \ell) z_1^{-\epsilon}, \quad \ell=0, \dots, L_1;$$

$$\text{and } p_n(z_2^{-1}) = \sum_{\tau=0}^{N_b} \delta(n, \tau) z_2^{-\tau}, \quad n=0, \dots, L_2.$$

Then from Fig. 3, the denominator $Q(z_1, z_2)$ of the transfer function is given by

$$1 + \sum_{i=0}^{M_b-1} \sum_{j=0}^{N_b-1} \left(\sum_{k=-K}^{K_2} \alpha(i, k) \hat{d}(k, m) \beta(m, j) \right) z_1^{i+1} z_2^{-j-1} + \sum_{i=0}^{M_b} \sum_{j=0}^{N_b} \left(\sum_{\ell=0}^{L_1} \sum_{n=0}^{L_2} \gamma(i, \ell) d(\ell, n) \delta(n, j) \right) z_1^{-i} z_2^{-j} \quad (5)$$

Comparing the coefficients of like powers of $Q(z_1, z_2)$ in (5) and $B(z_1, z_2)$ in (4) we have:

$$\underline{B}_p = \underline{\Gamma} \underline{D} \underline{\Delta} \quad \text{and} \quad \underline{B}_n = \underline{A} \hat{\underline{D}} \underline{\Lambda} \quad (6)$$

where,

$$\underline{B}_p = \begin{bmatrix} 0 & b(0,1) & \dots & b(0, N_b) \\ b(1,0) & b(1,1) & \dots & b(1, N_b) \\ \vdots & & & \vdots \\ b(M_b, 0) & & \dots & b(M_b, N_b) \end{bmatrix}$$

$$\underline{\Gamma} = [\gamma(i, j)], \quad 0 \leq i \leq M_b, \quad 0 \leq j \leq L_1$$

$$\underline{D} = [d(i, j)], \quad 0 \leq i \leq L_1, \quad 0 \leq j \leq L_2$$

$$\underline{\Delta} = [\delta(i, j)], \quad 0 \leq i \leq L_2, \quad 0 \leq j \leq N_b$$

$$\underline{B}_n = [b(i, j)], \quad -M_b \leq i \leq -1, \quad 1 \leq j \leq N_b$$

$$\underline{A} = [\alpha(i, j)], \quad -M_b \leq i \leq -1, \quad -K_1 \leq j \leq 0$$

$$\hat{\underline{D}} = [\hat{d}(i, j)], \quad -K_1 \leq i \leq 0, \quad 0 \leq j \leq K_2$$

$$\underline{\Lambda} = [\beta(i, j)], \quad 0 \leq i \leq K_2, \quad 1 \leq j \leq N_b \quad (7)$$

Determination of \underline{D} and $\hat{\underline{D}}$ from (6) can be easily done by assuming $L_1 = M_b$, $L_2 = N_b$, $K_1 = M_b - 1$, and $K_2 = N_b - 1$, and choosing \mathcal{K}_n , \mathcal{K}_p , \mathcal{H}_n , and \mathcal{H}_p such that the polynomials f_k 's (or respectively g_ℓ 's, h_m 's, p_n 's) are linearly independent of one another with respect to the basis (of polynomials) which is an appropriate subset of

$\{1, z_1, z_1^2, \dots, z_1^{(M_b-1)}\}$ (resp. $\{1, z_2^{-1}, \dots, z_2^{-(N_b-1)}\}$), $\{1, z_1^{-1}, z_1^{-2}, \dots, z_1^{-M_b}\}$, $\{1, z_2^{-1}, z_2^{-2}, \dots, z_2^{-N_b}\}$, say. In that case \underline{A} , $\underline{\Lambda}$, $\underline{\Gamma}$, and $\underline{\Delta}$ are invertible square matrices.

$$\hat{\underline{D}} = \underline{A}^{-1} \underline{B}_n \underline{\Lambda}^{-1} \quad \text{and} \quad \underline{D} = \underline{\Gamma}^{-1} \underline{B}_p \underline{\Delta}^{-1} \quad (8)$$

Without any loss of generality in the following we shall assume \underline{A} , $\underline{\Lambda}$, $\underline{\Gamma}$, and $\underline{\Delta}$ to be invertible.

The realization in Fig. 3 is possible because there exists at least one realization for \mathcal{K}_n , \mathcal{K}_p , \mathcal{H}_n , and \mathcal{H}_p [7] and because both \mathcal{L}_n and \mathcal{D}_p contain only forward paths as shown in Fig. 4. Obviously, realization in Fig. 3 has no delay-free loop. The coefficients of f_k 's, g_ℓ 's, h_m 's, and p_n 's can be used as parameters of design to achieve low-noise

or low sensitivity realizations. The realization of Fig. 3 employs the minimum number of both z_1^{-1} - and z_2^{-1} -blocks but in general uses more than N_b z_2^{-1} -delays. By simple manipulations, the structure can be modified to have only (N_b+1) , z_2^{-1} -delays as is discussed in [7]. Note that although the modified structure will use one extra z_2^{-1} -delay than is suggested by (4), it can be called a "minimal" realization. One extra z_2^{-1} -delay is the minimum number of such elements needed to perform one step prediction and is a must for making the configuration admissible.

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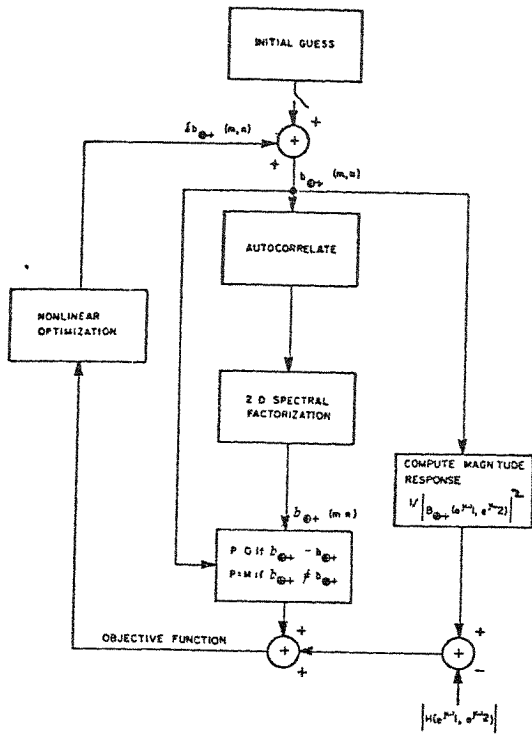


Figure 1. Half-plane filter design algorithm of [4].

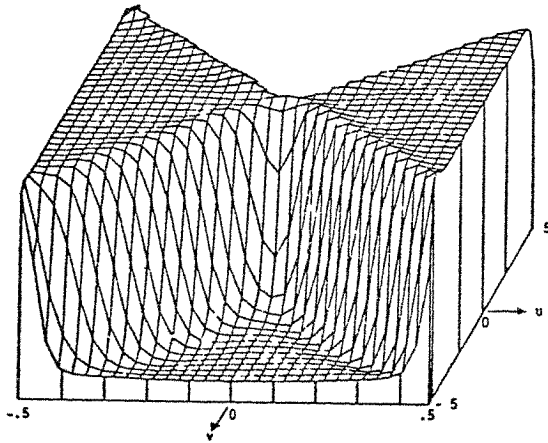


Figure 2. Magnitude-squared response of the 3×3 half-plane filter with 4×4 numerator.

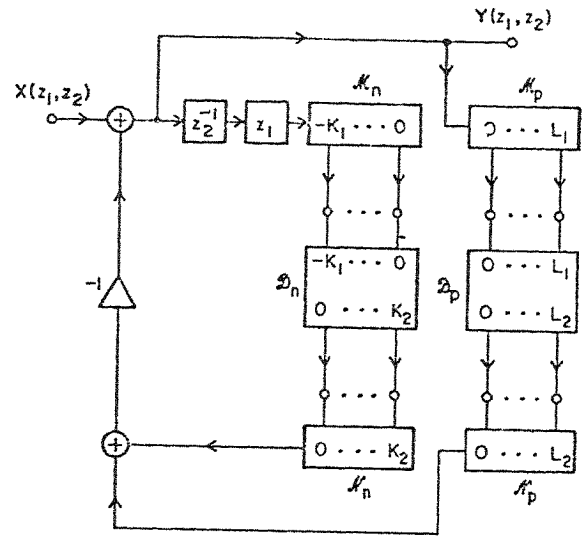
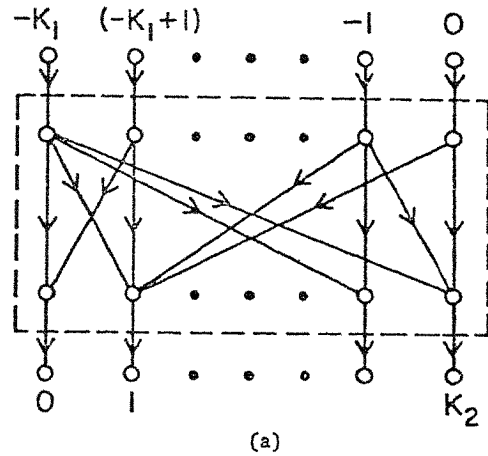
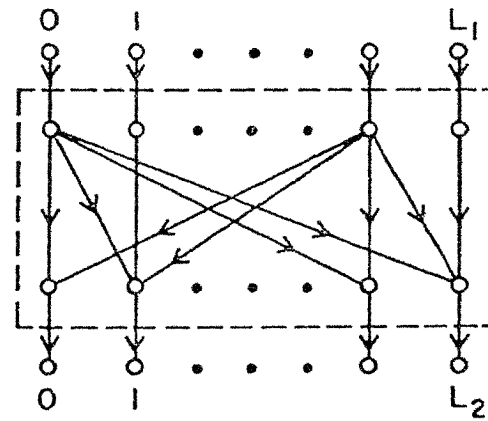


Figure 3. The configuration realizing (4).



(a)



(b)

Figure 4. Simplest topological realizations of (a) \mathcal{Z}_n and (b) \mathcal{Z}_p with corresponding branch transmittances from the i -th input node to the j -th node: $d(i,j)$ and $d(1,j)$, respectively.

TECHNICAL BIOGRAPHY - Irwin W. SANDBERG

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A CHARACTERIZATION OF THE INVARIANCE OF POSITIVITY FOR FUNCTIONAL DIFFERENTIAL EQUATIONS

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ABSTRACT

For systems of functional differential equations that can take into account finite or infinite delays, a complete characterization is given of the invariance of positivity in the sense that all solution components are positive whenever the initial condition function is positive. A related result concerning a comparison of the solutions of pairs of initial value problems is also given. One application of the results described concerns a model for synchronizing geographically separated oscillators, and another is in the area of economics.

I. INTRODUCTION

Consider a system of functional differential equations of the form

$$\dot{x} = f(t, x_t), \quad t \geq t_0, \quad x_{t_0} = \phi \quad (1)$$

in which x is a real n -vector valued function of t , \dot{x} denotes dx/dt , ϕ is an initial condition function, and x_t denotes the function defined by $x_t(s) = x(t+s)$ for $s \leq 0$. (When $f(t, x_t)$ depends only on t and $x_t(0)$, (1) reduces to a system of ordinary differential equations.)

The main purpose of this paper is to give a solution to the problem of determining conditions under which (under certain typically very reasonable conditions on f), $x(t)$ of (1) has components that are all positive for $t \geq t_0$ whenever ϕ is positive in, for example, the sense that $\phi(s)$ has positive components for $s \leq 0$. The problem arises in connection with the mathematical modeling and analysis of economic processes, and it comes up in several other areas as well. (An example concerning the synchronization of geographically separated oscillators is described in Section 2.6.) In some instances, the invariance of positivity in the sense described above is crucial, in that the lack of positivity of a component of $x(t)$ for some t and positive ϕ means that the associated model is inappropriate.

Our main result, Theorem 1 of Section II, is concerned with the case in which f is continuous and locally Lipschitz. It provides an explicit and useful condition under which positivity is invariant, and it also asserts that positivity is invariant if and only if (1) preserves nonnegativ-

ity in the sense that $x(t)$ has nonnegative components for $t \geq t_0$ whenever ϕ is nonnegative.

The nonnegativity-preservation problem has been considered in [1], [2], and [3], and the relationship between Theorem 1 and the earlier material is indicated in Section 2.3.

A corollary of Theorem 1 is as follows. Suppose that (1) is a system of ordinary differential equations, and that f is continuous and satisfies a global Lipschitz condition (in the usual sense). Let $g(t, x)$ denote $f(t, x_t)$. Then positivity is invariant for (1), by which we mean invariant for each starting point t_0 , if and only if for each i , $g_i(t_0, v) \geq 0$ for each t_0 and each real n -vector v such that $v_i = 0$ and $v_j \geq 0$ for $j \neq i$. Notice that for the special case in which $f(t, x_t) = Ax$, where A is a real $n \times n$ matrix, our condition is equivalent to the requirement that the off-diagonal elements of A are nonnegative. The corresponding proposition concerning nonnegativity preservation for this case is well known [4]. Of some interest is the fact that the corollary described above becomes false if the Lipschitz hypothesis is replaced with the assumption that (1) has exactly one solution for each initial condition (see Section 2.3).

A result related to Theorem 1 that provides a necessary and sufficient condition for the invariance of positivity, or of nonnegativity, of the difference of the solutions of a pair of equations of the type (1) is given in Section 2.4. Specific applications of that result, as well as of Theorem 1, are described in Section 2.6.

II. CHARACTERIZATION OF THE INVARIANCE OF POSITIVITY

2.1 Preliminaries

We shall use the following notation and definitions.

With n an arbitrary positive integer, R^n denotes the set of real n -vectors $v = (v_1, v_2, \dots, v_n)$, $R_+^n = \{v \in R^n: v_i \geq 0 \text{ for each } i\}$, and $|v| = \max |v_i|$ for $v \in R^n$. For u and v in R^n , the inequality $u \geq v$ ($u > v$) means that $u_i \geq v_i$ ($u_i > v_i$) for each i . The zero n -vector of R^n is denoted by θ .

We denote by C the Banach space of bounded continuous functions from $(-\infty, 0]$ to R^n , with norm

given by $|w| = \sup_{t \in (-\infty, 0]} |w(t)|$ for all $w \in C$.

The symbol T denotes any real interval of the form $[\alpha, \infty)$, (α, ∞) , or $(-\infty, \infty)$, and t_0 is an element of T . For each $t \in T$, and each bounded continuous function w from $(-\infty, t]$ to \mathbb{R}^n , w_t denotes the element of C defined by $w_t(s) = w(t+s)$ for $s \leq 0$.

Throughout Section II, f in (1) denotes a mapping of $T \times C$ into \mathbb{R}^n . We say that f is continuous in t if $f(t, w_t)$ is a continuous function of t for $t \geq t_0$ whenever $t_0 \in T$ and w is a bounded continuous mapping of $(-\infty, \infty)$ into \mathbb{R}^n , and we say that f is locally Lipschitz if for each $t_0 \in T$, each $\gamma \in [t_0, \infty)$, and each compact set B in \mathbb{R}^n , there is a constant $\rho(t_0, \gamma, B)$ such that $|f(t, u) - f(t, v)| \leq \rho(t_0, \gamma, B) |u - v|$ for each $t \in [t_0, \gamma]$ and each u and v in C such that the range of u , and also of v , is contained in B .

By a solution of (1) through a given $(t_0, \phi) \in T \times C$ is meant a continuous \mathbb{R}^n -valued function x that is defined on $(-\infty, \infty)$, is differentiable on $[t_0, \infty)$, and is such that (1) is satisfied (with the understanding that at $t = t_0$, \dot{x} denotes the right-hand derivative).^{*} As in the case of ordinary differential equations, if f is continuous in t and satisfies a uniform Lipschitz condition in the sense that f satisfies a local Lipschitz condition with $\rho(t_0, \gamma, B)$ independent of B , for each $(t_0, \phi) \in T \times C$ there is a unique solution of (1) through (t_0, ϕ) (see P. 409 of [5]).

In the next section, we refer to the following hypothesis.

H.1: There is a solution x of (1) through each $(t_0, \phi) \in T \times C$, and f is locally Lipschitz as well as continuous in t . (In particular, each solution of (1) is unique).

2.2 Our Principal Result

Under the assumption that H.1 holds, consider the following properties and condition.

Property 1 (Invariance of Positivity, Version 1): For each $(t_0, \phi) \in T \times C$ such that $\phi(0) > \theta$ and $\phi(s) \in \mathbb{R}_+^n$ for $s \leq 0$, we have $x(t) > \theta$ for $t \geq t_0$.

Property 2 (Invariance of Positivity, Version 2): For each $(t_0, \phi) \in T \times C$ such that $\phi(s) > \theta^*$ for $s \leq 0$, we have $x(t) > \theta$ for $t \geq t_0$.

^{*} It will become clear that our development can be extended at once to cover the case in which a solution need be defined on only an interval of the form $(-\infty, \beta)$ with $\beta > t_0$.

Property 3 (Invariance of Nonnegativity): We have $x(t) \geq \theta$ for $t \geq t_0$ whenever $(t_0, \phi) \in T \times C$ with $\phi(s) \in \mathbb{R}_+^n$ for $s \leq 0$.

Condition 1: For each i , $f_i(t_0, \phi) \geq 0$ whenever $(t_0, \phi) \in T \times C$ with $\phi(s) \in \mathbb{R}_+^n$ for $s \leq 0$ and $\phi_i(0) = 0$.

Theorem 1: Let H.1 be satisfied. Then the following four statements are equivalent: Property 1 holds, Property 2 holds, Property 3 holds, and Condition 1 is met.

The proof of Theorem 1 is omitted in this version of the paper.

2.3 Notes

The Condition 1-implies-Property 3 assertion of the theorem becomes false if the hypothesis that f is locally Lipschitz is dropped and Property 3 is modified in the natural way so that it concerns all solutions that correspond to the indicated type of initial condition [2].

The following example shows that the theorem becomes false if the Lipschitz hypothesis is replaced with the assumption that (1) has at most one solution for each $(t_0, \phi) \in T \times C$. Let $n=1$, and let f be defined for all t by $f(t, x_t) = -(x(t))^{1/2}$ for $x(t) \geq 0$, and $f(t, x_t) = 0$ for $x(t) < 0$. Observe that f is continuous, and that a solution (in the usual sense of $\dot{x} = f(t, x_t)$ for $t \geq 0$, $x(0) = x^0$, is given by $x(t) = x^0$ for $t \geq 0$ if $x^0 < 0$, and $x(t) = ((x^0)^{1/2} - 1/2t)^2$ for $t \in [0, 2(x^0)^{1/2}]$ with $x(t) = 0$ for $t > 2(x^0)^{1/2}$ if $x^0 > 0$. It can be verified that there are no other solutions, even though f is not locally Lipschitz. While here $x(t)$ is nonnegative for $t \geq 0$ whenever $x^0 \geq 0$, it is obviously not true that $x(t)$ is positive for all $t \geq 0$ whenever x^0 is positive.

Essentially, the fact that Condition 1 and Property 3 are equivalent for ordinary differential equations is proved in [2], and in [3] (and in the setting provided by the results in [5]) that result is extended to cover the more general case. At the time [2] was written this writer was unaware of [1] which contains a theorem (proved in a very different way) from which the result in [2] can be obtained. Our proof of the equivalence of Condition 1 and Property 3 (which is omitted in this version of the paper) is basically the same as the proof in [2] for the ordinary differential equations case. A modification of our proof is used to prove the theorem described in the next section. Also, for the case in which (1) takes into account only finite delays (i.e., for equations of "retarded" type), a direct variation of the proof, using the continuous dependence result in, for example, [6], shows that Condition 1 and Property 3 are equivalent without the Lipschitz hypothesis, provided that (1) has exactly one solution for each $(t_0, \phi) \in T \times C$.

2.4 The Comparison Theorem

The proof of Theorem 1 can be modified to establish a corresponding theorem concerning a comparison of the solutions of two initial value problems. To describe that result, let g be a function from $T \times C$ into R^n , and consider together with (1) the equation

$$\dot{y} = g(t, y_t), \quad t \geq t_0, \quad y_{t_0} = \psi \quad (2)$$

as well as the following hypothesis, properties, and condition.

H.2: For each $(t_0, \phi) \in T \times C$, (1) has a solution x , and similarly, for each $(t_0, \psi) \in T \times C$, (2) has a solution y . The mappings f and g are continuous in t , and at least one of the mappings f or g is locally Lipschitz.

Property 4: For each $(t_0, \phi, \psi) \in T \times C \times C$ such that $\phi(0) > \psi(0)$ and $\phi(s) \geq \psi(s)$ for $s \leq 0$, we have $x(t) > y(t)$ for $t \geq t_0$ (i.e., we have $x(t) > y(t)$ for $t \geq t_0$ for any solution x of (1) through (t_0, ϕ) and any solution y of (2) through (t_0, ψ)).

Property 5: For each $(t_0, \phi, \psi) \in T \times C \times C$ such that $\phi(s) > \psi(s)$ for $s \leq 0$, we have $x(t) > y(t)$ for $t \geq t_0$.

Property 6: We have $x(t) \geq y(t)$ for $t \geq t_0$ whenever $(t_0, \phi, \psi) \in T \times C \times C$ such that $\phi(s) \geq \psi(s)$ for $s \leq 0$.

Condition 2: For each i , $f_i(t_0, \phi) \geq g_i(t_0, \psi)$ whenever $(t_0, \phi, \psi) \in T \times C \times C$ with $\phi_i(0) = \psi_i(0)$ and $\phi(s) \geq \psi(s)$ for $s \leq 0$.

Our result is the following:

Theorem 2: If H.2 is met, then Property 4, Property 5, Property 6, and Condition 2 are equivalent to one another.

The proof is omitted in this version of the paper.

2.5 Comments

Since Property 6 does not hold when $f = g$ and (1) has more than one solution through some $(t_0, \phi) \in T \times C$, we see that the Condition 2-implies-Property 6 part of Theorem 2 becomes false if the hypothesis that at least one of the functions f or g is locally Lipschitz is omitted. The example given in Section 2.3 shows that the theorem becomes false even if the hypothesis is replaced with the assumption that (1) and (2) have at most one solution for each $(t_0, \phi) \in T \times C$ and each $(t_0, \psi) \in T \times C$, respectively. On the other hand, the equivalence of Condition 2 and Property 6 holds for equations of retarded type when the Lipschitz hypothesis is replaced with the assumption of uniqueness of solutions for at least one of the equations (1) and (2)†.

* For ordinary differential equations with $f = g$, this part of Theorem 2 is along the lines of a well-known result [7].

† See the corresponding comment in Section 2.3.

The proof of Theorem 2 given in the complete version of this paper can be used to verify that C in Theorem 2 can be replaced with the set of continuous bounded functions from $(-\infty, 0]$ to D , where D is any open convex subset of R^n , provided that by a solution of (1) or (2) is meant a solution whose values are contained in D for $t \geq t_0$.

2.6 Applications

There are many applications of Theorems 1 and 2. As a simple example for the purpose of illustration, consider the delay-differential equations

$$\dot{x}_i(t) = \sum_{\substack{j=1 \\ j \neq i}}^n h_{ij}(t)[x_j(t-\tau_{ij}) - x_i(t)], \quad t \geq 0$$

$$i = 1, 2, \dots, n \quad (3)$$

which arise [8] in the study of models of systems for synchronizing geographically separated oscillators. In (3), each τ_{ij} is a nonnegative constant, each h_{ij} is nonnegative, continuous, and bounded on $[0, \infty)$, $x_i(t)$ denotes the frequency of the i^{th} oscillator, and the h_{ij} can depend on x as well as on certain fixed nonlinear functions. Under certain reasonable hypotheses concerning the h_{ij} (see [8]), given a continuous $x(t)$ for $t \in \tau$, where $\tau = [-\max_{j \neq i} \tau_{ij}, 0]$, there is a constant ρ such that for each i , $x_i(t) \rightarrow \rho$ as $t \rightarrow \infty$. Assume here that there is such a ρ for each initial condition.

Theorem 1 shows that each $x_i(t)$ in (3) is positive for $t \geq 0$ whenever $x(t) > \Theta$ for $t \in \tau$.* (The nature of the dependence of the h_{ij} on x is not of consequence at this point. If it were not true that $x(t) > \Theta$ for $t \geq 0$ whenever $x(t) > \Theta$ for $t \in \tau$, we would have a contradiction to the theorem). Assuming now that the h_{ij} are independent of x , it follows from Theorem 2 that, for example, ρ is either increased or unchanged when $x(t)$ for $t \in \tau$ is replaced with any continuous $\bar{x}(t)$ for which $\bar{x}(t) \geq x(t)$ for $t \in \tau$.

Two related observations concern the equations

$$\dot{x}_i(t) = -b_{i0}[x_i(t)] + \sum_{\substack{j=1 \\ j \neq i}}^n b_{ij}[x_j(t-\tau_{ij})] + u_i(t), \quad t \geq 0$$

$$i = 1, 2, \dots, n \quad (4)$$

of a model of a compartmental system with delays [9], in which the b_{i0} and the b_{ij} for $i \neq j$ are locally Lipschitz monotone-nondecreasing functions such that $b_{i0}(0) = b_{ij}(0) = 0$, each u_i is continuous and satisfies $u_i(t) \geq 0$ for $t \geq 0$, and, as in

* This proposition is a special case of Lemma 1 of [8] whose proof is very different.

the preceding example, the τ_{ij} are nonnegative constants. In (4), $x_i(t)$ denotes the amount of material in the i^{th} compartment.

From Theorem 2, we see that if x^a is a solution of (4) corresponding to $(u_1, u_2, \dots, u_n) = u^a$ and $x(t) = x^a(t)$ for $t \in \tau$, where again $\tau = [-\max_{i \neq j} \tau_{ij}, 0]$, and similarly with regard to x^b and u^b , then we have $x^a(t) \geq (>) x^b(t)$ for $t \geq 0$ when $u^a(t) > u^b(t)$ for $t > 0$ and $x^a(t) \geq (>) x^b(t)$ for $t \in \tau$. The " $>$ " part" of this proposition was given in [9]. From Theorem 1, it is clear that we have $x(t) > 0$ for $t \geq 0$ whenever $x(t) > 0$ for $t \in \tau$, which does not seem to have been proved earlier, even for the case in which $\tau_{ij} = 0$ for all $i \neq j$.*

Consider now the case in which f in (1) is given by $f_i(t, x_t) = h_i(x_t)$ for each i , where each h_i is a functional on C with the property that $h_i(u) \geq h_i(v)$ for all u and v in C such that $u_i(s) = v_i(s)$ and $u(s) \geq v(s)$ for $s \leq 0$. Functions f of this form are generalizations of time-invariant quasimonotone (or Wazewski type) functions [10] which are of interest in several areas, including economics. In economics applications, the $x_i(t)$ often denote prices (see, for example, [11]). Observe that (4) is of the form considered here when the u_i are independent of t .

Assuming that H.1 is met, Theorem 1 provides the following simple necessary and sufficient condition for the invariance of positivity in the sense of Property 1 or Property 2: For each i , $h_i(w) \geq 0$ for each w in C such that $w_i(0) = 0$, $w_i(s) \geq 0$ for $s \leq 0$, and $w_j(s) = 0$ for $s \leq 0$ and $j \neq i$.

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* The monotonicity of the b_{i0} and b_{ij} is not needed for this result. It suffices that $\alpha b_{ij}(\alpha) \geq 0$ for $\alpha > 0$ and $i \neq j$.

TECHNICAL BIOGRAPHY - Chi-Chia HSIEH

Chi-Chia HSIEH received his B.S.E.E. degree from National Taiwan University in 1965, and his Ph.D. E.E. degree from University of Santa Clara, Santa Clara, California in 1975.

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Dr. Hsieh has been designing thin-film microwave circuits for over seven years. His main interest are in the low-noise and high-power amplifiers, down-converters, and subsystems.

LINEAR AMPLIFICATION TECHNIQUES IN 2 GHz MICROWAVE RADIOS

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Abstract

This paper describes four linear amplification techniques in the 2 GHz band which can provide high R.F. output power with low third-order intermodulation distortion, namely; The Brute-Force technique, the Negative Feed-Back technique, the Feed-Forward technique, and the I.F. Pre-distortion technique. The basic operation, the advantages, and the disadvantages of each technique will be described, a comparison of these techniques will be given.

Introduction

In the design of some microwave radios in the 2 GHz band, a linear high power amplifier is needed to provide high output power with low intermodulation products at the output of the amplifier may fall within the carrier frequency band of interest, and therefore cannot be eliminated by R.F. filtering techniques. Therefore, the difference in R.F. levels between the carrier and the third-order intermodulation distortion products (in dB) can be used as a meaningful measure of the linearity of the power amplifier at a given output power.

The common way of indicating the linearity of an R.F. power amplifier is to specify the output power at the 1-dB gain compression point or the third-order intercept point. Because of the "non well-behaved" characteristic (that is, the third-order intermodulation distortion curve does not follow the 3:1 slope) of many R.F. power transistors manufactured today, these two numbers no longer provide a meaningful indication of the linearity of power amplifiers. Hence, the best indication of the linearity of the R.F. power amplifier will be the completed plot of the saturation and the third-order intermodulation distortion curves with respect to input and output powers (Figure 1).

The main difficulty in designing a high power linear amplifier is trying to maintain high D.C. efficiency and providing high linear output power simultaneously. There are four different ways of achieving high linear amplification which will be described in the following sections.

1. **Brute-Force Technique:** This is also known as the "Back-Off" technique which is the most common way of achieving linear amplification [1]. In this

technique one would operate the amplification at an output level which is far below its output capability. As shown in Figure 1, if the amplifier is "well-behaved", the third-order intermodulation distortion products will be reduced at a 2:1 ratio with respect to the output power level. If the amplifier is not "well-behaved" (Figure 2), then one should carefully examine the third-order intermodulation distortion curve with respect to the output power to be certain that at high output level (such as in an AM system) the system can withstand the amount of third-order intermodulation distortion products.

The main advantages of this technique are; 1) it does not require any linearization process, 2) the only band limiting element is the amplifier, therefore it is relatively easy to obtain broadband amplification. Two major disadvantages of this approach are; 1) it requires high-power linear transistors which are hard to obtain at the present time. The highest rate commercially available linear power transistor can provide an output power of 2-watts at 2 GHz with third-order intermodulation products down 30 dB from the carrier level. This performance is obtained using a two-tone signal with low intermodulation distortion (-50 dB). Therefore, to obtain a 2-watt linear output power, the amplifier would require several high level stages and a large number of power transistors. 2) Due to the low efficiency of the Class-A amplifier, the unit necessarily dissipates a large amount of DC power, hence making the approach impractical.

2. **Negative Feed-Back Technique:** It is well-known that negative feedback is a way of reducing distortion in linear amplifiers. However, application of negative feedback to a microwave amplifier requires special treatment of the time delay and bandwidth involved [2] [3]. Since a typical amplifier will have several cycles delay from input to output, a simple means of applying feedback is to include a single-tuned, band-limiting cavity in the feedback loop. Such a configuration is shown in Figure 3. The amplifier A, feedback loss B, and cavity C are chosen so that the loop transmission is greater than one only between two frequencies of 180° phase shift. Consider the response of each block:

$$A = ae^{-j\tau_a\Delta\omega} \quad (1)$$

$$B = be^{-j\tau_b\Delta\omega} \quad (2)$$

$$C = \frac{c}{1 + j\Delta\omega T} \quad (3)$$

Where a, b, and c are the midband gains of each block, τ_a and τ_b are the time delays through the amplifier and feedback path, T is the cavity time constant $T = 1/\pi BW$, and $\Delta\omega$ is the frequency difference from the center frequency. (Where B includes the input and output couplers.) Then:

$$e_o = \frac{AC}{1 + ABC} e_i + \frac{1}{1 + ABC} e_{im} \quad (4)$$

Where e_{im} is the intermodulation products introduced by the amplifier. Thus the intermodulation products are reduced by $1/(1 + ABC)$ and the amplifier gain is reduced by $C/(1 + ABC)$.

The factor $(1 + ABC)$ determines the trade-offs which must be made between loop gain, bandwidth, and phase margin. For a given set of loop gain and phase margin the maximum bandwidth can be easily determined. The total time delay from input to output ports of a practical 2 GHz high power linear amplifier is approximately 11 ns, assuming a reduction of 10-dB in the intermodulation products is needed, the maximum bandwidth of this amplifier is less than 5 MHz. This clearly shows the main drawback of negative feed-back technique. However, for a narrow band application this technique could be the most practical way to achieve linearity at microwave frequencies.

3. Feed-Forward Technique: The feed-forward error-control technique was first proposed by H. S. Black [4]. By applying the MIC technology it is possible for one to produce a practical feedforward amplifier system, which will deliver high linear output power at a considerable reduction of the applied DC power as compared to the Brute-Force approach [5] [6] [7] [8].

The basic operation of a feedforward error-control system can be described by means of a block diagram as shown in Figure 4. An input signal $A_1 e^{j\omega t}$ enters the system through an input coupler C_1 , and is split into two isolated ports: one ($A_1 e^{j\omega t}$) driving the main amplifier (with gain K and delay τ) into saturation, and the other entering a reference path. The reference signal is delayed by an amount of time which is equal to the transit time through the main amplifier. This distortion-free signal $A_1 e^{j\omega(t-\tau)}$ is then subtracted from the output of the main amplifier which contains all the IM distortion products, $(A_1 K + B) e^{j\omega(t-\tau)}$, by means of a sampling Coupler C_2 , an attenuator (with attenuation $1/K$), and an error-determination coupler C_3 .

The result of this subtraction - $(B/K) e^{j\omega(t-\tau)}$ which contains all the distortion products must then be brought to the compatible level with that of the main amplifier output signal so that error cancellation can be achieved. This requires an auxiliary amplifier (with gain K and delay τ') and a corresponding delay (τ') for the main amplifier signal so as to maintain time-frame compatibility. Finally, the error signal $-Be^{j\omega(t-\tau-\tau')}$ and the delayed main amplifier signal $(A_1 K + B) e^{j\omega(t-\tau-\tau')}$ are brought together for cancellation in the error-injection coupler C_4 and the distortion-free amplified signal $A_1 K e^{j\omega(t-\tau-\tau')}$ emerges at the output port.

To achieve temperature stability in a practical feedforward system, the degree of linearity improvement should be kept at a reasonably low level. Experiments show that a 20-dB of linearity improvement would correspond to a phase imbalance of 5° and a gain imbalance of 1.0 dB, which means that the system can withstand circuit parameter variations due to temperature change without any adaptive control system.

The band limiting elements in a feedforward amplifier system are the amplifiers. The couplers, the attenuators, and the phase shifters. Broad-band amplifiers, and passive circuit elements are readily available, therefore a feedforward amplifier with bandwidth of 30 MHz at 2 GHz can be achieved.

The main disadvantage of feedforward amplifier system is its circuit complexity. However, using MIC technology with a high level of circuit integration will greatly simplify the system.

4. I.F. Predistortion Technique: Recent reports [9] [10] show that by applying predistortion technique at the IF frequency stage, a reduction of intermodulation distortion products at the output of the RF power amplifier can be achieved. The technique provides both broad frequency bandwidth and wide dynamic range.

The basic operation of an IF predistortion system can be shown in Figure 5. The input coupler C_1 splits up the incoming signal and distributes it among the two arms of the bridge which have an equal electrical length. The 180° phase shift required for the subtraction is achieved by the two couplers C_1 and C_2 . An amplifier located in one of the arms generates nearly the same intermodulation distortion as the main RF power amplifier. A time delay equalizer τ in the second arm serves for setting the same electrical length. By means of coupler C_2 both arms of bridge are coupled together with an amplitude ratio of 2:1, the signal from the passive arm having the higher level. The signal-to-noise ratio at the output of the bridge, i.e., at b, is the same as that of the predistortion amplifier; except, the distortion products are in opposite phase. This predistorted signal is then up converted to the RF frequency and fed

into the main power amplifier. Hence, the intermodulation distortion products generated by the main power amplifier will be reduced.

Experiment shows that a 15-dB of linearity improvement can easily be achieved by carefully selecting the predistortion amplifier. To achieve a wide dynamic range one must carefully select a predistortion amplifier which has the same third-order intermodulation distortion characteristic as the main power amplifier.

Conclusion

Four linear amplification techniques in the 2 GHz band has been described. Each technique has its advantages and disadvantages; therefore, in selecting a suitable linear amplifier for 2 GHz microwave radio one must carefully examine the specific linearity requirement. If efficiency is not a major concern, or the output power required is relatively low, then the "Brute-force" technique will be the most practical one. For narrow band applications, to achieve 10-15 dB linearity improvement the Feedback technique will be the best candidate. Feedforward technique can provide high level of linearity improvement (20-25 dB) at low DC power consumption. The IF predistortion technique provides a 10-15 dB linearity improvement at very low cost. Broadband operation and wide dynamic range make the predistortion technique a practical solution in many microwave radios.

Acknowledgement

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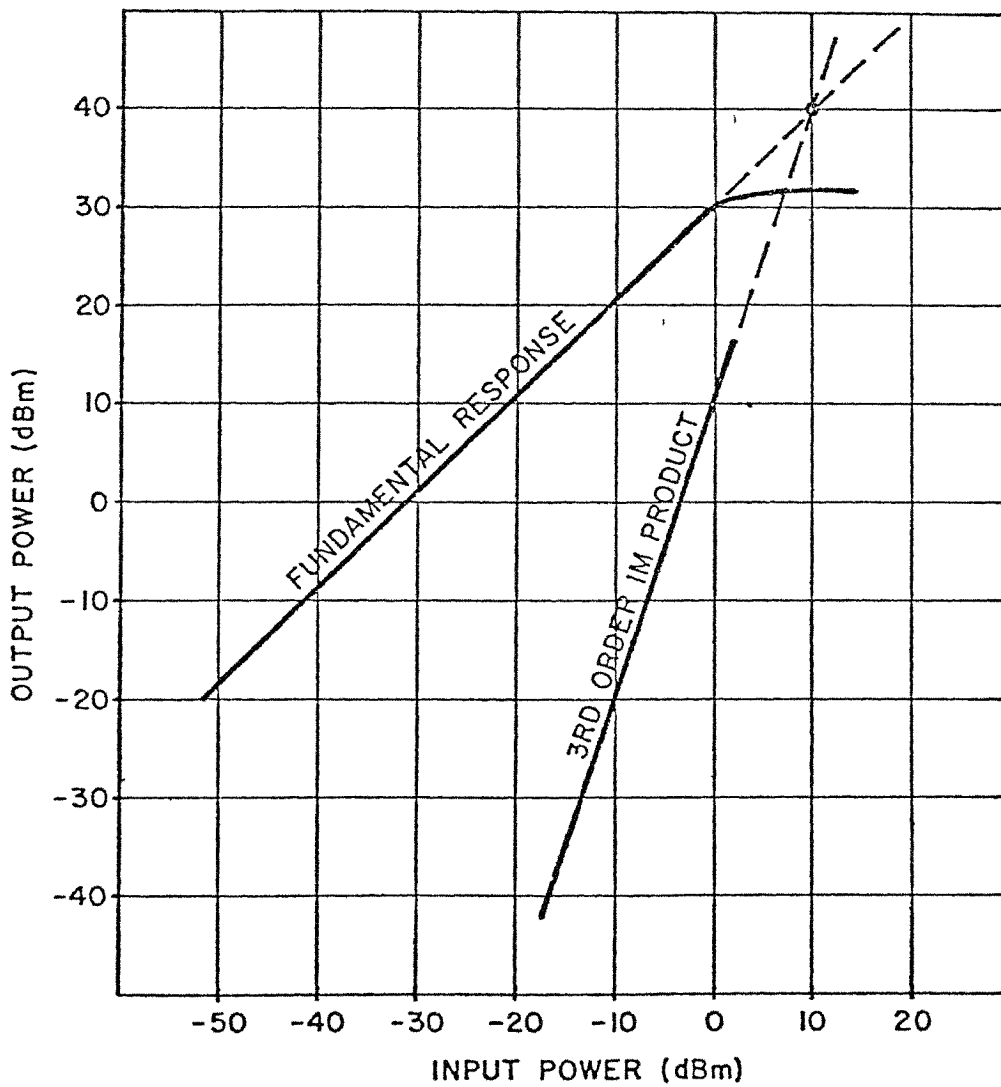
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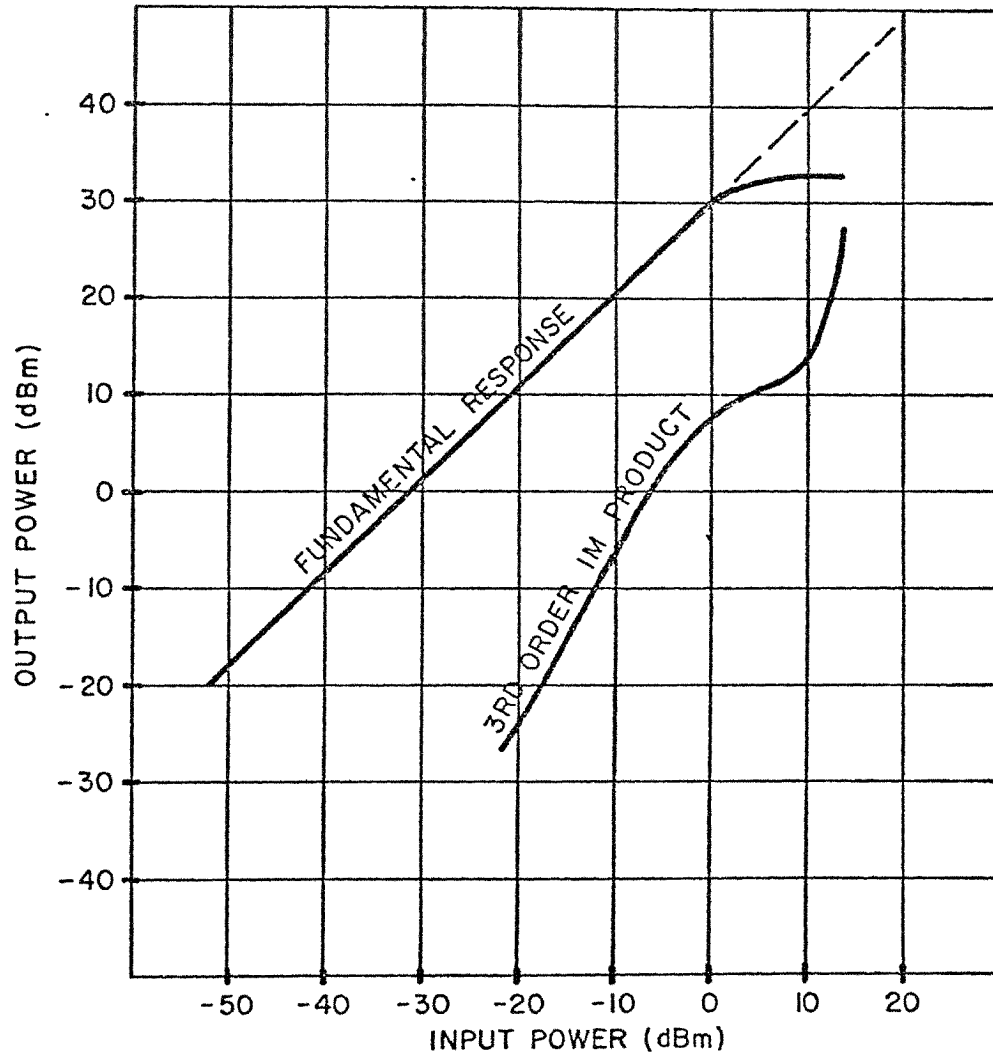
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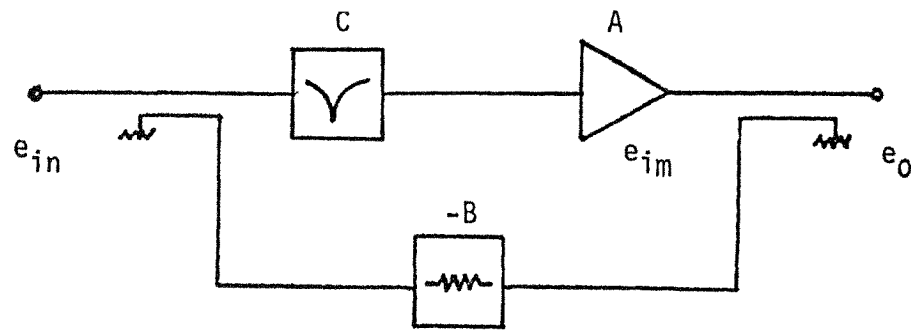
The Fundamental and Third-Order IMD Response Curves of a Well-Behaved Linear Amplifier

FIGURE 1



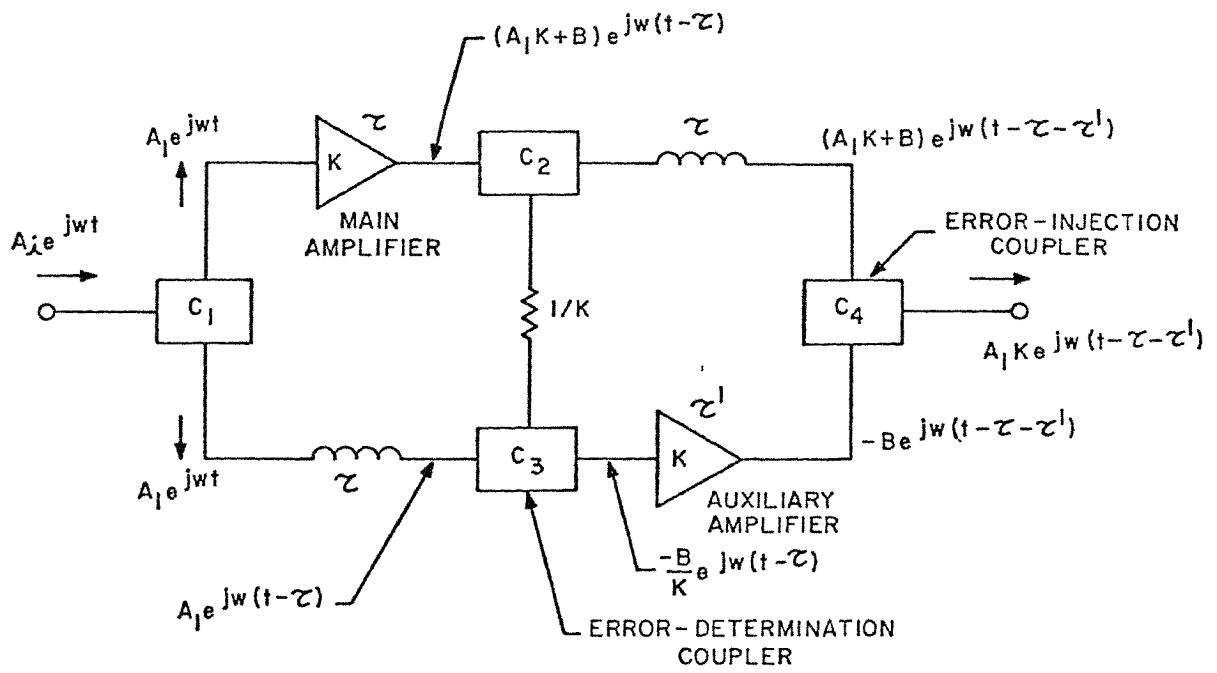
The Fundamental and Third-Order IMD Response Curves of
A Non Well-Behaved Linear Amplifier

FIGURE 2



A Microwave Feedback Amplifier System

FIGURE 3



A Feedforward Error Control System

FIGURE 4

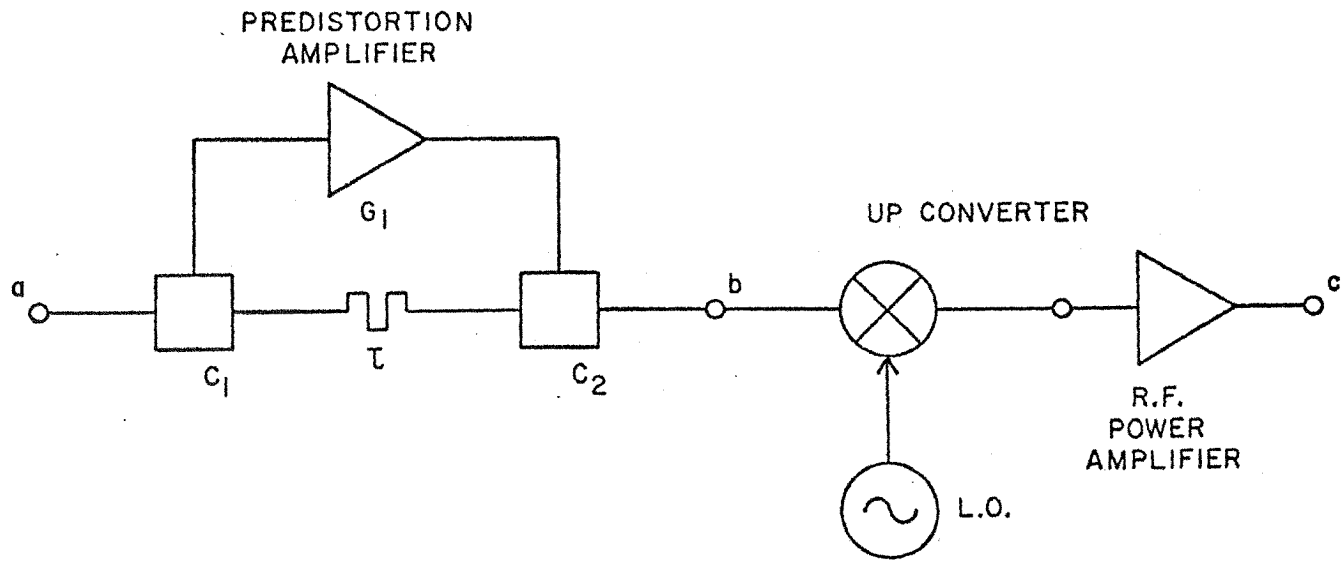


FIGURE 5. AN IF PREDISTORTION SYSTEM.

TECHNICAL BIOGRAPHY - Leon O. CHUA

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COMPLETE STABILITY OF NON-RECIPROCAL NONLINEAR NETWORKS

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ABSTRACT

This paper reports a recent breakthrough in research on deriving complete stability criteria for non-reciprocal network having multiple equilibrium points. Although the proof is quite mathematical in nature, the method itself is circuit-theoretic and is applicable to a large class of non-reciprocal network.

INTRODUCTION

An autonomous system $\dot{x} = f(x)$, $x \in \mathbb{R}^n$ is said to be "completely stable" if all solutions converge to some equilibrium points in the state space. This property is extremely important in practice because it excludes not only oscillations, but also other more exotic modes, such as almost-periodic oscillations. In the special case where the system has only one equilibrium point, the concept of complete stability [1,2] reduces to that of "global asymptotic stability." Much research has been directed at deriving conditions for identifying completely stable nonlinear network [3-7]. The results obtained so far, however, have been restricted to either "reciprocal" networks [3,5,6] (or "eventually reciprocal" [4] networks), or networks which have only one equilibrium point [7]. Unfortunately, these results are not applicable to many non-reciprocal networks of practical interest, such as switching networks which invariably have multiple equilibrium points. This "non-reciprocity" barrier has not been overcome in spite of much research efforts over the past decade because of the formidable problem of constructing global Lyapunov functions for such networks. In this paper, we report a breakthrough in this non-reciprocity barrier which we believe would have far reaching significance for research in this area.

DEFINITIONS AND BASIC PROPERTIES [8]

Consider the system described by an ordinary differential equation

$$\dot{x} = f(x), \quad x \in \Sigma \subseteq \mathbb{R}^n, \quad \Sigma \text{ is open} \quad (1)$$

where $f: \Sigma \rightarrow \mathbb{R}^n$ is assumed to be continuously differentiable (unless otherwise specified). A particular point x is called an equilibrium point of the system if $f(x) = 0$. We will be dealing only with systems having isolated and a finite number of equilibrium points.

A function $x: \mathbb{R}_+ \rightarrow \Sigma$ is called a solution of

the system if $\frac{d}{dt} x(t) = f(x(t))$ for all $t \in \mathbb{R}_+$ (where $\mathbb{R}_+ =$ set of all nonnegative real numbers). A solution is bounded if its range is bounded. A point p is called an ω -limit point of a solution $x(\cdot)$ if there is an unbounded increasing sequence $\{t_k\}$ such that $\lim_{k \rightarrow \infty} x(t_k) = p$. The set of all ω -limit points of a solution is the ω -limit set of that solution. A subset $M \subseteq \Sigma$ is called positively invariant if every solution $x(\cdot)$ with $x(0) \in M$ satisfies $x(t) \in M$ for all $t > 0$.

Let ω be a map from Σ to the collection of all subsets of Σ which sends a point p to the ω -limit sets of all solutions $x(\cdot)$ with $x(0) = p$. Since f is continuously differentiable, there is one and only one solution with p as the initial point. A fundamental result which will be invoked quite often in the proofs is that if the solution starting at p is bounded, then $\omega(p)$ is nonempty, compact and connected. Also well known, is that $\omega(p)$ contains entire solutions, not necessarily $x(\cdot)$, and $\omega(p)$ is invariant in the sense that all solutions originating in $\omega(p)$ remain within $\omega(p)$.

Also useful in this paper is the notion of a general solution which is a function $\phi: \mathbb{R} \times \Sigma \rightarrow \Sigma$ with the property that (for our purpose) $\phi(\cdot, p)$ is a solution for all $p \in \Sigma$. A theorem about the general solution states that if f is r times continuously differentiable so is ϕ .

GENERAL THEOREMS ON COMPLETE STABILITY

A subset K of the space Σ is called a complete set of the system if K is positively invariant and contains its ω -limit sets i.e.

$$K \supset \omega(K) \triangleq \bigcup_{p \in K} \omega(p)$$

The following theorem is a more general version of an earlier result [6].

Theorem 1. Let $K \subseteq \Sigma$ be a complete set and $V: K \rightarrow \mathbb{R}$ be a continuously differentiable function on K with

- a) $(\forall V(x))^T f(x) \leq 0$ for all $x \in K$,
- b) $(\forall V(x))^T f(x) = 0$ if and only if $f(x) = 0$,

then all bounded solutions in K converge to equilibrium points in K .

Corollary 1. If in Theorem 1, $K = \Sigma$ then, the system is completely stable in the sense that all of its solutions that are bounded converge to some

equilibrium points.

Our next theorem allows us to transform the extremely difficult problem of global stability analysis into several albeit much easier stability analysis within appropriately subdivided complete subsets of the state space Σ .

Theorem 2. System (1) is completely stable if:
 1) there is a finite collection $\{(K_\alpha, V_\alpha) | \alpha \in J\}$ where each K_α is a complete set and its associated V_α satisfies on K_α , the hypotheses of Theorem 1, and
 2) there is a continuously differentiable function $V_0: \Sigma \rightarrow \mathbb{R}$ such that for $x \in \Sigma - K_J$ ($K_J \triangleq \bigcup_{\alpha \in J} K_\alpha$), we have

a) $(\nabla V_0(x))^T f(x) \leq 0$

b) $(\nabla V_0(x))^T f(x) = 0$ if $f(x) = 0$. □

Intuitively, we can interpret each K_α as a "reduced" state space and V_α as a Lyapunov function on it. These reduced systems are completely stable in view of Theorem 1. Now, the existence of V_0 implies that each bounded solution of the full system is attracted to some K and, hence, eventually to some equilibrium point. We can think of V_0 as a "global" Lyapunov function outside of K_J . Since the behavior of V_0 within each $K_\alpha \subset K_J$ is irrelevant, it is usually much easier to construct V_0 once a suitable set of K_α has been identified. The above interpretation allows us to think of each "complete set" K_α as a magnified "super" stable equilibrium point. Roughly speaking, we can establish complete stability of (1) in two steps: First, identify a suitable set of "super" stable equilibrium points. Second, show that each bounded solution tends to one of these "super" equilibrium points. We remark that sets with properties similar to K_α are sometimes called "regions of attractions" in the literature. Here, we are more precise since we also specify the mechanism of attraction.

APPLICATIONS TO NONRECIPROCAL AUTONOMOUS NONLINEAR NETWORKS

Consider now the very general class of autonomous nonlinear networks (see Fig. 1) whose state equations are described in [9]. These state equations are made up of the following 3 components: 1) Constitutive relation of the "non-reciprocal" resistive n-ports: $y = g(x)$. 2) Constitutive relations of the "reciprocal" capacitors and inductors: $x = h(z)$ where h is an injective continuously differentiable state function and H is its potential function, $\nabla H(z) = h(z)$. 3) Port interconnections: $\dot{z} = -y$

The networks in this class are described by systems of the form

$$\dot{z} = -g \circ h(z) \triangleq f(z) \tag{2}$$

Associated with the network, x_0 will be called an operating point if $x_0 = h(z_0)$ where z_0 is an equilibrium point of the system (2).

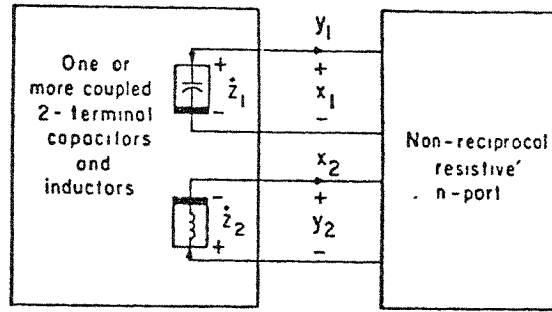


Fig. 1. A general autonomous network.

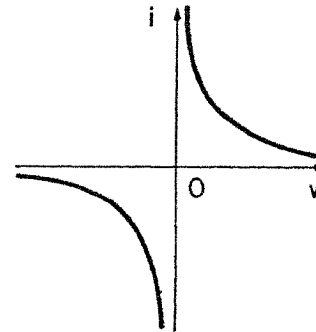


Fig. 2. A strictly passive one-port resistor which is not relatively passive.

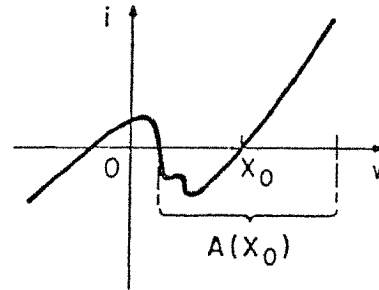


Fig. 3. An active one-port resistor which is strictly passive relative to x_0 in $A(x_0)$.

Definition. The resistive n-port is strictly passive relative to an operating point in a set $A(x_0)$ containing x_0 if

$$\langle x - x_0, g(x) \rangle > 0 \text{ for all } x \in A(x_0) - x_0$$

Remarks: 1. This definition is different from the classical definition of "passivity" and "local passivity" as illustrated in Figs. 2 and 3, respectively.

2. This definition would still be meaningful even if $x_0 \notin A(x_0)$. However, such an extension is not intuitively appealing as will be clear later. It is also possible to relax the definition where x_0 need not be an operating point. However, there doesn't seem to be any value in such a more

general setting either.

3. Classical thinking would tend to take $A(x_0)$ to be a sphere around x_0 . That is all right except that our dynamics occurs in z -space (charges and fluxes) rather than x -space (voltages and currents). Note that a sphere around an equilibrium point in z -space when mapped into the x -space is not necessarily a sphere around the corresponding operating point.

4. In this paper, it is convenient to think of "energy" and "potential" as concepts pertaining to the dynamical variables in the z -space, and to think of "power" and "dissipation" as concepts pertaining to the network variables in the x -space. These two independent concepts can be represented graphically as an "energy profile" and a "power profile," respectively. To each operating point, we can draw a corresponding power profile. The port interconnection "matches" the energy profile with each of the "power profile." We will now show in our next theorem, (the main result of this paper) that if the matching is right, there can be no oscillation.

Theorem 3. The network described by (2) is completely stable if:

1. there is a set S of operating points such that for each $x_0 \in S$, g is strictly passive relative to x_0 with

$$A(x_0) = \{x = h(z) \mid [H(z-H(z_0)) - \langle x_0, z-z_0 \rangle] < a(x_0)\}$$

for some $a(x_0)$ and $z_0 = h(z_0)$.

2. $A(s) \triangleq \bigcup_{x_0 \in S} A(x_0)$

$$\sup \{x \mid \langle x, g(x) \rangle \leq 0 \text{ and } g(x) \neq 0\}.$$

This theorem gives a criteria for matching the "energy" to the "power" profiles so that the network is completely stable. To give an interpretation of condition 1, consider the following Taylor expansion:

$$\begin{aligned} H(z) &= H(z_0) + \langle \nabla H(z_0), z-z_0 \rangle \\ &+ \frac{1}{2} \langle z-z_0, \frac{\partial^2 H}{\partial z^2}(z_0)(z-z_0) \rangle \\ &+ O(\|z-z_0\|^3). \end{aligned}$$

Since $\nabla H(z_0) = h(z_0) = x_0$, and $\frac{\partial^2 H}{\partial z^2}(z_0) = \frac{\partial h}{\partial z}(z_0)$, we can write

$$\begin{aligned} [H(z)-H(z_0)] - \langle x_0, z-z_0 \rangle &= \frac{1}{2} \langle z-z_0, \frac{\partial h}{\partial z}(z_0)(z-z_0) \rangle \\ &+ O(\|z-z_0\|^3) \end{aligned}$$

and interpret this quantity as an approximation of the incremental potential function around the equilibrium point z_0 .

V. AN ILLUSTRATIVE EXAMPLE

Consider a non-reciprocal autonomous nonlinear network described by the following component equations:

$$\begin{aligned} 1) \quad g_1(x,y) &= x(x^2-1) + \frac{3}{2}xy^2 \\ g_2(x,y) &= y + y^3 + \frac{1}{2}x^2y \\ 2) \quad (x,y) &= h(z_1,z_2) = (z_1,z_2) \\ 3) \quad \dot{z}_1 &= -g_1(x,y) \\ \dot{z}_2 &= -g_2(x,y) \end{aligned}$$

The associated state equations are given by

$$\begin{aligned} \dot{x} &= -[x(x^2-1) + \frac{3}{2}xy^2] \\ \dot{y} &= -[y + y^3 + \frac{1}{2}x^2y] \end{aligned}$$

and the operating points are $(-1,0)$, $(0,0)$, $(1,0)$. Let $S = \{(-1,0), (1,0)\}$.

$$\begin{aligned} \text{Relative to } (1,0): \quad & (x-1)x(x^2-1) + \frac{3}{2}(x-1)xy^2 \\ & + y^2 + y^4 + \frac{1}{2}x^2y^2 \\ & = x(x-1)^2(x+1) + y^2(2x^2 - \frac{3}{2}x+1) \\ & + y^4. \\ & > 0 \text{ for } x > 0 \end{aligned}$$

Suppose we choose

$$a((1,0)) = \frac{1}{2}, \text{ then}$$

$$\begin{aligned} [H(z)-H(z_0)] - \langle x_0, z-z_0 \rangle &= \frac{1}{2} \langle z-z_0, z-z_0 \rangle \\ &= \frac{1}{2} [(x-1)^2 + y^2] < \frac{1}{2} \end{aligned}$$

implies that $(x-1)^2 + y^2 < 1$. Consequently, $A((1,0))$ is an open disc of radius 1 centered at $(1,0)$.

$$\begin{aligned} \text{Relative to } (-1,0): \quad & (x+1)x(x^2-1) + \frac{3}{2}(x+1)xy^2 \\ & + y^2 + y^4 \\ & > 0 \text{ for } x < 0. \end{aligned}$$

Choosing again $a((-1,0)) = \frac{1}{2}$, we obtain

$$\begin{aligned} [H(z)-H(z_0)] - \langle x_0, z-z_0 \rangle &= \frac{1}{2} \langle z-z_0, z-z_0 \rangle \\ &= \frac{1}{2} [(x+1)^2 + y^2] < \frac{1}{2} \end{aligned}$$

and $(x+1)^2 + y^2 < 1$. Consequently, $A((-1,0))$ is an open disc of radius 1 centered at $(-1,0)$.

Now to check condition 2, we calculate

$$\langle (x,y), g(x,y) \rangle = x^2(x^2-1) + \frac{3}{2}x^2y^2 + y^2 + y^4 + \frac{1}{2}x^2y^2 + (x^2+y^2)^2 - (x^2-y^2)$$

Observe that this expression is negative inside the shaded area shown in Fig. 4, which in turn is a subset of $A(S)$. Since all hypotheses of Theorem 3 are satisfied, it follows that the network is completely stable.

PROOFS OF THEOREMS

1. Proof of Theorem 1. Let $x(t)$ be a bounded solution in K . Then $\omega(x(0))$ is compact and therefore $V(\omega(x(0)))$ is bounded. Moreover,

$$\lim_{t \rightarrow \infty} x(t) \in \omega(x(0))$$

$$\Rightarrow \lim_{t \rightarrow \infty} V(x(t)) = V(\lim_{t \rightarrow \infty} x(t)) \in V(\omega(x(0)))$$

Hence, for any unbounded increasing sequence $\{t_k\}$, $t_k \in [0, \infty)$, $\{V(x(t_k))\}$ is a bounded sequence with a finite limit. It remains for us to show that this sequence actually converges. Since $x(t_k) \in K$ $\forall t_k \in [0, \infty)$,

$$\dot{V}(x(t)) = \langle \nabla V(x(t)), f(x(t)) \rangle \leq 0 \quad \forall t \in [0, \infty)$$

Therefore, $\{V(x(t))\}$ is a decreasing sequence of real numbers. Hence it converges to a unique limit V_∞ .

Next we show that V is constant on $\omega(x(0))$. Let $x \in \omega(x(0))$, then there is a sequence

$$\{t_k\} \rightarrow \infty \text{ such that } \{x(t_k)\} \rightarrow x.$$

then

$$V(x) = V(\lim_{k \rightarrow \infty} x(t_k)) = \lim_{k \rightarrow \infty} V(x(t_k)) = V_\infty.$$

Finally, because $\omega(x(0))$ is invariant, there is a solution $\phi(t, x) \subset \omega(x(0)) \forall t$. So along this solution,

$$\dot{V}(\phi(t, x)) \equiv 0, \text{ in particular } \dot{V}(\phi(0, x)) = \dot{V}(x) = 0$$

Consequently, $\dot{V}(\omega(x(0))) = 0$ and it follows from the hypothesis that $\omega(x(0))$ consists of equilibrium points only.

2. Proof of Theorem 2. By Theorem 1, every solution that starts in K_α , converges to equilibrium points in K_α , $\alpha \in J$. Since the solution through each point is unique, every solution whose path intersects K_j must also converge to equilibrium points.

Let $X(t)$ be a bounded solution that is contained in $\Sigma - K_j$ for all finite time. If $\omega(x(0)) \cap K_j \neq \emptyset$, then either $\omega(x(0))$ consists of equilibrium points and we are done, or it doesn't. In the latter case, there is a solution that is non constant which starts in $\omega(x(0)) \cap K_j$ and is contained in $\omega(x(0))$. But such solution converges to equilibrium points in K_j .

Finally we are left with the case that $\omega(x(0)) \subset \Sigma - K_j$. But then $\{x(t)\} \cup \omega(x(0))$ is a complete set and V_0 is defined on $\Sigma - K_j$ so it is defined on $\{x(t)\} \cup \omega(x(0))$. It follows from Theorem 1 that $x(t)$ converges to an equilibrium point in $\Sigma - K_j$.

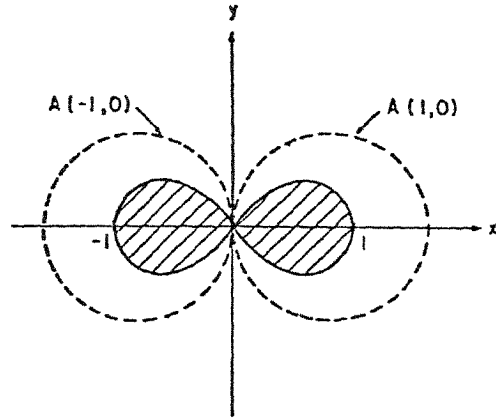


Fig. 4. The two complete sets $A((1,0))$ and $A((-1,0))$. The point $(0,0)$ is not in $A(S)$.

3. Proof of Theorem 3. Let $\hat{A}(z_0) \triangleq \{z | h(z) \in A(x_0)\}$. We will show that $\hat{A}(z_0)$ is a complete set for all z_0 such that $h(z_0) \in S$.

For $z \in \hat{A}(z_0)$ define

$$V_{z_0}(z) \triangleq [H(z) - H(z_0)] - \langle h(z_0), z - z_0 \rangle < a(x_0).$$

Pick a point $p \in \hat{A}(z_0) - z_0$, then $V_{z_0}(p) < a(x_0)$.

Let $z(t)$ be a solution starting at p . Since

$$\begin{aligned} \dot{V}_{z_0}(z(t))_{t=0} &= \dot{V}_{z_0}(p) = \langle \nabla V_{z_0}(p), \dot{z}(0) \rangle \\ &= \langle h(z(0)) - h(z_0), \dot{z}(0) \rangle \\ &= \langle h(p) - x_0, -g(h(p)) \rangle. \end{aligned}$$

and $p \in \hat{A}(z_0)$ means $h(p) \in A(x_0)$, therefore

$$\dot{V}_{z_0}(p) < 0$$

in view of the "relative passivity" hypothesis. Hence for some small time $\epsilon > 0$,

$$V_{z_0}(z(\tau)) < V_{z_0}(p).$$

Let t_1 be the earliest time such that $V_{z_0}(z(t_1)) = V_{z_0}(p)$. By the mean-value theorem, there exists a $\tau \in (0, t_1)$ such that

$$V_{z_0}(z(t_1)) - V_{z_0}(p) = \dot{V}_{z_0}(z(\tau)) \cdot t_1 = 0.$$

But this is impossible because by our choice of t_1 ,

$$V_{z_0}(z(\tau)) < V_{z_0}(p) < a(x_0) \text{ so that } z(\tau) \in \hat{A}(z_0) \text{ and therefore } \dot{V}_{z_0}(z(\tau)) < 0.$$

Consequently, for all $t \in (0, \infty)$,

$$V_{z_0}(z(t)) < V_{z_0}(p) < a(x_0), \text{ i.e. } z(t) \in \hat{A}(z_0).$$

Hence, $\lim_{t \rightarrow \infty} V_{z_0}(z(t)) < a(x_0)$ and $\omega(p) \subset \hat{A}(z_0)$.

Then $\{\hat{A}(z_0) \mid h(z_0) \in S\}$ is a collection of complete sets and $\{V_{z_0} \mid h(z_0) \in S\}$ satisfies the hypotheses of Theorem 2.

Finally, let $V_0(z) = H(z)$, then

$$\begin{aligned} \dot{V}_0(z) &= \langle \nabla H(z), z \rangle = -\langle h(z), g(h(z)) \rangle \\ &= -\langle x, g(x) \rangle, \text{ where } x = h(z), \end{aligned}$$

which by hypothesis is negative if $x \notin A(S)$ and $g(x) \neq 0$. Hence, $\dot{V}_0(z) < 0$ if $z \notin \bigcup_{h(z_0) \in S} \hat{A}(z_0)$ and $g \circ h(z) \neq 0$.

Since all hypotheses of Theorem 2 are satisfied the network is completely stable.

CONCLUSION

Although networks containing "locally active" and "non-reciprocal" elements are quite susceptible to oscillation, Theorem 3 provides us with an invaluable tool for uncovering a subclass of such networks where oscillation is impossible.

Intuitively speaking, if one measures power with respect to ground, a network belonging to this class may appear "active" in some regions of the state space. Such regions may correspond to the "charging" of capacitors, etc. Now if one searches for a "target" point where the active charging network is "aiming" for, then around that point, a "non-oscillatory" network should appear passive. In another words, the difference in energy levels between the instantaneous value and that of the target diminishes.

It might be conjectured that a substantial subclass of all "switching circuits" operates in this manner: they all have stable targets by design,

and the switching mechanism is active. However, since each target is a stable state, these must exist a region which is relatively passive with respect to each target.

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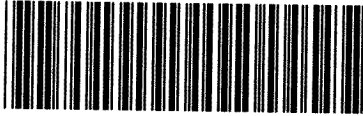
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