Improved electrical properties of metal-oxide-semiconductor capacitor with HfTiON gate dielectric by using HfSiON interlayer

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Metal-oxide-semiconductor (MOS) capacitor with HfTiON/HfSiON stack structure as high-*k* gate dielectric is fabricated, and its electrical properties are compared with those of a similar device with HfTiON only as gate dielectric. Experimental results show that the device with HfTiON/HfSiON gate dielectric exhibits better interface properties, lower gate leakage current, and enhanced high-field reliability. All these improvements should be attributed to the fact that the HfSiON buffer layer effectively blocks the diffusion of Ti atoms to the Si substrate, thus resulting in a SiO_2/Si-like HfSiON/Si interface. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2798248]

The development of alternative high-*k* gate dielectrics for future complimentary metal-oxide-semiconductor (CMOS) devices is indispensable for achieving both low leakage current and small equivalent oxide thickness.[1] Recently, Hf oxide and Hf silicate have been receiving more and more attention for the forthcoming CMOS technologies.[2–4] However, the *k* values of Hf oxide and silicate are not high enough to satisfy the requirements of high-*k* gate dielectric. So, titanium was added into Hf oxide and silicate to increase the *k* value because both Ti oxide and silicate have higher dielectric constant.[5] As a result, HfTiON is a promising high-*k* gate dielectric for small MOS devices. Besides small band offset with Si, the small bandgap[6,7] and poor thermodynamic stability[8,9] of titanium oxide compared to hafnium oxide suggest that a buffer layer should be used to isolate the Ti atoms in HfTiON from the Si substrate. It is well known that N-incorporated Hf silicate can suppress phase separation and microcrystallization, thus increasing the *k* value and decreasing the leakage current.[10] In this work, a stack structure of HfTiON on HfSiON is designed and fabricated as the high-*k* gate dielectric of MOS device. Experimental results show that excellent electrical properties and reliability can be obtained for the stack gate dielectric structure.

MOS capacitor with HfTiON/HfSiON stack gate dielectric (denoted as the stack sample) was fabricated on (100)-oriented *n*-type Si wafers with a doping concentration of 2×10^{17} cm^{-3}. After RCA cleaning, the wafers were put in diluted HF for 1 min to remove the native SiO_2. Then, the wafers were immediately loaded into the vacuum chamber of a sputtering system made by DENTON Corporation. A HfN film (~2 nm) was deposited at room temperature by the sputtering of a Hf target at 25 W rf power in an Ar/N_2 (=24/6) ambient. Igniting pressure and sputtering pressure were 60 and 6.6 mTorr, respectively. Then, HfTiN was deposited at room temperature through cosputtering of Hf at 25 W rf power and Ti at 33 W dc power in the same ambient and pressure as for the deposition of HfN. Next, the sample was transferred to a postdeposition annealing (PDA) system. The PDA was performed in N_2 (500 ml/min) at 700 °C for 30 s to oxidize the HfN and HfTiN films by consuming the residual oxygen in the N_2 ambient. During the PDA, Si out diffused into the buffer layer to form a HfSiON interlayer. A control sample with only HfTiON as gate dielectric (i.e., without the buffer layer, denoted as the control sample) was

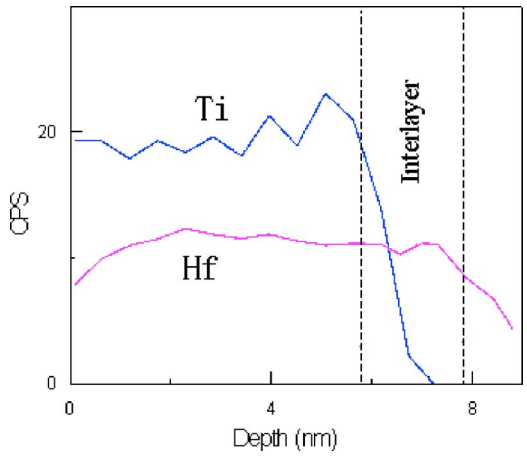

FIG. 1. XPS of the stack sample.

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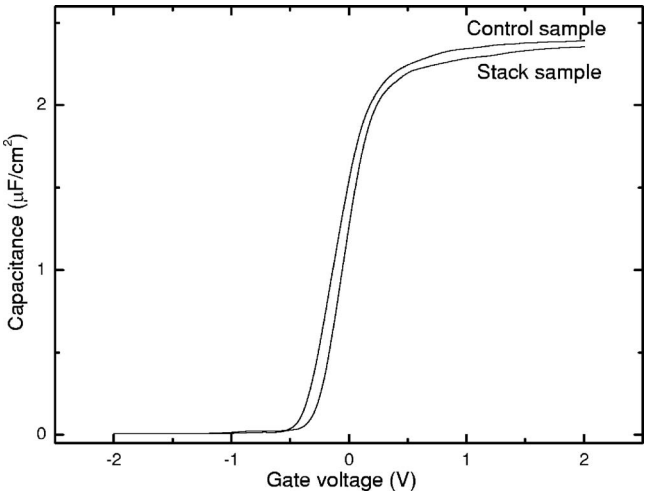

FIG. 2. Typical high-frequency *C-V* curves of the two samples.

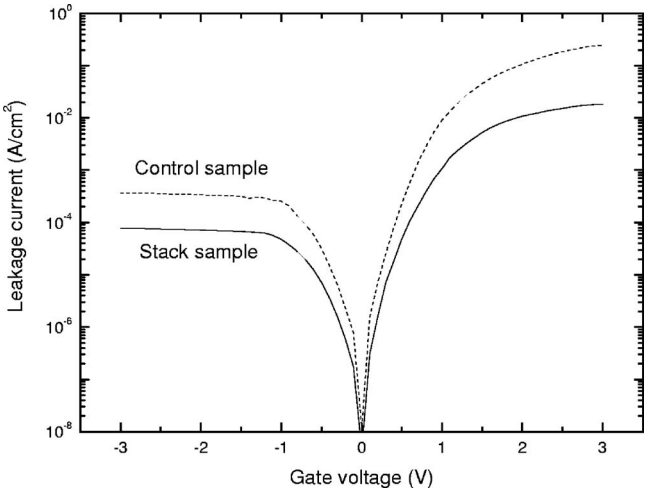

FIG. 3. Gate leakage current density of the two samples.

also fabricated. Then, Al was thermally evaporated and patterned using lithography technology as the gate electrode with an effective area of 7.85×10^{-5} cm^2. Also, Al was evaporated as the back electrode of the MOS devices to decrease contact resistance. Finally, both samples were annealed at 400 °C for 25 min in forming gas with N_2/H_2 =95/5.

High-frequency (1 MHz) *C-V* curves were measured at room temperature using HP4284A precision *LCR* meter. Flatband voltage (V_{fb}), and oxide-charge density (Q_{ox}) were extracted from the high-frequency *C-V* curves. The interface-state density (D_{it}) at midgap was also extracted from the high-frequency *C-V* curve using the Terman method.[11] High-field stress (2 MV/cm for 5000 s), with the capacitors biased in accumulation by HP4156A precision semiconductor parameter analyzer, was used to examine device reliability under high-field stress in terms of flatband-voltage shift (ΔV_{fb}) and gate-leakage increase. All measurements were carried out under a light-tight and electrically shielded condition.

The physical thickness T_{ox} of the high-k gate dielectric is measured to be 7.8 nm by ellipsometry. Ti and Hf distribution profiles of the stack sample are analyzed by x-ray photoelectron spectroscopy (XPS), as shown in Fig. 1. Obviously, Ti sharply decreases near the HfTiON/HfSiON interface and cannot penetrate to the Si surface, resulting in little reaction between Ti and Si. The *C-V* curves of the stack and control samples are shown in Fig. 2. Since the stack sample has an interlayer of HfSiON with a k value lower than that of HfTiON, it exhibits slightly smaller accumulation capacitance compared to the control sample.

Electrical parameters of the two samples are extracted from the HF *C-V* curves and listed in Table I. The equivalent oxide-charge density (Q_{ox}), including fixed charges, border-trap charges, mobile-ion charges, and interface-state charges, is calculated according to $Q_{ox}=-C_{ox}\ (V_{fb}-\phi_{ms})/q$, where ϕ_{ms} is the work-function difference between aluminum and Si substrate; C_{ox} is oxide capacitance per unit area. For the control sample, large Q_{ox} implies that a large amount of defects are generated near the interface, probably due to the reaction of Ti with Si at the interface.[9] For the stack sample, the reaction is greatly suppressed due to the isolation role of the HfSiON interlayer (~2 nm), as shown in Fig. 1, resulting in smaller Q_{ox}. Accordingly, a smaller V_{fb} shift is observed for the stack sample (−0.11 V) than the control sample (−0.20 V). Capacitance equivalent thickness (CET) can be obtained from the *C-V* curve based on CET $=k_0k_{SiO_2}/C_{ox}$, where k_0 and k_{SiO_2} are dielectric constants of vacuum and SiO_2, respectively. As compared to the control sample, smaller accumulation capacitance of the stack sample means a slightly larger CET. Moreover, the suppressed reaction between Ti and Si means that the stack sample has a lower interface-state density (2.15×10^{11} cm^{-2} eV^{-1}) than the control sample (8.27×10^{11} cm^{-2} eV^{-1}), due to the formation of a SiO_2/Si-like interface (i.e., HfSiON/Si interface). The k value of the stack sample is only slightly lower than that of the control sample due to the existence of the HfSiON interlayer.

Gate leakage current is another important device parameter. To evaluate the gate leakage performance of the devices, the *I-V* curve is measured in both accumulation and inversion, as shown in Fig. 3. Oxide charges and especially inter-

TABLE I. Electrical properties of the samples.

Sample	D_{it} (10^{11} cm^{-2} eV^{-1})	V_{fb} (V)	Q_{ox} (10^{11} cm^{-2})	k	CET (nm)
Stack	2.15	−0.11	5.69	19.7	1.51
Control	8.27	−0.20	18.4	20.8	1.40

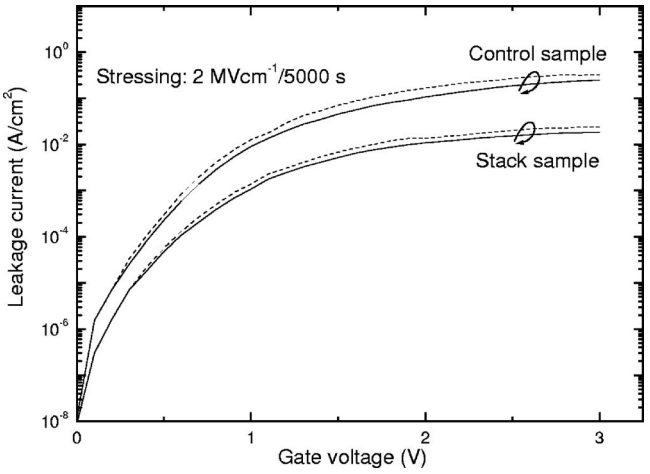

FIG. 4. Increase of gate leakage current after high-field stressing.

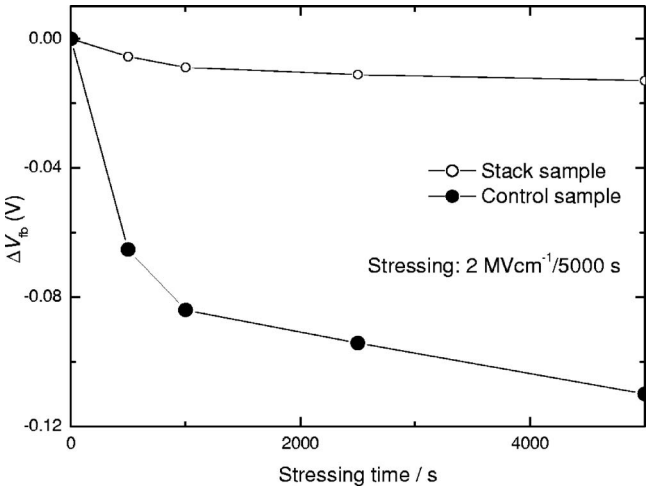

FIG. 5. Shift of flatband voltage (ΔV_{fb}) during high-field stressing.

face states could be responsible for the leakage properties. Owing to its smaller Q_{ox} and D_{it}, the stack sample exhibits lower gate leakage current than the control sample.

A high-field stressing at 2 MV/cm $[=(V_g - V_{\mathrm{fb}})/T_{\mathrm{ox}}$, where V_g is gate voltage] for 5000 s is used to evaluate the reliability of the devices. After stressing, increase of gate leakage current and shift of flatband voltage for the two samples are shown in Figs. 4 and 5, respectively. Obviously, the stack sample has much better reliability than the control sample due to the formation of a hardened oxynitrided interface without titanium silicide.

In summary, MOS device with HfTiON/HfSiON stack gate dielectric is fabricated, and excellent electrical properties are obtained, with lower interface-state/oxide-charge densities, lower gate leakage current, and better high-field reliability, as compared to the control sample without the HfSiON buffer. This is attributed to the HfSiON interlayer which effectively prevents Ti from penetrating to the Si surface, and thus forms an oxynitrided and SiO_2/Si-like interface. Therefore, the HfTiON/HfSiON stack dielectric is a promising technology for preparing high-k gate-dielectric MOS devices with excellent electrical performances.

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