Effects of Sputtering and Annealing Temperatures on MOS Capacitor with HfTiON Gate Dielectric

C.D. Wang, C.X. Li, C.H. Leung and P.T. Lai

Abstract - In this work, Al/HfTiON/n-Si capacitors with different sputtering and annealing temperatures are studied. Larger accumulation capacitance and flat-band voltage are observed for samples with higher sputtering or post-deposition annealing temperature. Gate conduction mechanisms are only affected by sputtering temperature slightly. The flat-band voltage shift and interface-state density at midgap under high-field gate injection and substrate injection are investigated, and the results imply electron detrapping in the gate dielectric.

I. INTRODUCTION

Continual scaling down of microelectronic devices requires ultra-thin gate dielectric, which results in unacceptable current leakage when conventional SiO_2-based gate oxide is used [1]. One solution is to use high dielectric constant (high-*k*) materials as the gate insulating layer [2], by which a physically thicker gate film can be used to significantly reduce the gate leakage while maintaining the same capacitance equivalent thickness.

Many high-*k* dielectrics incorporated on Si substrate have been investigated, such as Al_2O_3 [3], Ta_2O_5 [4], TiO_2 [4], La_2O_3 [5], Y_2O_3 [6], HfO_2 [7], ZrO_2 [8], HfSiON [9], and HfLaON [10]. When applied to Si substrate, however, such materials do not have comparable qualities as SiO_2 in thermal stability and electrically reliability. They either have too small conduction-band offset with Si (like Ta_2O_5 and TiO_2), or have too many fixed charges (like Al_2O_3), or are apt to moisture absorption (like La_2O_3), or have low crystallization temperature (like TiO_2 and Y_2O_3) [11]. Among many candidates, Hf-based high-*k* dielectrics are considered to be the most promising ones when taken overall properties into account [12], with HfTiON having relatively high *k* value.

Several methods have been used to grow gate dielectric thin films, among which sputter deposition is commonly used nowadays as a physical vapor deposition method. As for sputter deposition, temperature is one important parameter which should influence the quality of the thin films. In addition, post-deposition annealing (PDA) is usually conducted after gate film deposition to acquire good dielectric quality. PDA temperature is very critical and should be chosen elaborately, for too low temperature may not be effective to remove defects while too high temperature may result in film crystallization [13]. In this work, the effects of sputtering and PDA temperatures on Al/HfTiON/n-Si MOS capacitor will be studied. The gate leakage mechanism and dielectric reliability under high-field stress will also be investigated.

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II. EXPERIMENTS

(100) phosphorus-doped silicon substrate with resistivity of 0.5 ~ 0.7 Ω·cm was used to fabricate MOS capacitors. The wafers were first cleaned using the standard RCA process, and then were immediately transferred into the chamber of a sputter system. A thin layer of HfTiN (~ 6 nm) was deposited using reactive co-sputtering of Hf and Ti targets in a N_2/Ar ambience at different substrate temperatures: room temperature (RT), 200°C, 300°C and 400°C, respectively. Post-deposition annealing was then conducted in dry N_2 under different conditions (1 minute at 500°C, 600°C and 700°C respectively), where HfTiN was transformed into HfTiON due to residual O_2 in N_2. For comparison, some samples did not receive the PDA treatment. Al with a thickness of 500 nm was evaporated and then patterned as gate electrode with an area of 7.85×10^{-5} cm^2. Finally, a forming-gas anneal was performed at 425°C for 20 minutes to make better electrical contact.

High-frequency capacitance-voltage and gate leakage current characteristics were measured at room temperature using HP4281A precision LCR meter and HP 4156A precision semiconductor parameter analyzer, respectively. Also, high-field stress was imposed to examine the device reliability. The thickness of the dielectric layer was measured using spectroscopic ellipsometry (SE). All the measurements were performed under a dark ambience and electrically-shielded condition.

III. RESULTS AND DISCUSSION

In Fig. 1, it can be observed that the thickness decreases as the temperature of sputter deposition or PDA treatment increases. This is probably because when the substrate is heated at higher temperature during film deposition, surface diffusion of atoms is significantly increased so that better planarization and denser film are accomplished. For the same sputter deposition condition, especially at low deposition temperatures (RT and 200°C), compared with samples without PDA treatment, PDA at 500°C and 600°C can reduce the thickness of dielectric layer significantly. For the samples with PDA at 700°C, a pronounced reduction of dielectric thickness is observed

compared with the samples under other PDA temperatures due to better densification at 700°C.

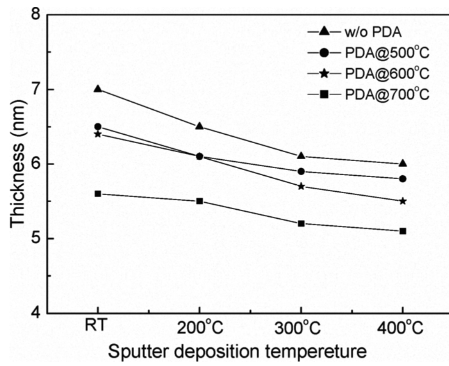

Fig. 1. Physical thickness of dielectric layer for samples with different sputter deposition and PDA temperatures.

High-frequency (1-MHz) capacitance-voltage (C-V) characteristics of the Al/HfTiON/Si MOS capacitors are shown in Fig. 2. As to each panel in Fig. 2(a), for the same sputter deposition temperature, samples with PDA at 700°C have pronounced improvements in device performance, suggesting that the temperatures of 500°C or 600°C are not high enough to remove defects inside the devices. It can also be noticed that for samples with sputter deposition at RT or 200°C, the higher the PDA temperature, the larger the accumulation capacitance is; while for samples with sputter deposition at 300°C or 400°C, the samples without PDA have larger accumulation capacitance than those with PDA at 500°C or even at 600°, which is a direct result of *in situ* annealing effect. As the deposition temperature increases, its *in situ* annealing effect complements the inadequate of the PDA treatment, and thus the difference in accumulation capacitance for the samples in each group is weakened. On the other hand, in each group, larger flat-band voltage V_{fb} is observed for samples with higher PDA temperature suggesting an increase of positive charge trapping or hole trapping at higher PDA temperature. Such V_{fb} trend is different from HfO_2 gate dielectrics annealed in O_2 ambient where V_{fb} shifts negatively first and then shifts positively as the annealing temperature ranges from 550°C to 800°C [13]. In Fig. 2(b), at same PDA treatment, larger V_{fb} is shown obviously for the samples with the higher sputter deposition temperature. Also, it can be found from each panel that higher sputter deposition temperature leads to larger accumulation capacitance.

High-frequency (1-MHz) bidirectional C-V characteristics (not shown) suggest almost no C-V hysteresis (no more than 20 mV) and no kinks near the inversion region for all the samples, indicating there are almost neglectable near-interfacial slow oxide traps [14, 15]. In addition, the bidirectional C-V curves seems almost not affected by different sputter deposition and PDA temperatures, suggesting such near-interfacial slow oxide traps would not be created by *in situ* annealing or PDA treatment in N_2 ambience.

Fig. 3 shows the gate leakage characteristics in accumulation region obtained for samples with PDA at 700°C but with different sputter deposition temperatures. It can be found that higher sputter deposition temperature

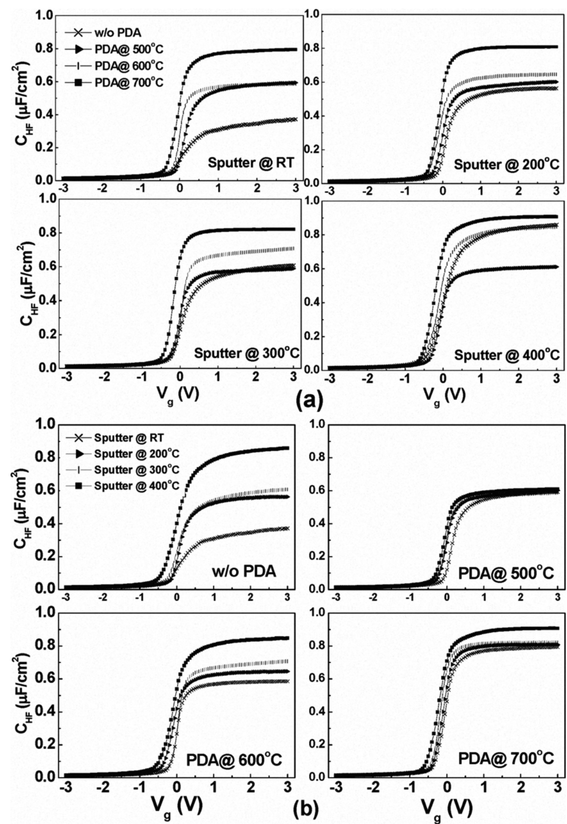

Fig. 2. High-frequency C-V characteristics (1 MHz) of the Al/HfTiON/Si MOS capacitors: (a) each panel shows samples with same sputter deposition temperature but with different PDA treatments; (b) each panel shows samples with same PDA treatment but with different sputter deposition temperatures.

leads to relatively larger gate leakage. The insets of Fig. 3 show the current conduction mechanisms at different voltage regions for the sample with sputter deposition at 400°C. For an electric field less than 0.9 MV/cm, the current can be fitted with the Schottky emission equation, $\ln J_g \propto E^{1/2}$, where E is electric field in the dielectric. For an electric field larger than 0.9 MV/cm, the current can be fitted by direct tunneling, $E \times \ln(J_g/E^2) \propto E^{3/2}$ [16]. Thus, at a low voltage, electrons at the surface of silicon after acquiring enough energy from the electric filed can overcome the potential barrier to form the gate leakage; while at a high voltage, electrons tunneling through the dielectric is the main process resulting in gate leakage. The results are in agreement with the former reports [16, 17]. Other samples have the same conduction mechanisms. By using the electron effective mass data reported [17], the HfTiON/Si barrier height can be estimated coarsely to be in the range of 0.60~0.66 eV when $m^* = 0.1m_0$ is used, while in the range of 0.64~0.70 eV when $m^* = 0.4m_0$ is used, where m_0 is free electron mass, and m^* is electron effective mass in dielectric. The small value of barrier height may be attributed to Ti [1]. It can be noted that different sputter deposition temperatures do not result in large dispersion of barrier height (no more than 60 mV). In addition, the small barrier height should

account for the large gate leakage when HfTiON is used as dielectric layer.

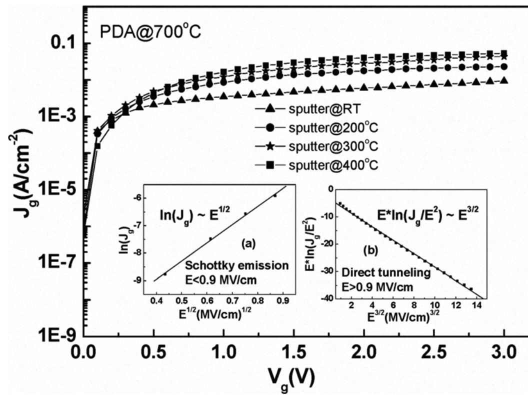

Fig. 3. Gate leakage characteristics at accumulation region obtained for samples with PDA at 700°C but with different sputter deposition temperatures. The insets show current conduction mechanisms at different voltage regions for the sample with sputter deposition at 400°C, where scatters are experimental data, and straight lines are linear fitting.

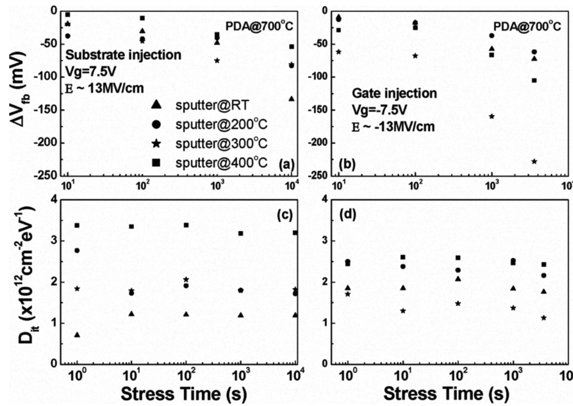

Fig. 4. Flat-band voltage (ΔV_{fb}) and interface state density (D_{it}) at midgap after a constant voltage stress for samples with PDA at 700°C but with different sputter deposition temperatures; (a) ΔV_{fb} and (c) D_{it} are substrate injection, V_g=7.5V; (b) ΔV_{fb} and (d) D_{it} are gate injection, V_g=-7.5V.

The change of flat-band voltage (ΔV_{fb}) and interface-state density (D_{it}) at midgap are studied under high-field stress (~ 13 MV/cm), and the results are shown in Fig. 4. A negative shift of V_{fb} is observed for the devices under gate injection (V_g = -7.5 V), which is consistent with other works [18-20]. This is probably due to hole trapping or electron detrapping, or less efficient electron trapping than hole trapping. On one hand, new traps for holes may be created under high-field due to stoichometry variation [21] or strained bonds [22] or other unknown defects. On the other hand, it has been demonstrated that electron detrapping through tunneling is very effective in the high-filed range [23], and the cross section for electrons captured by holes decreases strongly at high electric filed [18]. Thus, although both electron and hole injection occur under gate injection, the trapped holes are not likely to be neutralized when a large amount of electrons flow through dielectric. To further understand the mechanism, substrate injection is also studied by which a positive biased voltage (V_g = 7.5 V) is applied to the gate. It is noticed that the V_{fb} still shifts negatively as the stress time increases. Since only electrons are injected from substrate under substrate injection due to lack of holes in the metal electrode, the negative shift of V_{fb} is more likely attributed to electron detrapping. For both gate injection and substrate injection, D_{it} at midgap after each stress period is extracted from high-frequency C-V trace by the Terman's method [24]. For each case, D_{it} is almost independent of stress time and remains nearly constant for each sample, implying that very few interface states are generated by the high-field stress. The characteristics of D_{it} at midgap seem not influenced significantly by different sputter deposition temperatures since their values are in the same order for all the samples studied.

IV. CONCLUSION

Al/HfTiON/n-Si capacitors with different sputtering and annealing temperatures are fabricated and investigated. The results show that higher sputter deposition or PDA temperature reduces the physical thickness of dielectric layer, and also leads to larger accumulation capacitance and larger flat-band voltage as well. 500°C or 600°C are not high enough for PDA treatment while 700°C can significantly improve the device performance. Negligible C-V hysteresis is observed for all the samples. Leakage characteristics show that the gate conduction is governed by Schottky emission at low filed and direct tunneling at high filed. Higher sputter temperature results in slightly smaller barrier height and thus relatively larger gate leakage. Negative flat-band voltage shift and almost constant interface-state density under high-field gate injection and substrate injection indicate electron detrapping in the gate dielectric.

ACKNOWLEDGEMENT

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