Optimization of N Content for Higk-*k* LaTiON Gate Dielectric of Ge MOS Capacitor

H. X. Xu, J. P. Xu*, C. X. Li, L. Liu, P. T. Lai*, C. L. Chan

***Abstract* - Thin LaTiON gate dielectric is deposited on Ge (100) substrate by reactive co-sputtering of La_2O_3 and Ti targets under different Ar/N_2 ratios of 24/3, 24/6, 24/12, and 24/18, and their electrical properties are investigated and compared. Results show that the LaTiON gate-dielectric Ge MOS capacitor prepared at an Ar/N_2 ratio of 24/6 exhibits highest relative permittivity, smallest capacitance equivalent thickness, and best electrical characteristics, including low interface-state density, small *C-V* hysteresis and low gate leakage current. This is attributed to the fact that a suitable N content in LaTiON can effectively suppress the growth of low-*k* GeO_x interfacial layer between LaTiON and Ge substrate.**

I. INTRODUCTION

As Si-based metal-oxide-semiconductor field-effect transistor (MOSFET) is approaching its limit, germanium MOSFETs with high relative permittivity (high *k*) gate dielectrics are extensively discussed as alternative candidates for future CMOS technology. La_2O_3 is considered as one of the most promising high-*k* materials due to its large bandgap (5 ~ 6 eV) [1-2], relatively large *k* value (~25) [2-4], high electrical breakdown field strength and good thermal stability [1, 5] when contacting with Si. Recently, it was reported that La_2O_3 thin film also showed many advantages when contacting with Ge, including low interface-state density, very small frequency dispersion and hysteresis due to formation of a stable lanthanum germanate [6-8]. However, a relatively low permittivity for lanthanum germanate due to Ge diffusion into high-*k* dielectric prevents further decrease in equivalent oxide thickness [7].

Ti addition has been studied by several groups to increase the permittivity of Hf-based oxide because of the extremely high relative permittivity of Ti-based oxides (~80) [9-10]. Higher permittivity has been obtained with Ti increase while leading to gate leakage current increase [11]. On the other hand, N incorporation in HfO_2 results in beneficial characteristics including reduction of gate leakage current, improved thermal stability of the dielectric material, due to suppression of the onset of crystallization [12-13]. In view of of the two effects, it is expected that good properties can be achieved by simultaneously incorporating Ti and N into La_2O_3 thin film, when suitable Ti and N contents are chosen. In this work, Ge MOS capacitors with LaTiON thin gate dielectrics deposited under various Ar/N_2 ratios (24/3, 24/6, 24/12, and 24/18) are fabricated and the impacts of N content on their electrical properties are examined. It is found that the *k* value, interface-state density, gate leakage current and C-V hysteresis of these MOS capacitors strongly depend on the N content in the LaTiON film. When N content is controlled at a suitable value, good electrical properties can be obtained for the MOS devices.

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TABLE I
PREPARETION CONDITIONS AND N CONTENT in LaTiON FILMS

Ar/N_2 flow ratio	Ti-target power (W)	La_2O_3-target power (W)	physical thickness (nm)	N content (%)
24/3	17.4	30	7.59	11.5
24/6	17.4	30	7.55	12.9
24/12	17.4	30	7.62	13.5
24/18	17.4	30	7.65	14.8

Note: N percentage is evaluated by comparing the growth rate of LaTiON film with that of LaTiO film deposited at the same powers of La_2O_3 and Ti targets and the same Ar flow rate.

II. EXPERIMENTS

Ge substrate used was Sb-doped *n*-type Ge (100) wafers with a resistivity of 0.10 ~ 0.11 Ωcm. The wafers were cleaned in organic solvents, and lastly with de-ionized water rinsing followed by 30-s diluted HF (1:50) dipping for several cycles to remove the native oxide, leaving a H-terminated surface. After drying in N_2, LaTiON thin film was deposited by reactive co-sputtering of La_2O_3 and Ti targets at different Ar/N_2 ratios of 24/3, 24/6, 24/12, and 24/18 with fixed Ar flow rate of 24 sccm at room temperature. The powers of La_2O_3 and Ti targets were fixed at 30 W and 17.4 W, respectively, for all the Ar/N_2 ratios. A post-deposition annealing (PDA) was carried out in N_2 ambient with a

flow rate of 500 ml/min at 500℃ for 5 min. Subsequently, Al was evaporated and patterned by lithography as gate electrodes with an area $A = 7.85\times10^{-5}$ cm^{-2}, followed by a forming-gas annealing (FGA) at 300 °C for 20 min. High-frequency (HF, 1-MHz) capacitance-voltage (*C-V*) curves were measured by HP4284A precision LCR meter. Gate leakage current was measured by HP4156A precision semiconductor parameter analyzer. Physical thickness of the gate dielectrics was determined by a multi-wavelength ellipsometer and TEM.

III. RESULTS AND DISCUSSION

To determine the thickness and structural aspects of the LaTiON films, high-resolution transmission electron microscopy (TEM) image is taken and depicted in Fig.1 for the sample with an Ar/N_2 ratio of 24/6. From the image, it can be found that the physical thickness of the LaTiON gate dielectric is ~ 7.55 nm, which is consistent with that (~ 7.50 nm) measured by ellipsometer. Thus, the growth rate of the LaTiON film can be determined to be ~ 0.5 nm/min for the samples. It can be seen that negligible interfacial layer between the high-k dielectric and Ge substrate can be observed. This should be ascribed to the inhibiting effect of the incorporated N in the dielectric against O and Ge inter-diffusions, and thus suppressing the growth of interfacial layer at the surface of the Ge substrate [14].

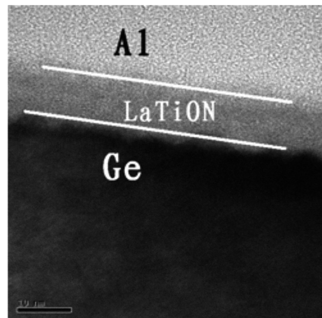

Fig. 1 TEM image of LaTiON/Ge cross section prepared at an Ar/N_2 ratio of 24/6.

Typical HF *C-V* curves measured at 1-MHz frequency for the LaTiON gate-dielectric MOS capacitors prepared under different Ar/N_2 ratios are shown in Fig. 2. The capacitor prepared at an Ar/N_2 ratio of 24/6 exhibits the largest accumulation capacitance (C_{ox}). This result suggests that the N content in LaTiON film prepared at the Ar/N_2 ratio of 24/6 is optimal for suppressing the growth of low-*k* germinate and germanium oxide on the Ge substrate. Thus, it can be reasonably speculated that the LaTiON film deposited under a high Ar/N_2 ratio (higher than 24/6, implying a small N_2 flow rate) would give an insufficient N corporation in the dielectric film, and thus could not effectively block the inter-diffusions of O and Ge, resulting in the formation of a thicker low-k GeO_x interfacial layer. On the other hand, for small Ar/N_2 ratio (lower than 24/6), i.e. large N_2 flow rate, a high concentration of N plasma species react with the Ge substrate and too much N may produce interfacial strain, giving rise to the growth of germanium oxide [15], and hence a thicker GeO_x interfacial layer. Fig. 3 displays the relative permittivity (*k*) and capacitance equivalent thickness (*CET*) for the samples. Corresponding to the C_{ox}, the LaTiON film deposited at an Ar/N_2 ratio of 24/6 has the largest *k* value and smallest *CET*.

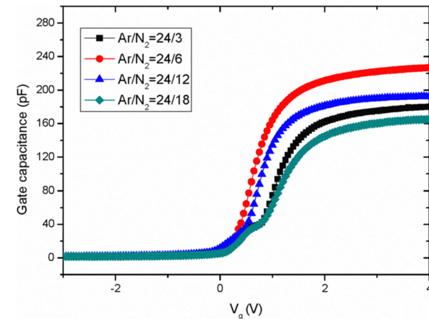

Fig. 2 High-frequency (1-MHz) *C-V* curve of the LaTiON gate-dielectric MOS capacitors prepared at various Ar/N_2 flow ratios.

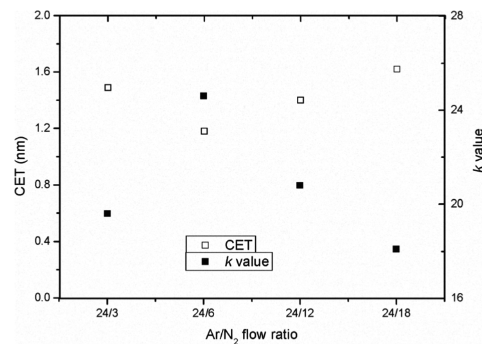

Fig. 3 Capacitance equivalent thickness (*CET*) and relative permittivity (*k*) of the LaTiON gate dielectrics prepared at various Ar/N_2 flow ratios.

Interface-state density (D_{it}) near midgap and equivalent oxide-charge density (Q_{ox}) of the LaTiON films prepared under various Ar/N_2 ratios are shown in Fig. 4. The flatband voltage (V_{fb}) of MOS capacitor is generally determined by the metal-semiconductor work function difference and the oxide charges. The positive shift of V_{fb} in the *C-V* curves, as shown in Fig.2, is indicative of negative Q_{ox} in the LaTiON gate dielectric, which probably originates from the acceptor-like interface and near-interface traps generated mainly by the Ge diffusion from the substrate to the high-*k* layer. The larger Q_{ox}'s for those LaTiON films deposited under large or small Ar/N_2 ratio than that deposited at an Ar/N_2 ratio of 24/6 should be related to more acceptor-like interface and near-interface traps in their thicker interfacial layer. The D_{it} is extracted from the 1-MHz *C-V* curve using the Terman's method [16] for the purpose of comparison. The interface states arise from the presence of dangling bonds and/or defects at the dielectric/Ge interface. The samples prepared under small or large Ar/N_2 ratio introduce more defects at/near the dielectric/Ge interface due to the growth of thicker low-*k* GeO_x interfacial layer, resulting in higher D_{it}, which is demonstrated by the distortion of the *C-V* curves

in the weak inversion region (see Fig. 2). The hysteresis of the *C-V* curve is measured by sweeping in both directions and hysteresis voltages of the samples are shown in Fig. 4. The hysteresis results from the trapping and detrapping of charges at slow states or deep-level traps while sweeping back and forth over the voltage range. Obviously, a large hysteresis occurs in the LaTiON films deposited under small or large Ar/N_2 ratio, implying the presence of a large amount of defects in the dielectric films. Again, small hysteresis is observed for the sample deposited at an Ar/N_2 ratio of 24/6, indicating largely reduced defects due to appropriate N incorporation in the LaTiON film.

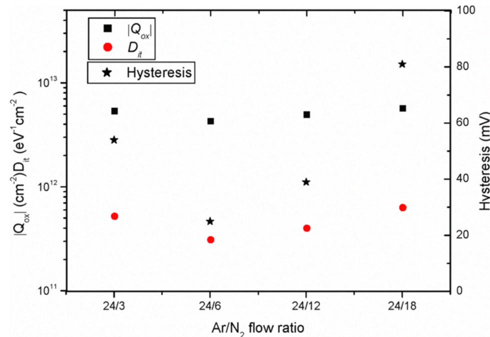

Fig. 4 Equivalent oxide-charge density (Q_{ox}), interface-state density (D_{it}) and *C-V* hysteresis of the samples.

The gate leakage properties of the LaTiON gate-dielectric MOS capacitors deposited under different Ar/N_2 ratios are illustrated in Fig. 5. At a gate voltage of 1 V, the gate leakage current density of the MOS capacitor prepared under an Ar/N_2 ratio of 24/6 (even with the thinnest physical thickness of gate dielectric) is lower than those of the other samples. This is ascribed to its less defects at the interface and in the dielectric film, and thus less leakage paths created, due to suitable N incorporation in the LaTiON film for effectively suppressing the growth of low-*k* GeO_x interfacial layer between the Ge substrate and gate dielectric, as mentioned above.

IV. SUMMARY

Ge MOS capacitors with LaTiON as gate dielectric deposited at various Ar/N_2 ratios (24/3, 24/6, 24/12, and 24/18) have been fabricated, and the impacts of N content in the LaTiON film on the electrical properties of MOS capacitors have been investigated. A turnaround of the electrical properties with increase of Ar/N_2 ratio is found, with an optimal Ar/N_2 ratio of 24/6. This implies that there exists an optimal N content for LaTiON used as gate dielectric, at which the deposited film can effectively suppress the growth of low-*k* GeO_x interfacial layer due to suitable N incorporation in the LaTiON film, leading to less defects at the interface and in the dielectric film. In our case, the LaTiON gate-dielectric Ge MOS capacitor prepared at an Ar/N_2 ratio of 26/4 exhibits increased *k* value, decreased *CET*, improved interface quality, low gate leakage current and small *C-V* hysteresis.

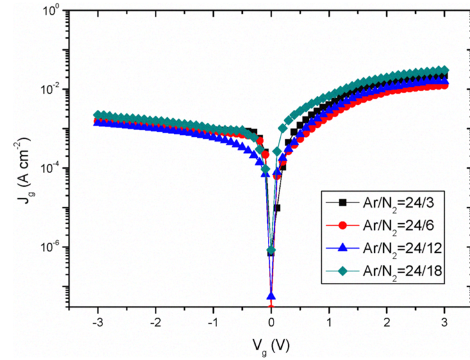

Fig. 5 Gate-leakage current density (J_g) of the LaTiON gate-dielectric Ge MOS capacitors prepared at different Ar/N_2 flow ratios.

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