

A Thermal Simulation Process Based on Electrical Modeling for Complex Interconnect, Packaging, and 3DI Structures

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Abstract—To reduce the product development time and achieve first-pass silicon success, fast and accurate estimation of very-large-scale integration (VLSI) interconnect, packaging and 3DI (3D integrated circuits) thermal profiles has become important. Present commercial thermal analysis tools are incapable of handling very complex structures and have integration difficulties with existing design flows. Many analytical thermal models, which could provide fast estimates, are either too specific or oversimplified. This paper highlights a methodology, which exploits electrical resistance solvers for thermal simulation, to allow acquisition of thermal profiles of complex structures with good accuracy and reasonable computation cost. Moreover, a novel accurate closed-form thermal model is developed. The model allows an isotropic or anisotropic equivalent medium to replace the noncritical back-end-of-line (BEOL) regions so that the simulation complexity is dramatically reduced. Using these techniques, this paper introduces the thermal modeling of practical complex VLSI structures to facilitate thermal guideline generation. It also demonstrates the benefits of the proposed anisotropic equivalent medium approximation for real VLSI structures in terms of the accuracy and computational cost.

Index Terms—Equivalent thermal conductivity, finite difference method, interconnects, Joule heating, packaging, resistance solver, thermal analysis, three-dimensional integration (3DI), very-large-scale integration (VLSI).

I. INTRODUCTION

ALTHOUGH the power of silicon devices is still dominant in the total on-chip power consumption, Joule heating due to current flow in on-chip interconnect, packaging and 3DI (3D integrated circuits) vias is becoming more important. Due

to shrinking dimensions, both wire current density and effective copper resistivity are rising [1]–[3]; this will further increase Joule heating. Secondly, the thermal resistances from metal wires to the silicon substrate are higher due to the inclusion of more metal layers and lower permittivity insulating materials in the backend [3]–[5]. Thirdly, to improve the VLSI performance and heterogeneous integration of technologies on a single die, 3D integration technologies are being pursued [6], [7]. Because device layers are stacked on top of each other, 3DI faces more serious thermal challenges [8]. The Joule heating in interconnects leads to an additional temperature rise over the junction temperature or the temperature near the silicon surface. On the other hand, the heat from device layers has serious implications for temperatures of all interconnect layers. Moreover, vias in the backend stack or the through-silicon-vias (TSV) connecting different strata in 3DI function as heat pipes. Their thermal performance optimization could affect the electrical requirement. Hence, many reliability degradations could easily be underestimated, such as temperature dependent electromigration, stress migration, and inter-metal dielectric leakage [5]. In addition, the temperature profile is important to signal integrity and timing analysis [9].

Efficient thermal analysis in complex VLSI problems with the consideration of every entity (such as wires, vias, substrate, and multiple dielectrics) has not been demonstrated. Most methodologies used by industries are implemented in standalone tools, which can only handle relatively small size problems and are difficult to integrate with existing EDA design flows [3], [10], [11]. Some methods use approximate analytical models for thermal analysis [3], [12]–[16]. Although one can obtain results quickly through these analytical models, certain deficiencies must be resolved. The analytical model in [12] was derived from the conformal mapping method. But the model is only valid for a single wire, which is not the case in VLSI on-chip interconnects. In [13], an analytical approach was proposed for some typical interconnect structures. But the objective structures are not complicated enough to deal with complex Manhattan structures. In [14]–[16], an analytical solution for embedded wires with vias at both ends was derived. But these works did not consider vias in other interconnect topologies (e.g., each power wire has typically more than two connected vias, which are not only set at the ends but also along the length). Also, as mentioned in [3], the thermal resistance model of parallel interconnect arrays intentionally neglects fringing heat dissipation, which leads to inaccuracy.

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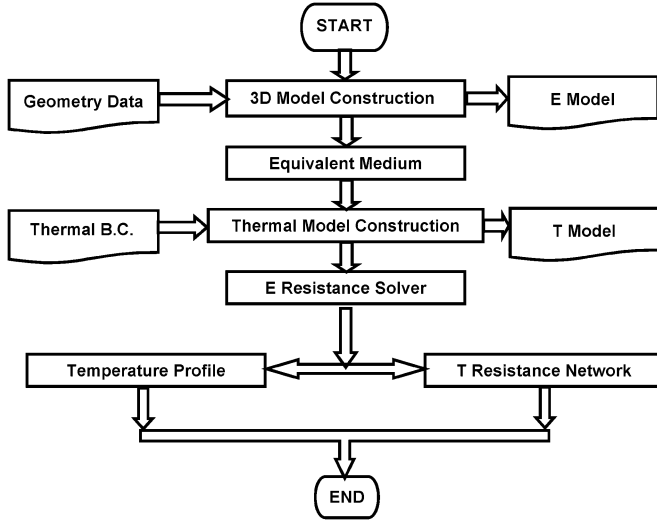


Fig. 1. Flowchart illustrating various steps in the 3D thermal simulation using an electrical (resistance extraction) solver.

Recently, a methodology was developed which exploits the well known analogy between electrical and thermal problems [17]. It produces a general fast 3D thermal analysis engine for on-chip interconnect, packaging and 3DI using an existing electrical resistance extraction tool [18]. Naturally it is compatible with the IC design environment, where electrical analysis is dominant. However the approximation in [17] that treats the power consuming wire as a single equal potential port is not valid if the temperature gradient along the wire cannot be ignored. To solve this issue, the nonequal potential port is introduced. This paper further pursues a novel and accurate empirical model to allow isotropic and anisotropic equivalent media to replace the noncritical region details with minimal error. Thermal analysis of realistic and complex interconnect stacks using proposed methods are subsequently demonstrated.

II. THERMAL SIMULATION METHODOLOGY

A brief workflow of the proposed method is shown in Fig. 1. It starts from obtaining layout geometries and material properties. A model for electrical analysis (E Model) is generated. If the problem size is too large, noncritical details are replaced by equivalent media. Then thermal boundary conditions, such as heat sources and heat sinks, are added to form a thermal model (T Model). Using an electrical resistance solver [18], the thermal model is processed by an electrical resistance solver to generate either the temperature profile or the thermal resistance network in the SPICE net list.

The basic idea behind the methodology is based on the equivalence between the static electrical Laplace equation and the steady state heat conduction equation. The first one is expressed as

$$\nabla \cdot J_{el} = \nabla \cdot (-\sigma_{el} \nabla \phi) = 0 \quad (1)$$

where J_{el} is the electrical current density, σ_{el} is the electrical conductivity, and ϕ is the electrical potential. The heat conduction equation is written as

$$\nabla \cdot J_{th} = \nabla \cdot (-\kappa_{th} \nabla T) = p \quad (2)$$

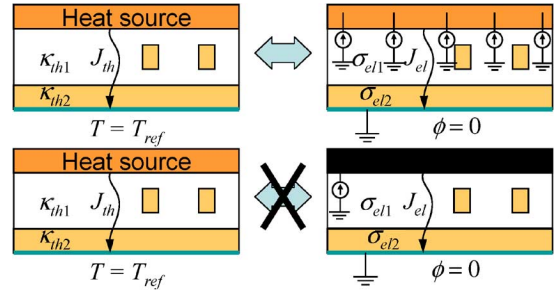


Fig. 2. The analogy between electrical and thermal problems in terms of the heat density boundary condition setup. Top: correct way. Bottom: incorrect way.

where J_{th} is the heat flux density, κ_{th} is the thermal conductivity, T is the temperature, and p is the heating power density. It is clear that T is analogous to ϕ , J_{th} is analogous to J_{el} , and κ_{th} is analogous to σ_{el} ; the thermal resistance is analogous to the electrical resistance.

Thermal boundary conditions are realized using electrical sources in the resistance solver. There are several important thermal boundary conditions that have to be replaced by limited source options. The constant temperature boundary condition, the most popular one for ambient temperature setups, is represented by a voltage source. If only the current source is allowed in the resistance solver, a very small parallel resistor has to be added to create a voltage source. Another boundary condition is the heat density per unit area, which can be easily replaced by the current source. However, because of limited thermal conductivities, the nonequal potential (temperature) distribution has to be guaranteed. Hence, a distributed current sources (Fig. 2, top) instead of one (Fig. 2, bottom) is added to enable the heat density boundary condition. The third thermal boundary condition is the Joule heating boundary condition. Obviously it is a function of wires' resistivity and current. Its implementation needs the precalculation of consumed power of metal segments and then sets the heat density boundary condition according to current directions.

Hence, it is feasible to develop a fast thermal analysis engine for on-chip interconnect, packaging, and 3DI using existing electrical resistance solvers. There is another reason driving this effort: the thermal-electrical coupling effect. The temperature rise increases the material resistivity according to the temperature coefficient of resistance (TCR). This changes the current distribution and power consumption (Joule heating) inside conductors. In return it alters the temperature profile. Hence, the workflow in Fig. 1 shall be a closed loop instead of an open loop. The temperature profile output must be fed back to update the material property. New power consumption of wire segments must be modified. An iterative process is required for a true steady state result if Joule heating is central to the problem [19], where significant changes in the results during the closed loop iteration process were observed. Because we are using the same solver, meshing and solving processes could be correlated and optimized easily. Hence, a unified solver is preferred.

An electrical resistance solver (IBM RGEN) using the finite difference method (FDM) is employed for the proposed thermal analysis. According to Fig. 1, IBM RGEN generates the voltage profile to replace the temperature distribution. IBM

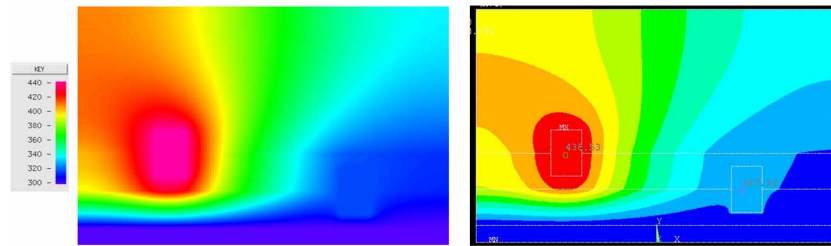


Fig. 3. Simulation results using RGEN [18] and C-tool for a 2D wire structure. Left: 2D temperature profile obtained from IBM RGEN. Right: 2D temperature profile obtained from C-Tool.

TABLE I
SIMULATED TEMPERATURE COMPARISON FOR FIG. 3

	IBM RGEN (K)	C-Tool (K)
Left Wire	437.89	438.53
Right Wire	317.29	317.33

RGEN uses orthogonal meshes. Since Manhattan style VLSI structures are typically rectangular, the orthogonal basis is expected to be more efficient than the tetrahedron, which is used by the finite element method (FEM) in many commercial softwares. To further improve the efficiency, the projection gridding is used. The projection gridding fits the physical heat conduction path better than tetrahedron shape meshes. Hence, there are less rectangular cells than tetrahedrons in a unit volume for VLSI.

Interestingly this method can be easily applied to 2D type thermal analysis. It is very useful for preliminary canonical BEOL thermal performance characterization. Fig. 3 shows a validation of 2D simulation case [17] when the result of this method is compared with that of a popular commercial tool (anonymously named as C-Tool [3], [11]). Two wires buried inside a three-layer dielectric structure on top of a ground plane (heat sink) were injected with 10 W power each. To make the problem more general, each wire sits through a dielectric boundary. The temperature profiles from both methods are highly identical to each other. The wire temperatures given in Table I. show that the IBM RGEN method is generating very close results as C-Tool.

Using this method, a 2D 45-nm stack was analyzed to understand the temperature rise of power wires when their neighboring signal wires are simultaneously switched on. Quiet wires are named as dummy lines in this test, as shown in Fig. 4 [17]. Artificial vias are added in between the dummy wires and the ground heat sink. The worst case is defined as the situation in which there is no metal fill below and above the metal layer under investigation, and there is no via connection at all. Fig. 5 shows the temperature rise of relevant power wires versus the number of heated signal wires. It is obvious that 1) the worst cases are significantly different from real situations when there are many metal fills between the interested metal layer and the heat sink; 2) vias guide a lot of heats down to the ground.

It is natural to extend this method from 2D simulation to 3D. However, even though the port setups follow the same principles as 2D, more careful considerations have to be taken into account. It is quite often that a copper plane is required to be the constant temperature surface, or a plane with constant power

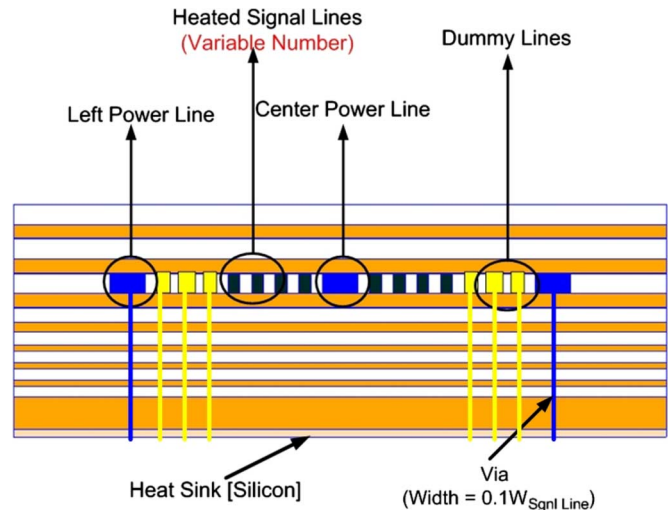


Fig. 4. 2D 45-nm stack profiles with the definitions of heated signal lines, dummy lines, power lines, and artificial vias.

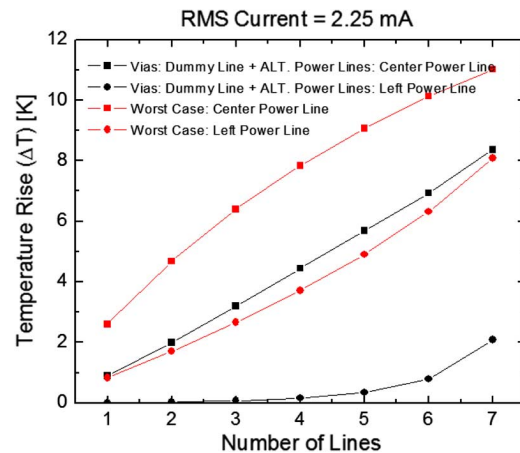


Fig. 5. Power wire temperature rise versus the number heated signal wires in the 2D 45-nm stack defined in Fig. 4.

distribution. But it is very easy to get errors in the results without proper port setups.

One testing case to show these concerns is to use multiple heaters and multiple heat sinks. As shown in Fig. 6, a straight copper wire buried in a multilayer structure which has a ground plane on its back acting as the heat sink. If we assume that the copper wire is the heater with constant temperature, we can put one or multiple heaters on its top surface. Similarly, we can put

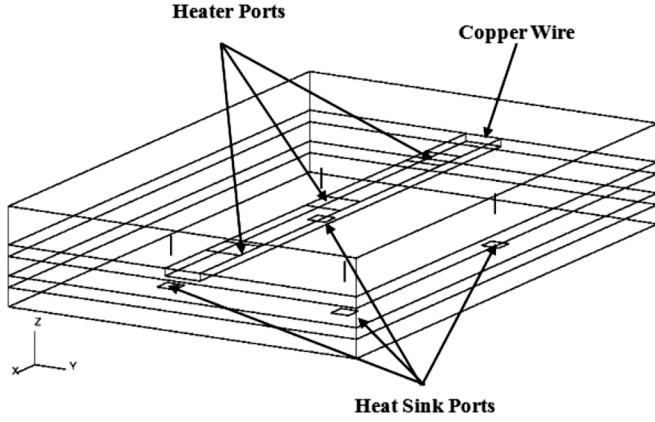


Fig. 6. Port effect testing case. A straight copper wire is put inside a five-layer dielectric structure. A ground plane supports the bottom of it. Four vertical narrow vias are used to disturb the heat conduction. Heater ports are set on the top surface of the copper wire. The heat sink ports are set at the bottom ground plane surfaces. They are all in the shape of small rectangular patches.

TABLE II
PORT SETUP EFFECTS

Case Number	Heater Port Number	Sink Port Number	Thermal Resistance (K/W)
1	1	1x1	52.63
		2x2	52.60
		3x3	52.26
2	2	3x3	46.73
	3	3x3	45.79
	4	3x3	45.52
<i>Set the thermal conductivity of copper wire to be 40000 W/m-K</i>			
3	1	3x3	45.4

multiple heat sink ports at the bottom ground plane. By investigating different combinations of heater ports and heat sink ports as shown in Table II, it is found that more ports generate better results. The reason is that the copper planes (both the signal wire and the ground plane) have finite thermal conductivity. For the case there is only one heater port set, the temperature of other surfaces on the copper wire will be computed out. Due to the finite thermal conductivity, they will have different temperature distributions. This actually made the wire or surface non equal potential, which will not satisfy the constant temperature boundary condition. There are two ways to solve this issue: 1) cover the whole constant temperature surface using one or more ports seamlessly; 2) artificially increase the thermal conductivity of the corresponding surface. In the last row of Table II, even the single heater port setup is able to achieve satisfactory solution because the copper wire's thermal conductivity was increased to 40 000 W/m-K.

However, for the power density boundary condition, nonequal potential is important. For example, if the uniform current flows through one uniform copper wire, the heat power density generated due to the Joule heating is homogeneous along the wire. However, depending on the ambient setups, the temperature at different location of the wire will be different. Besides the Joule heating boundary condition, the constant power density boundary condition can be used (this boundary condition is more useful for device layers). The common point of the Joule

heating and constant power density boundary conditions is that the temperature across the whole boundary is different. Therefore, as explained in Fig. 2, the electrical resistance solver has to be carefully tuned to guarantee this point.

A 3D validation was also conducted found excellent accuracy compared to C-tool. From [20], it was seen that to achieve the same accuracy, RGEN based analysis is much faster than C-tool. Meanwhile our proposed methodology can be easily integrated with VLSI EDA workflows. Actually this work has been implemented into our cross-platform 3DI thermal map generation flow smoothly and seamlessly.

III. CLOSED-FORM THERMAL MODEL AND EQUIVALENT MEDIUM APPROXIMATION

To further reduce the computation time and memory usage, an equivalent medium with effective thermal conductivity κ_{eff} can be used to replace the detailed metal fills in noncritical regions. This idea was also introduced in [3] and [14]. However, those analytical models are not comprehensive enough for practical needs.

The model in [3] is based on series and parallel thermal circuit approximations. It divides the structure by layers, assuming a parallel thermal circuit within a layer and series thermal circuits between layers. Every layer has its own effective thermal conductivity as shown in Fig. 7. The effective inter-layer dielectric (ILD) thermal conductivity is written as

$$\kappa_{\text{ILD,eff}} = f\kappa_{\text{via}} + (1 - f)\kappa_{\text{ILD}} \quad (3)$$

where f is the via density defined by the ratio of the via volume to the ILD volume. The thermal resistance R_{w2g} per unit length between two metal wire layers is expressed as

$$R_{w2g} = \frac{1}{\kappa_{\text{ILD,eff}}} \frac{t_{\text{ILD}}}{w + d} + \frac{1}{\kappa_{\text{IMD,eff}}} \frac{t_{\text{wire}}}{w + d} \quad (4)$$

where $\kappa_{\text{IMD,eff}}$ is the effective metal wire layer (IMD) thermal conductivity, t_{ILD} is the distance between wire and ground, t_{wire} is the wire thickness, w is the wire width, and d is the wire spacing. In general, $\kappa_{\text{IMD,eff}} \gg \kappa_{\text{ILD,eff}}$. Hence, we have

$$R_{w2g} \approx \frac{1}{\kappa_{\text{ILD,eff}}} \frac{t_{\text{ILD}}}{w + d} \quad (5)$$

which says that the unit area thermal resistance $(w + d) R_{w2g}$ between two metal wire layers is nearly independent from w , d , and t_{wire} . This is definitely not true particularly when wires are not closely packed ($d > w$). R_{w2g} is underestimated in this approach.

Another analytical approach [14] assumes that the problem can be divided into two regions: in one region the heat transfers downward and laterally, while in another region the heat only transfers downward. However, this approach ignores the fringing heat dissipation. Therefore it overestimates R_{w2g} particularly when wires are not closely packed ($d > w$).

Our model is based on the fact that the electrostatic and thermal problems have similar physical nature. The electrostatic Poisson's equation is expressed as

$$\nabla \cdot D = \nabla \cdot (-\epsilon \nabla \phi) = \rho \quad (6)$$

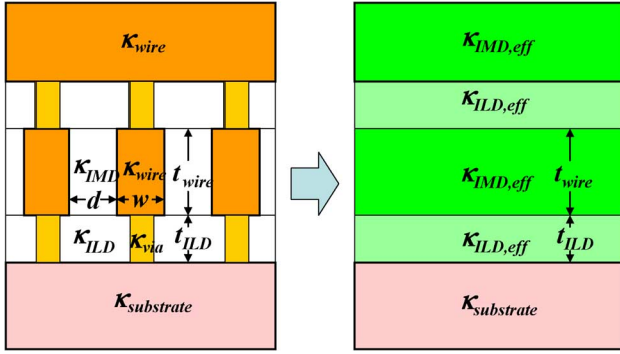


Fig. 7. Layer effective thermal conductivity approach in [3].

where D is the electrical displacement flux, ε is the material permittivity, and ρ is the charge density. The similarity between (2) and (6) shows that the thermal conductance is analogous to the electrical capacitance. But it requires that the majority electric field is within bonding dielectrics if we take advantage of corresponding capacitance problems. Or the analogy will require “0” relative permittivity, which is not physical. Since most VLSI problems have their majority electric fields confined within dielectrics, the interconnect capacitance models can be used for thermal analysis. It indicates that a capacitance solver could help to establish the thermal resistance network under the above assumption, too.

An interconnect capacitance model is shown in Fig. 7. The empirical interconnect capacitance model in [21] is chosen. The wire-to-ground capacitance per unit length (C_{GND}) is written as

$$\begin{aligned} C_{GND}/\varepsilon &= w/t_{ILD} \\ &+ 1.086(1 + 0.68e^{-t_{wire}/1.343d} \\ &\quad - 0.9964e^{-d/1.421t_{ILD}}) \\ &\cdot [d/(d + 2t_{ILD})]^{0.0476} (t_{wire}/t_{ILD})^{0.0337} \\ &= \text{func}(w, t_{wire}, t_{ILD}, d) \\ &\quad (\text{for } 0.3 \leq w/t_{ILD} \leq 10, 0.3 \leq d/t_{ILD} \leq 10, \\ &\quad 0.3 \leq t_{wire}/t_{ILD} \leq 10) \end{aligned} \quad (7)$$

where t_{ILD} is the distance between wire and ground, t_{wire} is the wire thickness, w is the wire width, and d is the wire spacing. It should be noticed that the temperature gradient in metal wires are much lower than that in dielectric due to very high metal thermal conductivity. Substituting C_{GND}/ε with $1/\kappa_{Die}R_{w2g}$, we can get

$$1/\kappa_{th}R_{w2g} = \text{func}(w, t_{wire}, t_{ILD}, d). \quad (8)$$

Hence, the total unit area thermal resistance for a Manhattan interconnect stack can be expressed as

$$\begin{aligned} R_{total} &= \sum_{i=1}^{n-1} [R_{i,no-vias}/(1-f)] \|(A_{i,via}R_{i,via}/f) \\ &+ [R_{n,no-vias}/(1-f)] \|(A_{i,via}(R_{n,via} + R_{n,wire}/4)/f) \end{aligned} \quad (9)$$

where n is the number of metal wire layers, i stands for the i th layer, $R_{i,no-vias} = R_{w2g}(w+d)$ is the unit area thermal resistance between the i th and the $(i-1)$ th wire layers when

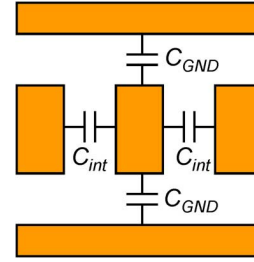


Fig. 8. Schematic plot of the capacitance model with two ground planes.

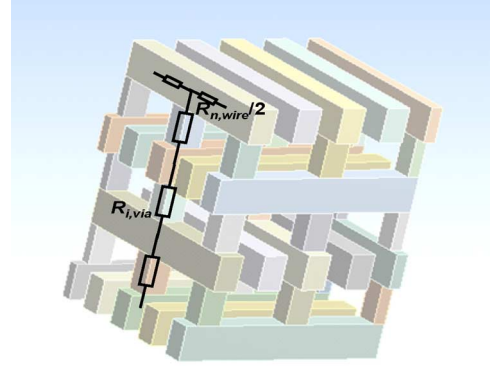


Fig. 9. Schematic plot of a backend interconnect stack (source: [11]).

vias are not considered, $R_{i,via} = (t_{i,ILD} + t_{i,wire})/\kappa_{metal}A_{i,via}$ is the via thermal resistance of the i th ILD layer, $R_{n,wire}$ is the thermal resistance of top layer wire between two vias, $A_{i,via}$ is the via area of i th layer, and f is the via density. The schematic plot of the model structure is shown in Fig. 8.

Using proposed equivalent medium model to replace the non-critical region details of complicated structures, the computational time can be significantly accelerated. In the layered chip structures, the z-direction (orthogonal to the layer surfaces) effective thermal conductivity of combined i th ILD layer and wire layer ($\kappa_{eff,i,z}$) is derived from its unit area thermal resistance

$$R_i = (t_{i,ILD} + t_{i,wire})/\kappa_{eff,i,z}. \quad (10)$$

Hence

$$\begin{aligned} \kappa_{eff,i,z} &= \frac{t_{i,ILD} + t_{i,wire}}{R_i} \\ &\approx \frac{t_{i,ILD} + t_{i,wire}}{[R_{i,no-vias}/(1-f)] \|(A_{i,via}R_{i,via}/f)}. \end{aligned} \quad (11)$$

The effective thermal conductivity of i th ILD layer (not combined with the wire layer) can be expressed as (7).

If the long distance lateral heat transfer is ignorable in a region, the isotropic effective thermal conductivity can be used. Fig. 10 shows an example using this equivalent isotropic medium replacement. The adiabatic boundary condition at the left side makes the structure equivalent to a mirror symmetrical problem. Hence, the width of the GND1 wire is set as half of that of the V_{DD1} . Detailed geometry and material properties are based on an industrial 45 nm process. The thermal contact resistances of vias are also considered to keep the simulation object close to the reality as much as possible. 1 mA current is

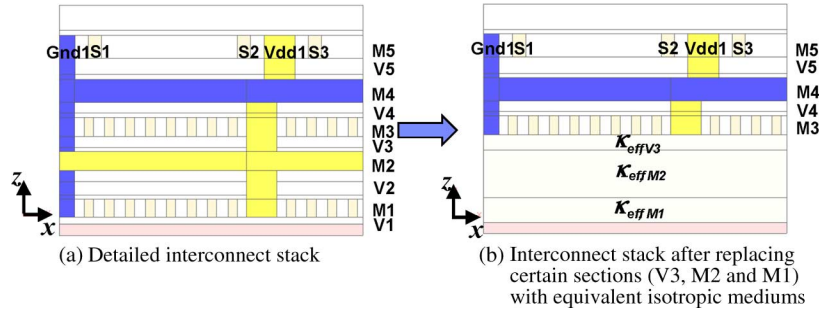


Fig. 10. (a) Vertical cross section of a representative backend stack. (b) The stack after certain sections ($V3$, $M2$, and $M1$) are replaced by equivalent isotropic mediums: $M1 - M5$ stand for five wire layers, while $V1 - V5$ stand for five ILD layers. $S1 - S3$ are signal wires that are treated as heat sources. The structure is $18.24 \mu\text{m}$ long (y -direction, perpendicular to the paper plane) and $2.28 \mu\text{m}$ wide (x direction).

TABLE III
VERIFICATION OF EQUIVALENT MEDIUM APPROXIMATION MODEL
(TEMPERATURES ARE REFERRED WITH RESPECT
TO THE BOTTOM HEAT SINK WITH T_{ref})

	Detailed structure	Using eq-medium	Error
$\Delta T_{\text{avg}, \text{Gnd1}}$ (K)	1.236	1.220	-1.3%
$\Delta T_{\text{avg}, S1}$ (K)	1.651	1.630	-1.3%
$\Delta T_{\text{avg}, S2}$ (K)	1.657	1.640	-1.0%
$\Delta T_{\text{avg}, \text{Vdd1}}$ (K)	1.249	1.241	-0.7%
$\Delta T_{\text{avg}, S3}$ (K)	1.688	1.671	-1.0%
$\Delta T_{\text{avg}, M5}$ (K)	1.383	1.364	-1.4%
$\Delta T_{\text{avg}, M4}$ (K)	0.937	0.912	-2.7%
$\Delta T_{S1, \text{Gnd1}}$ (K)	0.415	0.410	-1.2%
$\Delta T_{S2, \text{Gnd1}}$ (K)	0.408	0.400	-2.0%
$\Delta T_{S3, \text{Gnd1}}$ (K)	0.438	0.430	-1.9%
$\Delta T_{M5, M4}$ (K)	0.446	0.453	1.5%
Computation time	5.8 h	50 min	

TABLE IV
ERROR AND COMPUTATIONAL COST OF THREE CASES IN FIG. 13

	S4		V_{DD}		Computation time (hour)
	ΔT_{max} (K)	Error w.r.t.	ΔT_{max} (K)	Error w.r.t.	
Case 1	5.5767	-	4.4945	-	6.3
Case 2	5.7225	2.61%	4.5763	1.82%	3.2
Case 3	5.5537	-0.41%	4.4746	-0.44%	4.0

applied to signal wires $S1$, $S2$, and $S3$. The bottom reference temperature (T_{ref}) is 0 K.

The sample temperature results are summarized in Table III [20]. Excellent agreement (within 3%) between the equivalent medium approach and the exact direct approach with a 7X saving in the computational time has been achieved.

It is obvious that an equivalent medium with the anisotropic thermal conductivity will give better approximation if lateral heat transfers cannot be ignored. It detail process can be found in [20].

IV. ANALYSIS OF A COMPLEX INTERCONNECT STACK

As a demonstration, a very complex 45 nm technology interconnect stack is analyzed using the method proposed in Fig. 1. A zoomed in view of the simulated structure is shown in Fig. 11(a). The width and length of the structure are $2.28 \mu\text{m}$ ($0 \leq x \leq 2.28 \mu\text{m}$) and $330 \mu\text{m}$ ($-165 \mu\text{m} \leq y \leq 165 \mu\text{m}$), respectively. Seven interconnect layers are included. The self-heating

effect of a practical backend stack can be evaluated by analyzing the thermal profile of this intermediate structure because: (a) a structure with adiabatic boundary condition remains equivalent if it is mirrored to a symmetrical structure and duplicated periodically (this structure can be mirrored to $-2.28 \mu\text{m} \leq x \leq 0$ and duplicated periodically); (b) layer 8 and above have a negligible effect on the thermal profile if the self-heating of fifth layer is studied. In this work, eight signal wires ($250 \mu\text{m}$ long) in the fifth wire layer and their vias are injected with the root mean square (rms) current. The maximum temperatures of an excited signal wire and a neighbor victim V_{DD} wire are monitored. The reason for monitoring the victim V_{DD} is that the power wires (V_{DD} and GND wires) are more vulnerable to electromigration because of polarized current stress [5]. The total number of objects is around 9000. The current in signal wires is obtained through the electrical backend simulation. To drive the signal wire, an inverter with $2.6\text{-}\mu\text{m}$ -wide NMOS and $4.4\text{-}\mu\text{m}$ -wide PMOS is used to drive another inverter with $7.8\text{-}\mu\text{m}$ -wide NMOS and $13.2\text{-}\mu\text{m}$ -wide PMOS. The rms current is not uniform along the wire. This is because more current is required to charge and discharge the interconnect capacitance at the input of signal wires (or at the output of the previous stage CMOS driver). The wire current distribution is shown in Fig. 11(b).

Although the heat dissipation in z direction is well described using the proposed effective thermal conductivity method, it is not yet confirmed whether it is also valid in y direction. Hence, regions of layer $V1$ to $V3$ defined in Fig. 10 are replaced by equivalent media with isotropic effective thermal conductivity. Since they are $40 \mu\text{m}$ away from signal vias, the heat dissipation in y direction is not significant. Details close to signal vias are still maintained. There are about 15 million meshed unknowns for the simulation while the computation time is 6.3 h. The simulation results are shown in Fig. 12. The maximum temperature rise is 5.6 K in the heated signal vias for $S4$ wire. The maximum temperature rise in the victim V_{DD} wire is 4.4 K, which can have significant impact on EM lifetime degradation [5], [10]. The corresponding degradation in the mean time to failure (MTTF) of the victim V_{DD} wire is 19.3% at a junction temperature of 343 K (MTTF at 347.4 K with respect to that at 343 K) according to Black's equation [22] and the activation energy (~ 0.5 eV [23]).

The heat dissipation in y direction is not negligible for regions close to ($< 40 \mu\text{m}$ from) signal vias. For such a situation, equiv-

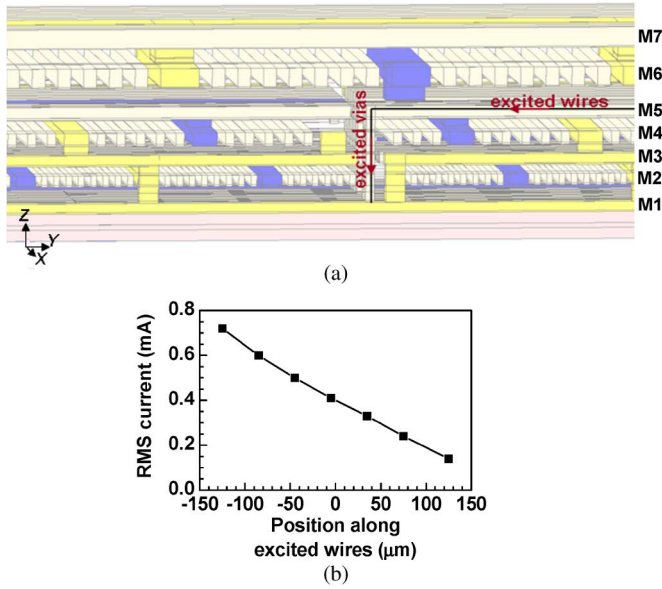


Fig. 11. (a) Zoomed in view of a 45 nm technology backend structure. The monitored V_{DD} wire is from $x = 0 \mu\text{m}$, $y = -125$ to $125 \mu\text{m}$, $z = 1.296 \mu\text{m}$. The monitored S4 wire is from $x = 0.938 \mu\text{m}$, $y = -125$ to $125 \mu\text{m}$, $z = 1.296 \mu\text{m}$. (b) The rms current distribution along the excited signal wires.

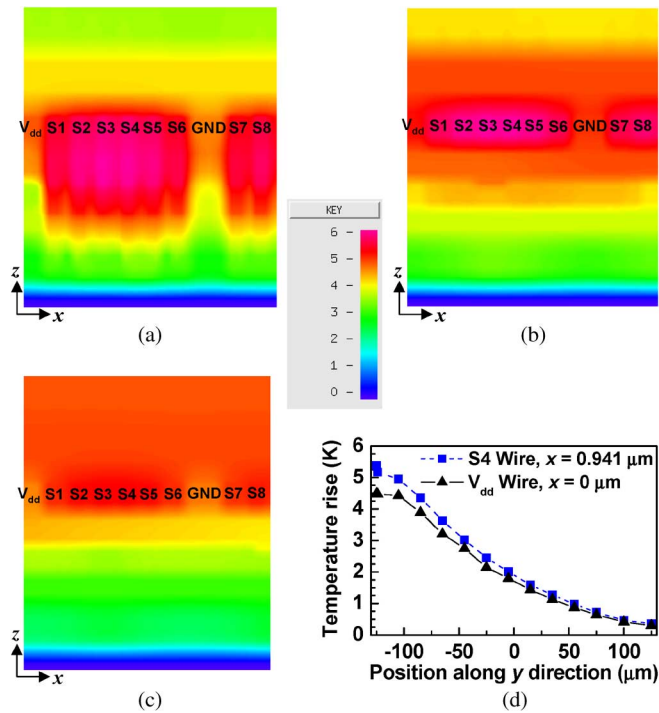


Fig. 12. Cross section of temperature profiles at (a) signal via region ($y = -124.95 \mu\text{m}$), (b) $1 \mu\text{m}$ away from the signal vias ($y = -124 \mu\text{m}$), (c) $30 \mu\text{m}$ away from the signal vias ($y = -95 \mu\text{m}$), (d) the temperature distribution along an excited signal wire with maximum temperature rise ($x = 0.938 \mu\text{m}$) and the victim V_{DD} wire ($x = 0 \mu\text{m}$) in the same metal layer ($M5$ layer). (Temperatures are referred to the bottom heat sink with T_{ref}).

alent media with anisotropic thermal conductivities [20] can be applied. As an accuracy verification, three cases (Fig. 13) are compared: case 1 replaces structures from $V1$ to $V3$ that are $40 \mu\text{m}$ away from signal vias using equivalent isotropic media; case 2 replaces structures from $V1$ to $V3$ that are $1.7 \mu\text{m}$ away

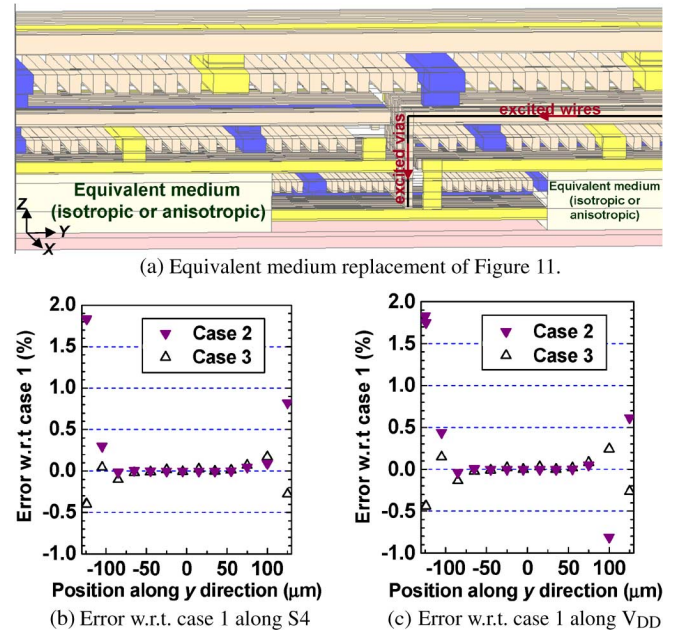


Fig. 13. (a) Backend structure shown in Fig. 11 is modified by equivalent media for regions that are $1.7 \mu\text{m}$ away from signal vias. For both isotropic (case 2) and anisotropic (case 3) replacement, the error with respect to case 1 [Fig. 12(d)] of temperature distribution along, (b) an excited signal wire (S4) with maximum temperature rise ($x = 0.938 \mu\text{m}$), and (c) the victim V_{DD} wire ($x = 0 \mu\text{m}$) in the same metal layer ($M5$ layer).

from the signal vias using equivalent isotropic media; case 3 replaces structures from $V1$ to $V3$ that are $1.7 \mu\text{m}$ away from signal vias using anisotropic media. As shown in Fig. 13(b) and (c), regarding case 1 result as the reference, case 3 shows much better accuracy than that of case 2. Meanwhile, the computation time of case 3 is comparable to case 2.

It should be noted that the temperature rise calculated in the above analysis is only due to the heat generation in $S1 - S8$ wires and vias. In reality, the heat generation of silicon devices and other interconnects also contribute to the temperature rise. The total temperature increase is obtained by superposition of temperature rises due to all heat sources. In other words, if more nearby metal wires are switched on simultaneously, the temperature rise will be greater, which results in worse EM degradation. Our analysis indicates that careful thermal guideline planning is necessary for today's VLSI designs.

V. TEMPERATURE-AWARE EARLY-STAGE CHIP PLANNING

In the early stages of chip planning, there is often flexibility in the placement of logical units, which can lead to improvements in thermal performance. For example, nearby hotspots can be rearranged to reduce the peak temperature. In a conventional (2D) chip design, this optimization is fairly straightforward, since local temperatures are closely related to local power density. Even then, however, the layout engineer's intuition alone may not always produce the best design. As mentioned earlier, 3D design of stacked chips entails many more possibilities, such as overlapping hotspots on successive chip layers, the presence of BEOL wiring in the thermal path, through-silicon vias (TSVs), etc. Therefore, it has become important to provide rapid feedback of local temperatures to layout engineers.

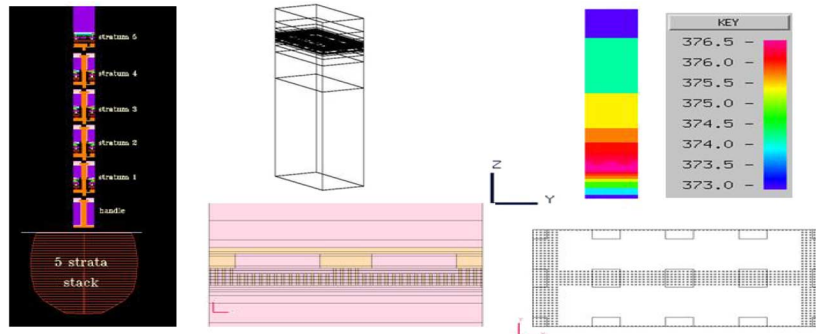


Fig. 14. Study of an eDRAM 3D packaging for the temperature distribution due to the device heating in the eDRAM chip.

Although detailed wiring information is generally not available at the early chip planning stage, previous designs provide good guidance for the specification of BEOL conductivities using the methods described earlier in this work. The underlying solver described above is also flexible enough to enable simple, scripted automation of more complex interconnect structures.

Therefore, the authors have been able to create a design environment, which enables tabular entry of the more common thermal structures and parameters, in addition to high level boundary conditions such as heat sink performance. The user of this design environment does not need to learn a thermal CAD GUI or be concerned with meshing details, as the scripting interface wrappers and underlying solver handle most of these issues automatically.

The circuit designer, as a normal part of the design process, has already specified the circuit placement and associated power dissipation of each circuit element or macro. Depending on the degree of complexity required, estimation of circuit temperatures can be available in as little as a few minutes, enabling multiple iterations in a short time frame. This rough temperature estimation also serves as a guide for designs where one should focus efforts on more detailed optimization and study.

As described above, detailed studies of wire power can be superimposed upon the previous analysis of chip power; many of these more complex models can be evaluated on the time scale of hours. As the design progresses, successively more accurate models can be produced and evaluated.

An eDRAM chip 3D packaging model, part of a stack of several chips, is constructed using ChipJoule automatically in Fig. 14. Chips above and below it are represented by blocks using relevant equivalent thermal conductivities. The device heating is emulated by heat density boundary condition within one layer of the eDRAM. The vertical temperature distribution through a slice, shown in the upper right, is obtained directly from the simulation when both ends of the whole stack are set to be the heat sinks. All the details of the multi-layer eDRAM chip layout were considered in the simulation and Fig. 14 also shows, in the bottom right, the different views of the heated region.

VI. CONCLUSION

In this work, an efficient and accurate thermal profile acquisition method for complex VLSI interconnect, packaging and 3DI

structures is achieved by using purely electrical simulations and modeling approaches. We exploit the existing framework of an electrical resistance solver that is compatible with other VLSI design tools for very complex structures. We then developed a novel accurate and empirical thermal model from the electrical capacitance model. The empirical thermal model has been used to derive the equivalent media to replace complex but non critical regions. Excellent agreement has been achieved by using the proposed methods. As an example, of practical design, the thermal profile of a 45 nm backend interconnect structure was generated. The accuracy of an anisotropic equivalent medium replacement was also verified using this structure.

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