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Tapered sidewall dry etching process for GaN and its applications in device fabrication

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A method of etching which allows the direct interconnection of multiple GaN-based devices is introduced. The mesa structures of devices are etched using an isotropic recipe which produces tapered sidewalls. The degree of inclination can be readily controlled through various etching parameters, which include the inductively coupled plasma power, plate power, and pressure, thus modifying the vertical and lateral etch components. This approach has been successfully adopted in the fabrication of interconnected and matrix-addressable microlight-emitting diodes, and offers superior optical and electrical performance and a high degree of uniformity compared to similar devices fabricated using conventional processes. © *2005 American Vacuum Society.*
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I. INTRODUCTION

The formation of mesa structures in the fabrication of GaN-based photonic devices is commonly achieved through dry etching processes, due to the resistance of the material to wet chemical etching. Of these, inductively coupled plasma (ICP) dry etching has proven to be particularly attractive, offering etch rates of up to $\sim 1\ \mu m$ per minute compared to tens of nanometers per minute for conventional reactively ion etching (RIE).[1] Typically, the etch process should yield high etch rates and selectivities, minimal surface roughening, good reproducibility, and a high degree of anisotropy. All of these properties can be achieved with ICP etching.

Anisotropic etching produces vertical and smooth sidewalls, which is critical for the operation of the edge-emission laser. However, other photonic devices like light-emitting diodes (LEDs) and vertical cavity surface emitting lasers (VCSELs) do not strictly require vertical sidewalls. While nonvertical sidewalls may not make a significant difference to a single device, they can play an important role in the interconnection of multiple devices in an array.

Arrays of microsized LEDs and VCSELs have been demonstrated in recent years,[2,3] as devices which can be used as microdisplays and optical switches in communication networks. Interconnection of individual devices cannot be achieved through direct metal lines, since the metal layer cannot provide satisfactory step-coverage across the sharp-edged mesa structure.

Traditionally, the problem has been overcome by the process of planarization. A sacrificial material is deposited over a surface with uneven topology. This is followed by planarization through dry etching or chemical-mechanical polishing to expose the device regions.[4] While planarization has been adopted for the fabrication of GaN-based devices, it is not without drawbacks. Nonrecoverable damage often forms on the *p*-type GaN surface due to etching or abrasion.[5,6] This manifests itself in the form of degraded electrical and optical properties in the fabricated devices. More importantly, nonuniformity in light emission across the array is often observed.

Consequently, the tapered-sidewall approach is introduced in this article to target this problem. The sidewalls of the individual devices can be made to have an inclination of 20°–45° to the vertical. As a result, conformal step coverage is possible for mesa structures with a height of up to $\sim 5\ \mu m$. Not only can devices can be interconnected directly by metal lines with this process, but improvements to the planarization scheme can also be achieved, as void formation can be avoided during deposition of the sacrificial material (such as SiO_2).

II. EXPERIMENTAL DETAILS

The tapered sidewalls were formed by ICP etching using a STS Multiplex ICP system. ICP etching is suitable because of its ability to control the vertical and lateral etch components through the variation of parameters, which include the ICP and plate powers, ambient pressure and temperature, and the gas chemistries. Mesa structures with widths of 20 μm and a separation of 4 μm were etched using photoresist as a masking material (Shipley SPR220, nominal thickness of 7 μm) under a range of conditions. The sidewalls were analyzed by cleaving the samples across the mesa structures and the cross-sectional profile was examined by scanning electron microscopy.

III. RESULTS AND DISCUSSIONS

A. Tapered-sidewall etching

A variety of process recipes can be tailored to meet the specifications, depending on their specific purposes. In this study, the plasma chemistry for the processes were fixed at 20 sccm Cl_2/8 sccm BCl_3/5 sccm Ar, while the temperature and pressure were maintained at 30 °C and 5 mTorr, respectively. On the other hand, the ICP and plate powers

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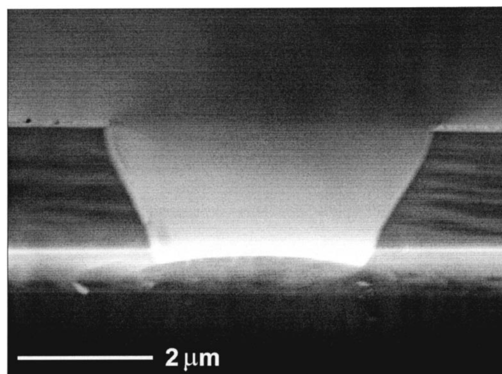
TABLE I. Typical conditions for anisotropic etching of GaN.

Conditions	ICP power/W	RIE power/W	dc bias/V	Etch rate/ nm min^{-1}	Selectivity	Inclination (°)
A	550	65	−160	2240	1:1.3	~25
B	650	50	−125	1670	1:2.13	~33
C	650	30	−90	767	1:2.96	~40

were varied to produce direct current (dc) bias ranging from −90 to −160 V. The complete list of processing conditions is tabulated in Table I. It can be seen that as the dc bias is reduced, the gradient of the tapered sidewall also reduces. This can be understood in terms of the directionality of the ions in the plasma. To achieve an anisotropic etch, a large RIE platen power is typically applied resulting in impinging ions having high energies and acceleration in the vertical direction. When the dc bias voltage is reduced, ion energies are lower and influence from the vertical electric field is reduced. This effect is enhanced by the lateral force component introduced by the ICP power coil around the chamber. Hence, ions are not confined to vertical pathways. Under such conditions, areas close to the edge of the masking material are less likely to be exposed to the ions, and a tapered sidewall is produced. Cross-sectional scanning electron microscopy (SEM) images of mesa structures etched under conditions A and C are shown in Figs. 1(a) and 1(b), respectively.

In general, a greater angle of inclination reduces the sharpness of the edge and improves step coverage. Hence, etching under conditions C would be most suitable for this purpose. However, the low etch rate achievable with this recipe places severe limitations on the depth of the mesa that can be etched. As an example, the thickness of a typical nitride-based device is ~3.5 μm. Based on a demonstrated etch rate of 767 nm/min and a selectivity of 1:2.96, the thickness of the photoresist has to be more than 10 μm. Not only are such photoresists uncommon, but the resolution achievable with thicker photoresists is also generally lower. Hence, a two-step etch recipe based on a combination of A and C can be adopted, which can then benefit from the higher etch rates of recipe A and the isotropy of recipe C. A cross-sectional SEM image of the resultant structure is shown in Fig. 2. The two-step gradient enabled represents an improvement to the single etch procedure.

A further variation of the process involves the technique of resist reflow, commonly used for the fabrication of microlenses. After resist patterning, the samples are left on a hotplate (set at 115 °C) for 3 min. Etch recipe A is employed for this etch. The gentle gradient achieved with this process, as illustrated in Fig. 3, represents a direct transfer of resist profile onto the GaN mesa structure, enabling uniform metal coating across the entire surface. Of course, this process is not without drawbacks. From the figure, a substantial loss of critical dimension can be observed. Hence, this process is not suitable for micron-scale devices.



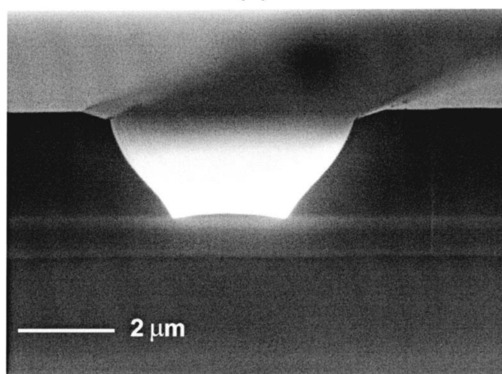


FIG. 1. SEM image showing the cross-sectional profile of a tapered-sidewall GaN mesa structure etched using (a) conditions A and (b) conditions C.

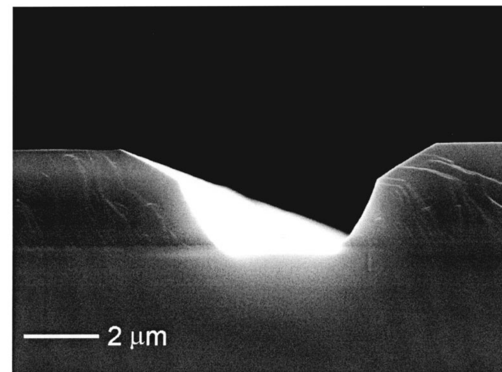


FIG. 2. SEM cross-sectional image of a GaN mesa structure etched using a two-step etching procedure.

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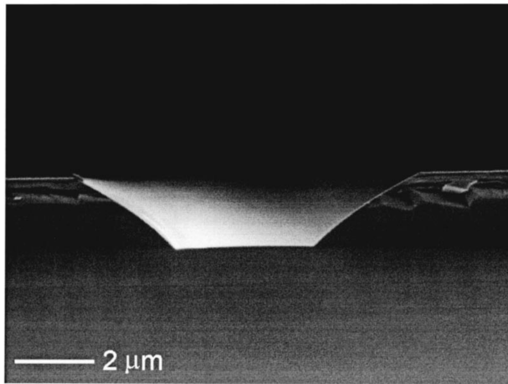


FIG. 3. SEM cross-sectional image of a GaN mesa structure. The masking pattern used in this etch has been treated with a thermal-reflow process.

B. Application to device fabrication

The processes developed here are targeted at the fabrication of InGaN-based microlight emitting diodes (micro-LEDs), there being linear or two-dimensional arrays of micrometer-sized LEDs. Up to now, two variants of these devices have been extensively developed with specific applications: interconnected micro-LEDs as high efficiency emitters,[7] and matrix-addressable micro-LEDs for microdisplay purposes,[8] at wavelengths varying from 370 nm (near-ultraviolet) to 520 nm (green). Figure 4 shows the planar view of a region of a completed micro-LED array with the 135-μm-thick Au metal lines running conformally across the 3.4 μm mesa columns. Application of the tapered sidewall etching scheme has resulted in significant improvements to the operational performance over devices fabricated using conventional approaches as evident from the microphotographs in Fig. 5. In Fig. 5(a), the emission characteristics of an interconnected array of 12 μm micro-LEDs emitting at a wavelength of 470 nm fabricated by the "standard" planarization technique is shown. As a result of extensive surface damage due to abrasion, the light emission pattern is extremely nonuniform. Adapting the tapered-sidewall approach, light emission is uniform across the complete array, as illustrated in Fig. 5(b). Such uniformity also applies to the electrical characteristics of the devices. Using the same etching technique, microdisplays with a resolution of 128×96 have been demonstrated, and is illustrated in Fig. 6.

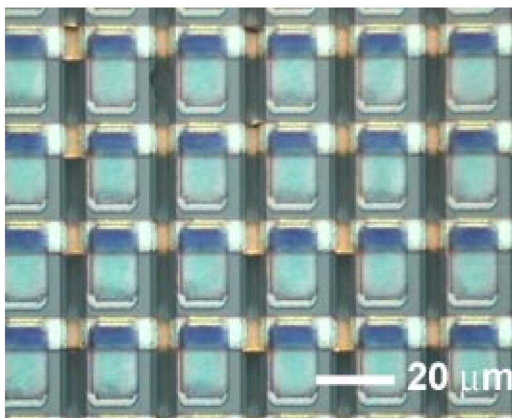
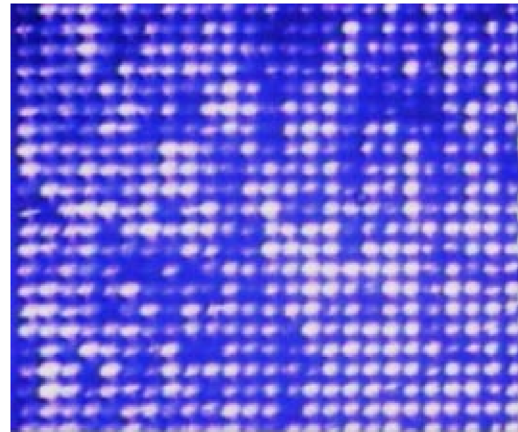


FIG. 4. Microphotograph image of a matrix-addressable micro-LED device, fabricated using the sloped-sidewall process. Note the metal lines running conformally across the GaN columns.



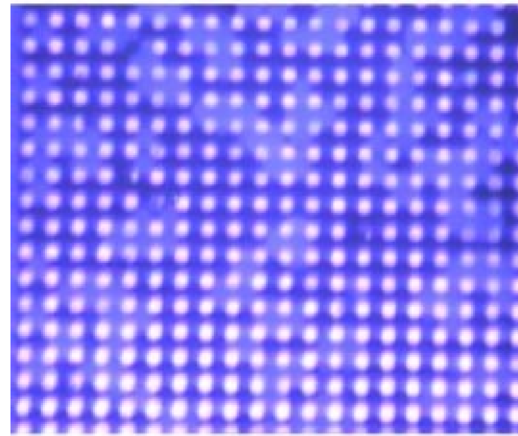


FIG. 5. Comparison of the emission uniformity in interconnected micro-LED devices emitting at 470 nm fabricated using (a) planarization and (b) tapered-sidewall techniques.

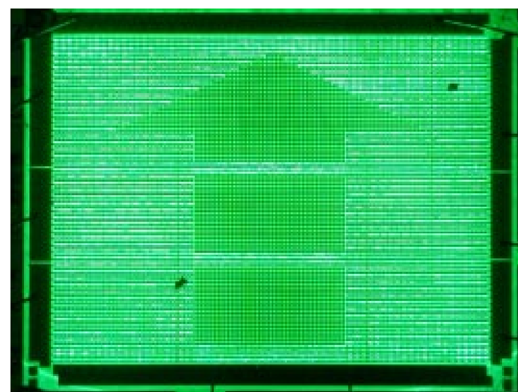


FIG. 6. Operational image of a 128×96 elements microdisplay, with an arrow pattern illuminated at a wavelength of 520 nm.

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IV. CONCLUSIONS

In summary, a method controllably of producing mesa structures with tapered sidewall in GaN-based materials has been introduced. ICP etching is used because of the ability to control the vertical and lateral etch components simultaneously. By adjusting a combination of parameters, tapered sidewalls can be formed, with inclination angles ranging from 25° to 40°, allowing for conformal metal coverage across the mesa structures. The process has been successfully adopted for the fabrication of interconnected and matrix-addressable micro-LEDs, where superior performance and uniformity have been achieved compared to devices fabricated using conventional techniques.

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