Generalized Self-Driven AC–DC Synchronous Rectification Techniques for Single- and Multiphase Systems

W. X. Zhong, W. P. Choi, Wing W. C. Ho, *Member, IEEE*, and S. Y. Hui, *Fellow, IEEE*

***Abstract*—This paper extends the single-phase self-driven synchronous rectification (SDSR) technique to multiphase ac–dc systems. Power MOSFETs with either voltage- or current-sensing self-driven gate drives are used to replace the diodes in the rectifier circuits. The generalized methodology allows multiphase SDSRs to be designed to replace the multiphase diode rectifiers. Unlike the traditional SR that is designed for high-frequency power converters, the SDSR proposed here can be a direct replacement of the power diode bridges for both low- and high-frequency operations. The SDSR utilizes its output dc voltage to supply power to its control circuit. No start-up control is needed because the body diodes of the power MOSFETs provide the diode rectifier for the initial start-up stage. The generalized method is demonstrated in 2-kW one-phase and three-phase SDSRs for inductive, capacitive, and resistive loads. Power loss reduction in the range of 50%–69% has been achieved for the resistive load.**

***Index Terms*—Energy saving, mains-frequency synchronous rectifiers, self-driven synchronous rectifiers.**

I. Introduction

SYNCHRONOUS rectifiers based on the use of power MOSFETs to replace the diodes in reducing the conduction losses have been widely used in low-voltage high-current applications since 1990 [1]. Synchronous rectifier techniques are primarily applied to various versions of dc–dc converters such as buck converters [2], [3], flyback and boost-buck converters [4], [5], half-bridge converters [6], [7], and LCC resonant converters [8], [9]. To reduce the cost of the gate-drive circuits, self-driven techniques have been an active research topic in synchronous rectifiers [2], [7], [9], [10], although the gate control integrated circuit for driving synchronous rectifiers is also commercially available [11]. Other research aspects include the use of the soft-switching technique [6], [9], [12]. Besides the dc–dc converters, the synchronous rectification techniques have been applied to the three-phase full-bridge ac–dc converter based on a three-phase fully controlled bridge [13] and even to the five-level converter [14]. While the self-driven technique uses the changing voltage polarity of the coupled windings to control the switching of the power MOSFETs, other techniques tend to use control integrated circuits to provide the gating signals.

An attempt to replace a general-purpose diode bridge with a synchronous rectifier for low-power and low-voltage (3–5 V) applications appears in [15] in which the synchronous rectification technique is applied to a center-tap rectifier topology. A customized charge pump circuit is however needed in the proposal of [15] in order to provide a suitable dc power supply for the gate drive. As such proposal aims at low-voltage applications, it is not suitable for high-voltage mains voltage operations. For a high-power and mains-frequency operation, a synchronous rectifier technique has been previously proposed [16]. It is based on the detection of the phase–phase voltage, and sophisticated logic and timing circuits are needed to provide the gating signals if the ac source has a significant source inductance. However, the gating signals for the synchronous rectifiers based on voltage detection are not adequate because the diodes of a traditional bridge rectifier only turn off after their current reverse-recovery processes.

It has been pointed out in [17] and [18] that it is more appropriate to use at least one current-sensed gate drive in each current loop of the synchronous rectifier for general power applications unless there is an external circuit that will be used to cut off the current for the rectifier. In this paper, the principle of ac–dc synchronous rectification based on the self-sensing and self-driven control circuit is generalized from single-phase systems to multiphase ones for both low- and high-voltage applications and for both low- and high-frequency operations. Power MOSFETs with either voltage or current self-sensing and self-driven gate drives are used to replace the diodes in the rectifier circuits. New self-driven synchronous rectification (SDSR) circuits are designed to behave like the traditional diode rectifiers, except that their conduction loss is much smaller than that of the diode rectifiers. This principle is successfully and practically demonstrated in a three-phase synchronous rectifier for capacitive, inductive, and resistive loads, with the significant loss reduction exceeding 50% when compared with a diode bridge at both 110 and 220 V mains. Consequently, the thermal management and heat

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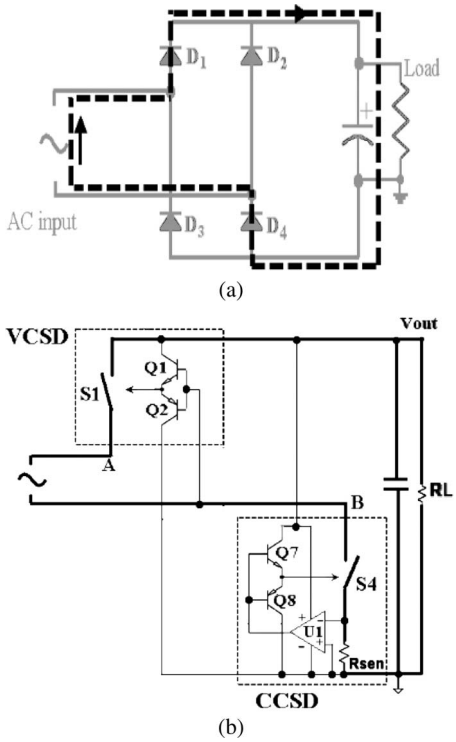

Fig. 1. (a) One conducting path via two diodes. (b) A conducting path via one VCSD and one CCSD.

sink requirements are reduced, and a more compact rectifier can be achieved for general-purpose ac–dc applications. In this paper, Section II outlines the generalized SDSR principle. The hardware implementation is illustrated in Section III using a three-phase SDSR as an example. The measurements on the single- and three-phase SDSRs and their diode rectifier counterparts are included in Section IV. Finally, we conclude in Section V.

II. Generalized SDSR Principle

A. Single-Phase Rectification System

Starting with a single-phase diode rectifier, this section describes the general principle behind the proposal. Fig. 1(a) shows one conduction loop of a diode rectifier. As the input ac voltage reverses and the current starts to reverse, the diodes will turn off after the current reverse recovery. This means that the power MOSFETs that replace the diodes in the SDSR should turn off when the sensed current begins to reverse. However, it should be noted that, as long as one MOSFET is turned off, the current path is cut off. Therefore, the first principle of this generalized method is that at least one of the power MOSFETs should have a "self-sensing" current-controlled self-driven (CCSD) gate drive. The CCSD MOSFET is controlled in such a manner that, by sensing the branch current, the MOSFET is turned on when the current is larger than a small threshold value (e.g., 0.1 A) and is then turned off so that its body diode will carry a current less than the threshold current and will perform the diode reverse recovery for full turn-off of the CCSD switch. The voltage-controlled self-driven (VCSD) MOSFET relies on voltage sensing of only the ac mains voltage. Since the CCSD gate drive is more complicated than the "self-sensing" VCSD gate drive, as shown in Fig. 1(b), it is proposed that one CCSD and one VCSD gate drive should be used in each current loop in the synchronous rectifier. In Fig. 1(b), a current-sensing resistor $R_{\rm sen}$ is used to provide the feedback signal for the CCSD gate drive. In principle, the ON-state resistance of the power MOSFET can be used as the current-sensing resistor if desired.

TABLE I
Logic Assignments of Different Circuit Elements

	CCSD	Diode	Inductor	VCSD	Capacitor
X	I	D	L	V	C
SX	1	1	1	0	0

A systematic way of generalizing an ac–dc SDSR system is shown as follows. Let X be a circuit component that can be one of the following: a diode (D), an inductor (L), a capacitor (C), a CCSD active switch (CCSD), and a VCSD active switch (VCSD). The location of the upper elements in a rectifier is defined by the subscript i of the circuit element symbol X_i. For the upper branch elements X_i

$$i = 1, 2, \ldots, n.$$

For the lower branch elements X_j

$$j = n+1, n+2, \ldots, 2n$$

where n is the number of converter branches. For example, for a single-phase rectifier

$$n = 2.$$

The numbers of the upper elements are one and two, and the numbers of the lower elements are three and four, as shown in Fig. 1(a).

A logic value is assigned to each circuit element X_i or X_j (which can be an active switch, a diode, or other circuit element), which is represented by

$$SX_i, \qquad i = 1, 2, \ldots, n$$
$$SX_j, \qquad j = n+1, n+2, \ldots, 2n.$$

For the circuit element showing the capability of the resisting instantaneous current change, a logic value of "1" is assigned. Therefore, "1" is assigned to a CCSD active switch, a diode, and an inductor. A VCSD active switch and a capacitor have no such capability of resisting the instantaneous current change. Therefore, they have been assigned a logic value of "0." Table I shows the corresponding logic value for each circuit element.

In a bridge rectifier, each current loop $\{X_i, X_j\}$ can be identified by the branch location in the circuit, and an associated circuit element logic value in the branch can be mapped in the corresponding current loop

$$\{X_i, X_j\} \rightarrow \{SX_i, SX_j\}. \tag{1}$$

In order to achieve the function of the SDSR in a rectifier, it requires that at least one CCSD active switch, inductor, or diode must be present in each current loop of a rectifier. The

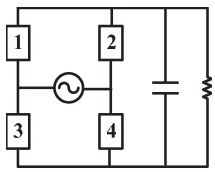

Fig. 2. Structure of a single-phase synchronous rectifier.

aforementioned circuit elements have the capability of blocking a reverse current flow and changing to the OFF state automatically. Therefore, the logical "OR" function of two circuit elements in a current loop must be equal to "1" such that the SDSR mechanism can be realized.

In the following analysis of the different possible configurations, the following terminology is used:

$SX_i \cup SX_j = 1$ means that a correct combination of circuit elements exists in a current loop;

$SX_i \cup SX_j = 0$ means that an incorrect combination of circuit elements exists in a current loop.

For a single-phase rectifier with four elements (Fig. 2), there are 16 (i.e., 2^4) possibilities. Table II defines the nine valid topologies of a full-bridge rectifier and the associated current loops, where the upper branches comprise circuit elements 1 and 2, while the lower branches comprise circuit elements 3 and 4. Some examples that are of particular practical significance are given here to demonstrate the general SDSR principle based on the configurations listed in Table II. These configurations are highlighted in bold in Table II.

Configuration 1 of Table II can be realized by the circuit shown in Fig. 3, where the two upper elements SX_1 and SX_2 are VCSD active switches (with logic "0") and the two lower elements SX_3 and SX_4 are CCSD active switches (with logic "1"). This is an example that will be studied in this paper for practical demonstration.

Configuration 4 of Table II can be used to develop a half-bridge rectifier or a voltage doubler, as shown in Fig. 4, where elements 1 and 3 are CCSD active switches (with logic "1") and elements 2 and 4 are capacitors (with logic "0"). Configuration 9 of Table II can lead to the implementation of a single-phase current doubler, as shown in Fig. 5, where SX_1 and SX_2 are inductors and SX_3 and SX_4 are CCSD active switches.

B. Multiphase Rectification Systems

The principle can be generalized to a multiphase system. For example, a three-phase ac-dc converter (Fig. 6) consists of six elements. Based on the generalized method, the valid configurations are listed in Table III. Out of the 64 (i.e., 2^6) possible arrangements, 18 configurations are valid for the three-phase synchronous rectification.

From the single- and three-phase systems, it can be seen that, for a two-level (standard) rectification, the number of valid configurations (N_v) obeys the following equation:

$$N_v = 2^{n+1} + n - 1 \tag{2}$$

where n is the number of converter branches (i.e., two for the single phase and three for the three phase).

Two examples that are based on Table III are used to illustrate the general principle. Fig. 7 shows a three-phase half synchronous rectifier based on configuration 8 of Table III. The three upper elements are diodes, and the three lower elements are VCSD active switches. This arrangement reduces the conduction losses in only three diodes when compared with a three-phase diode bridge. A three-phase full synchronous rectifier based on configuration 1 of Table III is shown in Fig. 8, where the three upper elements are VCSD active switches and the three lower elements are CCSD active switches.

III. Self-Driven Gate-Drive Circuitry

The low-power self-driven gate-drive circuitry for a three-phase synchronous rectifier is used to illustrate the operating principle of a multiphase SDSR system. As shown in Fig. 9, six power MOSFETs (M_1 to M_6) form the main circuit for the three-phase full-wave rectification. The self-driven gate-drive circuits for the six MOSFETs, highlighted in shaded boxes, are powered by the output dc voltage of the SDSR, and they consume a low power. The circuitry can, in principle, be integrated in the same rectifier package. The whole circuit can be divided into two parts: high- and low-side circuits. Both high- and low-side parts are symmetrical. The six body diodes of the power MOSFETs (M_1 to M_6) form a standard diode bridge. This means that, even if the gate-drive circuits are not ready for operation immediately at the start-up of the circuit, this standard diode bridge is inherent in the proposed circuit, which is used to perform the function of rectification before the gate-drive circuitry is ready.

A. Operating Principle—Initial Gate-Drive Start-Up

As shown in Fig. 9, there are three capacitors in each of the three high-side driving circuits (C_1, C_2, and C_3 for M_1; C_4, C_5, and C_6 for M_2; and C_7, C_8, and C_9 for M_3). Each upper gate drive has three driving stages. Taking M_1 as an example, Q_2 to Q_5, M_7 and M_8, and Q_6 and Q_7 form the three driving stages. Q_2 to Q_5 form the first logic stage, and they are for signal amplification and for providing charging paths for the capacitors acting as power supplies. M_7 and M_8 form an intermediate inverter stage. Q_6 and Q_7 form a fast and final driving stage for the power MOSFET M_1. C_3, C_6, and C_9 are charged as the power supplies in driving the first logic stages for M_1, M_2, and M_3, respectively. Before C_3, C_6, and C_9 are charged up to a certain threshold voltage, e.g., 10 V, the driving logic in the circuit will not be active. C_1, C_4, and C_7 will be charged up as the power supplies of the intermediate and final driving stages for the three upper MOSFETs. In the start-up stage, C_2, C_5, and C_8 are designed to be charged up faster than C_3, C_6, and C_9, until their voltages reach a certain level clamped by the Zener diodes D_{Z1}, D_{Z2}, and D_{Z3}. Bipolar transistors Q_1, Q_8, and Q_{15} are used to ensure that C_1, C_4, and C_7 will not be charged before C_3, C_6, and C_9 have been charged up to a voltage higher than the voltage of C_2, C_5, and C_8. Therefore, MOSFETs M_1, M_2, and M_3 will not switch before the driving logic has been set up.

TABLE II
VALID CONFIGURATIONS OF A SINGLE-PHASE SYNCHRONOUS RECTIFIER

	Logic Value of Circuit Element				A	B	Valid SR Config.
Congfig. No.	SX_1	SX_2	SX_3	SX_4	$SX_1 \cup SX_3$	$SX_2 \cup SX_4$	$A \cap B$
1	**0**	**0**	**1**	**1**	**1**	**1**	**1**
2	0	1	0	1	1	1	1
3	0	1	1	1	1	1	1
4	**1**	**0**	**1**	**0**	**1**	**1**	**1**
5	1	0	1	1	1	1	1
6	1	1	0	0	1	1	1
7	1	1	0	1	1	1	1
8	1	1	1	0	1	1	1
9	**1**	**1**	**1**	**1**	**1**	**1**	**1**

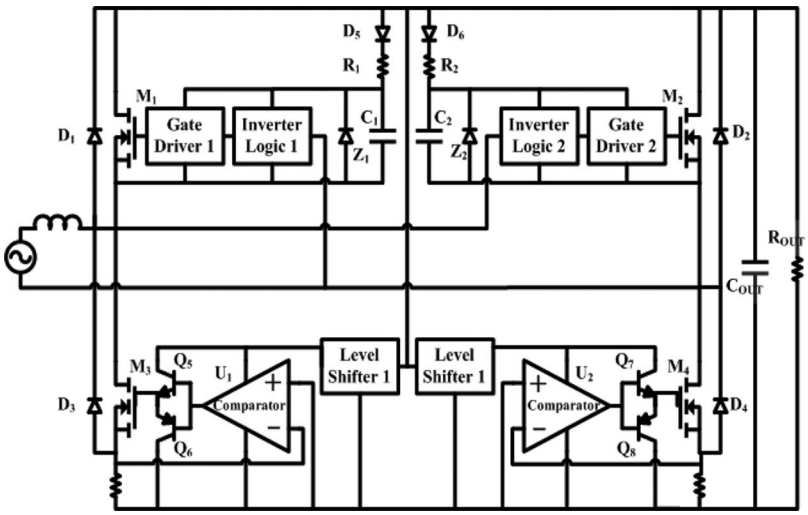

Fig. 3. Practical high-voltage circuit for a single-phase full-bridge rectifier based on configuration 1 of Table II.

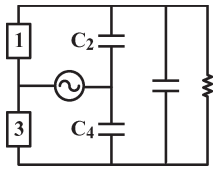

Fig. 4. Schematic of a half-bridge rectifier or voltage doubler on configuration 4 of Table II.

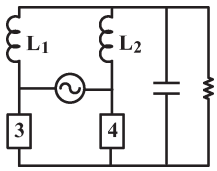

Fig. 5. Schematic of a current doubler based on configuration 9 of Table II.

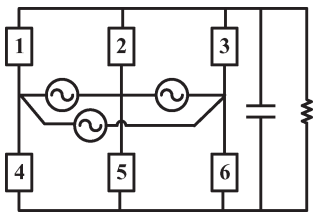

Fig. 6. Basic structure of a three-phase synchronous rectifier.

B. Operation Principle of the Upper Gate Drives

The transitional period shaded in Fig. 10 is used to illustrate the operation of the upper gate drive. We use v_{BCn} to represent the base–collector voltages of the BJT Q_n. The voltage across C_1, C_4, and C_7 is assumed to be at a constant level V. In this period, the output phase will change from phase A to phase B. Therefore, M_1 should be turned off, and M_2 should be turned on at the commutation point. Because the phase voltage v_c is the lowest, therefore v_{BC3} and v_{BC12} are clamped to zero (0.7 V to be precise) by the p-n junctions between the collector and the base of Q_3 and Q_{12}. With the aid of the timing diagram in Fig. 11, the operation of the upper gate drives can be explained as follows.

1) Before t_1: v_{AB} is higher than V. Both current directions in R_7 and R_8 are from left to right, as shown in Fig. 12(a). v_{BC5} is clamped zero by the collector–base p-n junction of Q_5. Therefore, the p-channel MOSFET M_7 is on, and the n-channel MOSFET M_8 is off. Such condition keeps the gate–source voltage of M_1 high, thus turning it on. Meanwhile, the current in R_8 flows through the base–collector p-n junction of Q_9, which clamps v_{BC10} at V. Because D_2 is reverse biased, the gate–source voltage of M_{10} is kept at V. Therefore, M_9 is off,

TABLE III
VALID CONFIGURATIONS OF A THREE-PHASE SYNCHRONOUS RECTIFIER

	Logic Value of Circuit Element						A	B	C	D	E	F	Valid Config.
Congfig. No.	SX_1	SX_2	SX_3	SX_4	SX_5	SX_6	$SX_1 \cup SX_5$	$SX_1 \cup SX_6$	$SX_2 \cup SX_4$	$SX_2 \cup SX_6$	$SX_3 \cup SX_4$	$SX_3 \cup SX_5$	$A \cap B \cap C \cap D \cap E \cap F$
1	0	0	0	1	1	1	1	1	1	1	1	1	1
2	0	0	1	1	1	1	1	1	1	1	1	1	1
3	0	1	0	1	1	1	1	1	1	1	1	1	1
4	0	1	1	1	1	1	1	1	1	1	1	1	1
5	1	0	0	1	1	1	1	1	1	1	1	1	1
6	1	0	1	1	1	1	1	1	1	1	1	1	1
7	1	1	0	1	1	1	1	1	1	1	1	1	1
8	1	1	1	0	0	0	1	1	1	1	1	1	1
9	1	1	1	0	0	1	1	1	1	1	1	1	1
10	1	1	1	0	1	0	1	1	1	1	1	1	1
11	1	1	1	0	1	1	1	1	1	1	1	1	1
12	1	1	1	1	0	0	1	1	1	1	1	1	1
13	1	1	1	1	0	1	1	1	1	1	1	1	1
14	1	1	1	1	1	0	1	1	1	1	1	1	1
15	0	1	1	0	1	1	1	1	1	1	1	1	1
16	1	0	1	1	0	1	1	1	1	1	1	1	1
17	1	1	0	1	1	0	1	1	1	1	1	1	1
18	1	1	1	1	1	1	1	1	1	1	1	1	1

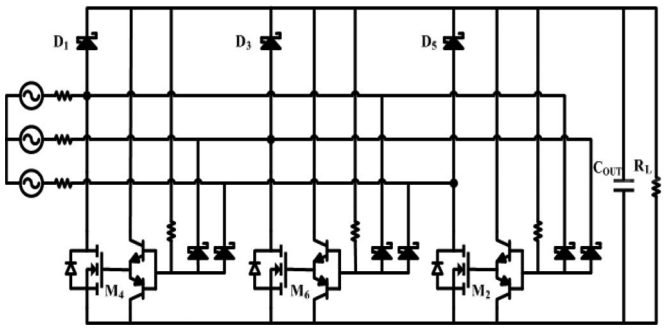

Fig. 7. Three-phase half synchronous rectifier for low-voltage applications.

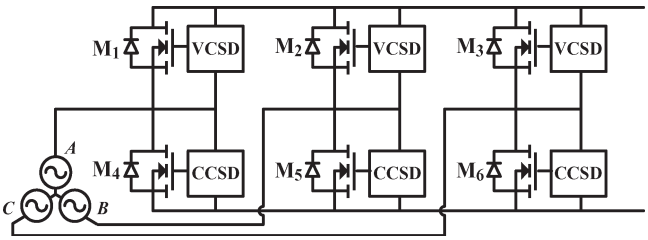

Fig. 8. Three-phase full synchronous rectifier for high-voltage applications.

and M_{10} is on to keep the gate–source voltage of M_2 low.

2) t_1–t_2: As shown in Fig. 12(b), when v_{AB} becomes lower than V after t_1, the current in R_7 changes its direction. Q_4 is turned on, and Q_5 turns off. v_{BC5} starts to be charged up from zero. Due to D_1 and Q_4, the gate–source voltage of M_8 will follow v_{BC5}. At the end of this interval, the gate–source voltage of M_8 reaches its gate threshold voltage.
3) t_2–t_3: M_8 begins to conduct at t_2. v_{GS1} starts to decrease. v_{BC5} continues to increase. Before it reaches the threshold voltage for M_7 to switch off at t_3, M_7 and M_8 will simultaneously conduct, as shown in Fig. 12(c). Somewhere in this interval, v_{GS1} will fall to the gate threshold voltage of M_1 (the time of which can be slightly controlled by the proportion of R_3 and R_4). The interval ends when v_{GS1} falls to zero and when M_1 is turned off.
4) t_3–t_4: As shown in Fig. 12(d), M_7 turns off at t_3, and M_8 is kept on to keep M_1 off. The current flows through the source–drain diode of M_1. Commutation will happen at t_4.
5) t_4–t_5: As shown in Fig. 12(e), when v_{AB} becomes lower than zero after t_4, the current in R_8 changes its direction. v_{BC10} begins to decrease from V, indicating that Q_9 is turned off and Q_{10} is turned on. While at t_4, v_{BC5} reaches V, and it will be clamped at the voltage of C_3 by the base–collector p-n junction of Q_4. Meanwhile, the source–drain diode of M_1 turns off, and the source–drain diode of M_2 begins to conduct naturally, as shown in Fig. 12(e). The interval ends when v_{BC10} falls down to the threshold voltage for M_9 to switch on.
6) t_5–t_6: As shown in Fig. 12(f), M_9 begins to conduct at t_5, and v_{BC10} continues to decrease. Before v_{BC10} falls down to the gate threshold voltage of M_{10} at t_6, M_9 and M_{10} simultaneously conduct. v_{GS2} begins to increase, and it will reach a high value at the end of the interval to turn M_2 on.
7) t_6–t_7: At t_6, M_{10} is turned off, and v_{BC10} continues to decrease, as shown in Fig. 12(g). The interval ends when v_{BC10} reaches zero.
8) After t_7: v_{AB} is lower than $-V$. v_{BC10} is clamped zero by the collector–base p-n junction of Q_{10}, as shown in Fig. 12(h).

C. Operation Principle of the Lower Gate Drives

The lower MOSFETs are controlled by the "current-controlled" gate-drive circuits. Current-sensing resistors R_{S1} to R_{S3} and comparators are used to detect the MOSFET currents and to drive the MOSFETs. Fig. 13 shows the drive circuit of

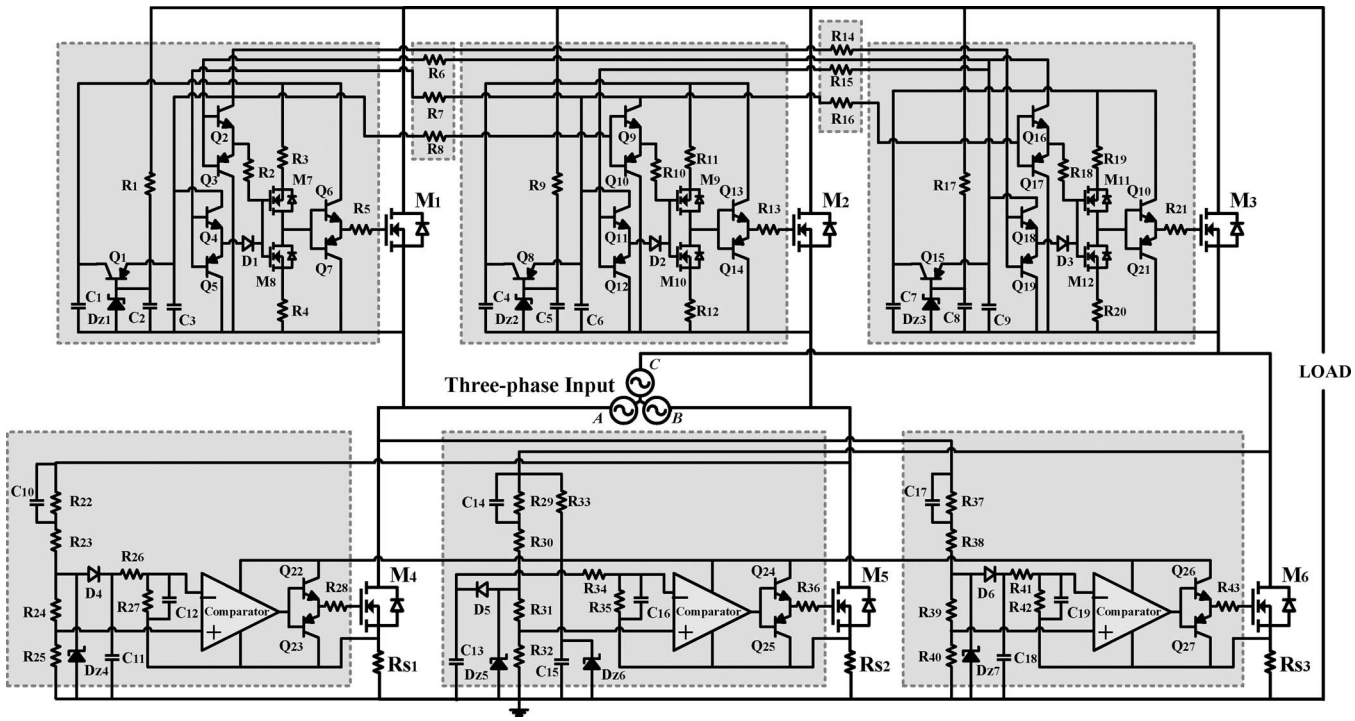

Fig. 9. Proposed three-phase self-driven synchronous rectifier.

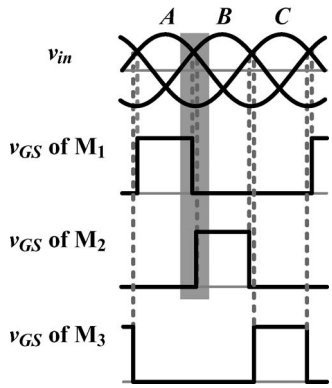

Fig. 10. Gate–source signals of the three upper MOSFETs with the input phase voltages.

M_5 (phase B). C_{13} is used to give a positive voltage for the inverting inputs of the comparators, which can provide a safe margin set by the potential divider comprising resistors R_{34} and R_{35}. The voltage of C_{15}, stabilized by the Zener diode D_{Z6}, is the power supply for the comparators. C_{13} will be charged up to the designated voltage before the voltage of C_{15} reaches a voltage that is high enough for the comparators to work. This arrangement ensures that the low-side MOSFETs M_4 to M_6 are switched only when the proper logic control is ready.

D. Additional Circuits for Turning Off at Zero-Crossing Points

The self-driven synchronous rectifier is designed to cope with the resistive, capacitive, and inductive loads. The driving waveforms of phase B for the resistive load are shown in Fig. 14. Here, v_{C0} is the input voltage of phase C, taking the low

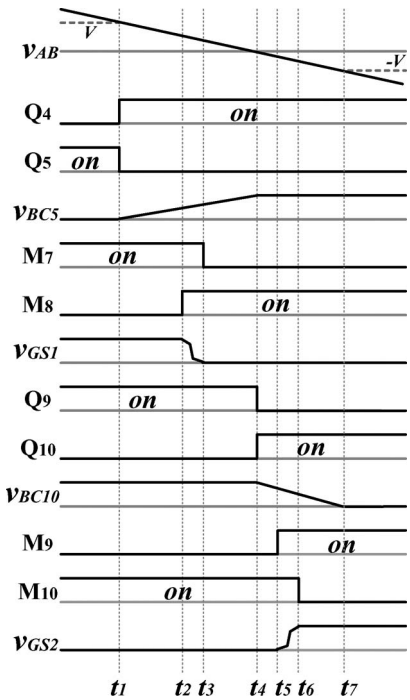

Fig. 11. Timing diagram for the high-side gate-drive circuits.

rectified voltage as reference zero (Fig. 1), and i_B is the current flowing through M_5. The current commutates with a sharp slope. The comparator may not respond quickly enough to turn off MOSFETs M_5 under such a fast current change, which may cause a fatal short-circuit situation. Therefore, an extra circuit (Fig. 15) is added to provide a small positive signal to the noninverting inputs of the comparator. The signal is generated

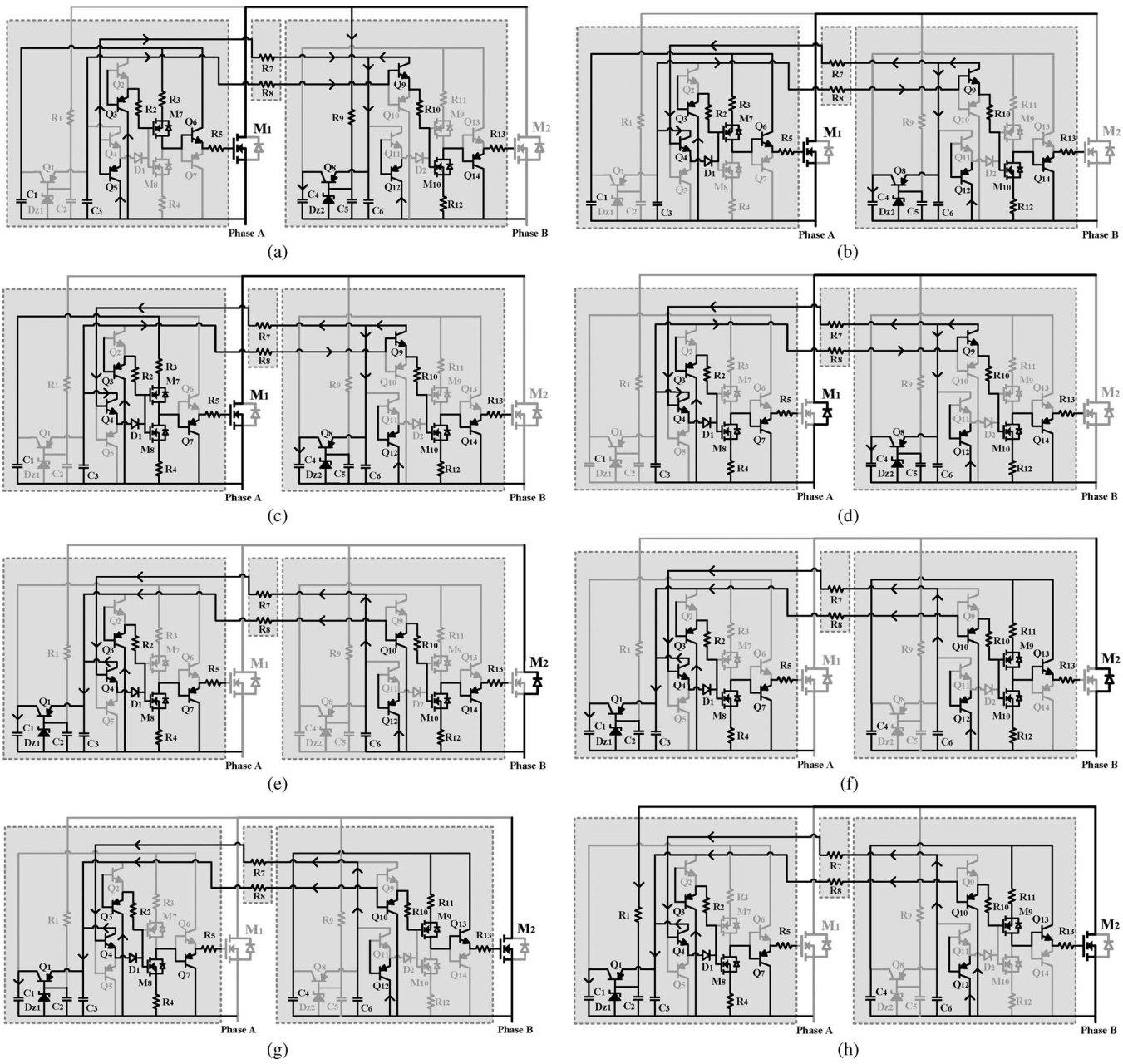

Fig. 12. Operation intervals of the proposed upper driver. (a) Before t_1. (b) t_1-t_2. (c) t_2-t_3. (d) t_3-t_4. (e) t_4-t_5. (f) t_5-t_6. (g) t_6-t_7. (h) After t_7.

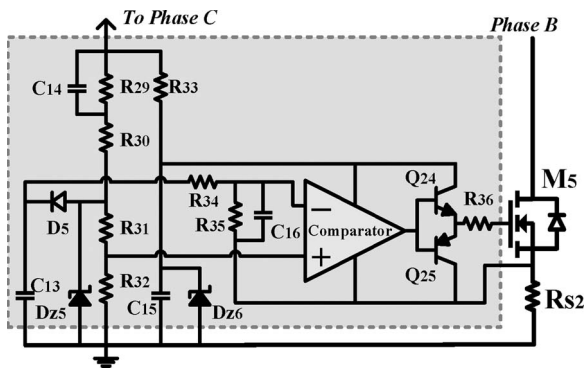

Fig. 13. Drive circuit of M_5 (phase B).

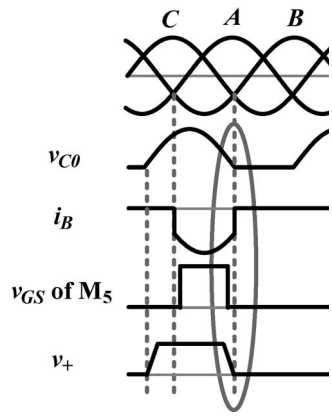

Fig. 14. Driving waveforms of the phase B low-side circuit.

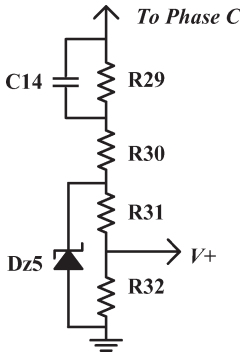

Fig. 15. Additional circuit to guarantee the comparator to turn off (phase B).

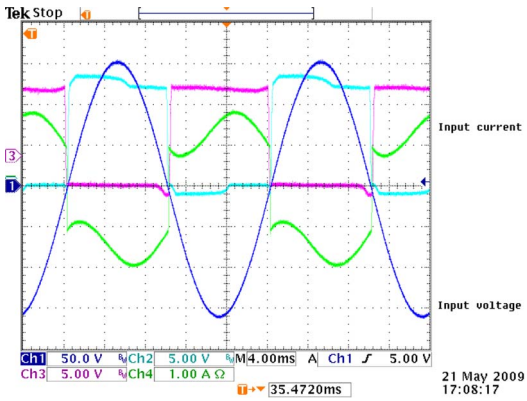

Fig. 16. (Light blue and pink) Gate voltage of the VCSD MOSFETs. (Dark blue) Input voltage. (Green) Input current [19].

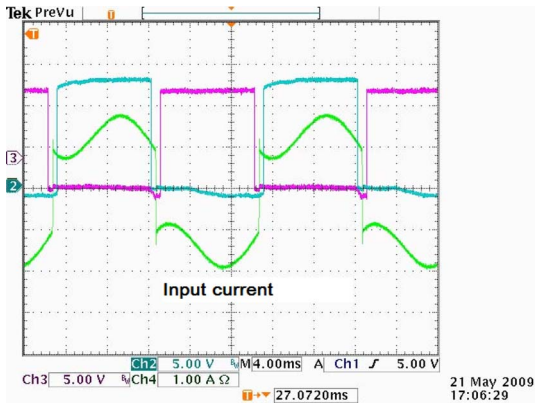

Fig. 17. (Pink and dark green) Gate voltage of the CCSD MOSFETs. (Green) Input current [19].

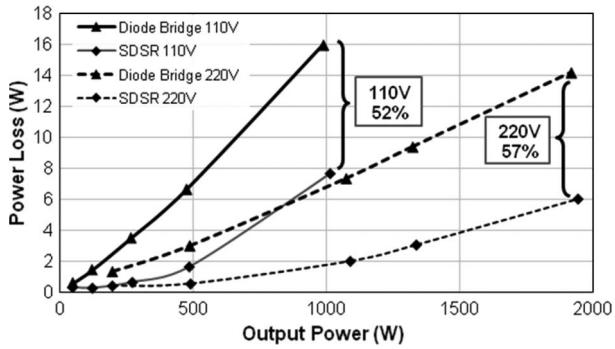

Fig. 18. Power loss comparison of the diode rectifier and the self-driven rectifier with a resistive load [19].

from the input voltage of phase C, as shown in Fig. 14, and it can guarantee the comparator to turn off the MOSFETs in time. In Fig. 15, D_{Z5} is a Zener diode of about 10 V. When the v_{C0} begins to rise from zero, the voltage of D_{Z5} will rise until it reaches its rated voltage. Then, it will remain at this voltage with a very small fluctuation. Here, R_{31} and R_{32} form a voltage divider to scale down the voltage signal with a reduced fluctuation.

IV. Practical Verification

Practical evaluations of a 2-kW single-phase SDSR based on Fig. 3 and a 2-kW three-phase SDSR based on Fig. 9 have been carried out. A diode bridge comprising diodes 60EPF06PbF, with a forward voltage drop of about 0.85 V, is used to compare with an SDSR based on MOSFETs IPW60R045CP, with an ON-state resistance of 45 mΩ. The current and voltage waveforms are captured with the use of a Tektronix digital storage oscilloscope, and the power measurements are captured using the Voltech PM6000 Power Analyser.

A. Single-Phase SDSR

A single-phase SDSR has been tested with an inductive–resistive load ($L = 133$ mH and $R = 73.3$ Ω). Two CCSD MOSFETs are used to replace the lower diodes, and two VCSD MOSFETs are employed to replace the two upper diodes [19]. Fig. 16 shows the two gate signals of the two VCSD MOSFETs, the input ac voltage, and the input current. It can be seen that the two gate signals are synchronized with their respective half-cycles of the ac mains voltage. The corresponding gate signals of the two CCSD MOSFETs are shown with the input current in Fig. 17. The input current waveform is a typical one, as expected from a diode bridge with an LR load. Fig. 18 shows a practical comparison of the power losses between this single-phase SDSR and a diode bridge. It can be seen that over 50% of the power loss reduction can be achieved.

B. Three-Phase SDSR

A three-phase SDSR has also been set up for a resistive load ($R = 348\ \Omega$) and a capacitive–resistive load ($C = 470\ \mu$F and $R = 73.3\ \Omega$). Similar to the situation in the single-phase case, the upper MOSFETS are voltage controlled, and the lower MOSFETS are current controlled. For comparison, Vishay diodes 60EPF06PBF and Infineon Mosfets IPW60R045CP are used in the tests. Fig. 19 shows the measured gate voltages of the three lower CCSD MOSFETs and the corresponding input current of one phase. It can be observed that the three lower switches conduct 120° per cycle as expected, and the phase current is similar to that expected from a standard three-phase diode rectifier with a resistive load. The measured gate voltages of the upper MOSFETs and the output voltage of the three-phase SDSR are shown in Fig. 20. These practical

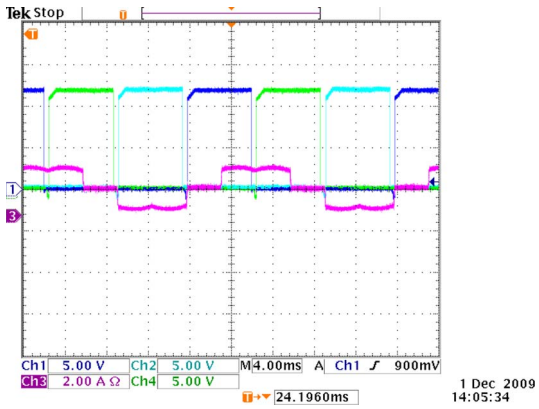

Fig. 19. Gate–source voltages of the lower (CCSD) MOSFETs and the input current of one phase (pink) for a resistive load.

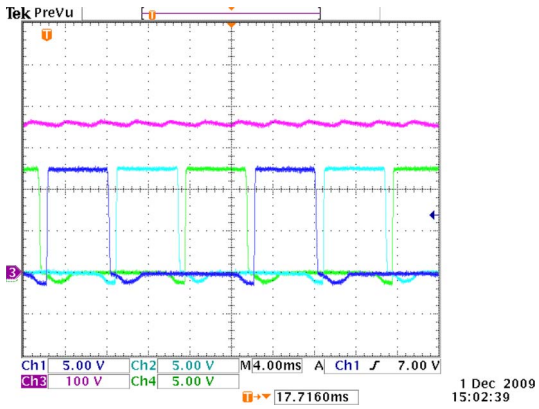

Fig. 20. Gate–source voltages of the upper (VCSD) MOSFETs and the output voltage (pink) for a capacitive–resistive load.

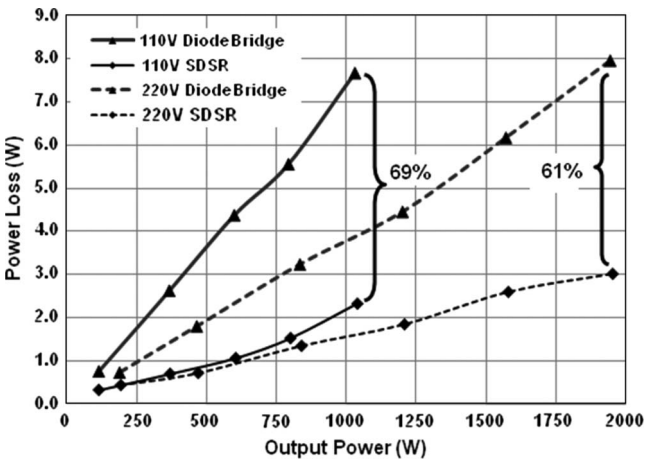

Fig. 21. Power loss comparison of a three-phase diode rectifier and a self-driven synchronous rectifier with a resistive load.

measurements confirm the operation of the multiphase SDSR. Fig. 21 shows the practical comparison of the power losses between a three-phase diode rectifier and a three-phase SDSR for a resistive load. It is found that over 60% of the power loss can be reduced.

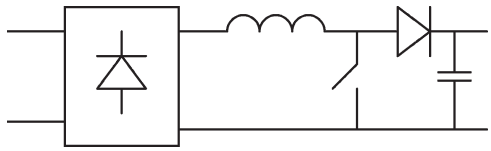

Fig. 22. Schematic of a boost-type power factor correction circuit with a front-end diode rectifier.

C. Application as a Front AC–DC Stage for a 100-kHz Boost-Type Power Factor Correction Circuit

The scheme of a 750-W boost-type power factor correction is shown in Fig. 22. The switching frequency of the boost converter is 100 kHz, and the converter is operated at the continuous conduction mode. This system is designed for a universal input voltage from 96 to 264 V and a dc output voltage of 400 V. In order to evaluate the efficiency improvement, the diode bridge is replaced by a self-driven synchronous rectifier, as shown in Fig. 23. Both the original and modified circuits are tested at 110 and 220 V. The energy efficiency plots of the two schemes are shown in Fig. 24. It can be seen that a power loss reduction of over 50% in the rectification power stage can be achieved. The measured input voltage, input current, and dc output voltage of the modified system are shown in Fig. 25. The power factor is found to be 0.99. These waveforms are essentially identical to those of the original systems. These practical measurements confirm that the SDSR can replace the diode bridge in a standard power factor correction circuit without affecting the waveforms and power factor. Since a reduction of almost 7 W (∼1%) can be achieved in a small diode rectifier circuit, the thermal stress of the rectifier circuit can be reduced, and a less heat sink requirement would be needed using the SDSR.

V. Conclusion

This paper has presented the fundamental concept of a generalized SDSR technique that can be extended to the multiphase rectifier systems. Unlike the existing synchronous rectifiers designed for the high-frequency power converters, the proposed self-driven synchronous rectifiers can be operated at mains frequencies. This principle stresses the need for at least one current-controlled (CCSD) MOSFET in each current loop of the synchronous rectifier so that the MOSFET can be switched off when the current reverses (i.e., like the current reverse recovery of a diode). Consequently, there is no need to design a sophisticated control logic to control the MOSFETs.

The principle has been successfully demonstrated in practical single- and three-phase systems up to 2 kW. The measurements have confirmed that a significant power loss reduction in the range of 50%–69% can be achieved. Further power loss can, in principle, be achieved by using parallel power MOSFETs to reduce the ON-state resistance. Since the diode rectifiers are widely used components in many electronic and electrical applications, the proposed principle can be used to design low-loss replacements for these diode rectifiers. With a significant reduction in the power loss, the temperature rise of the rectifier can be reduced, thus resulting in the reduction of the heat sink requirement for the overall circuit (i.e., higher compactness and

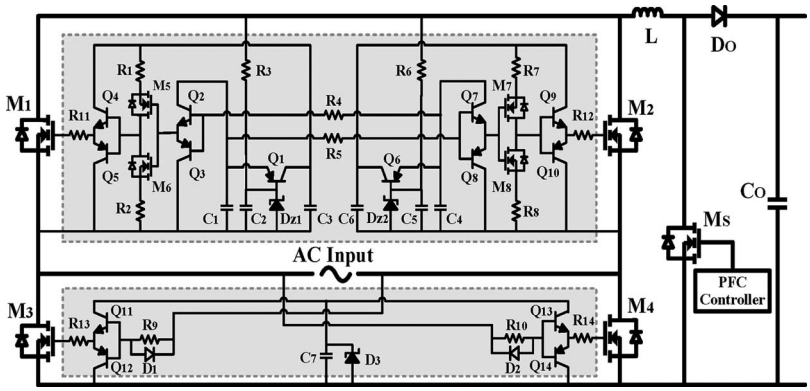

Fig. 23. Modified boost-type power factor correction circuit, with the diode rectifier replaced by an SDSR.

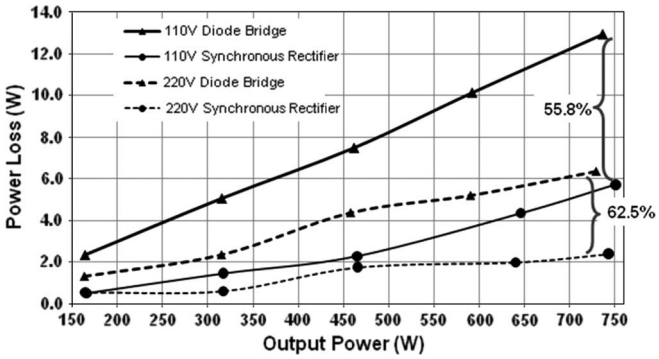

Fig. 24. Power loss comparison of the diode rectifier and the proposed SDSR in the 750-W boost-type power factor correction circuit, with a constant switching frequency of 100 kHz.

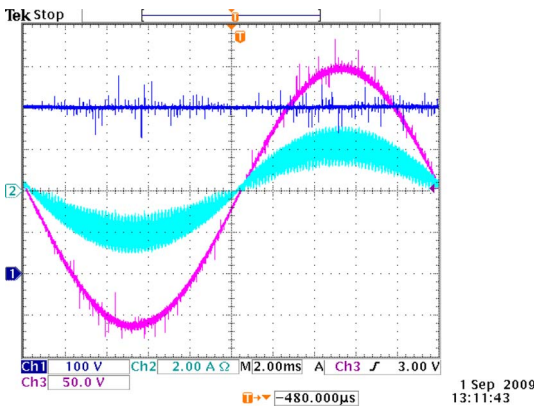

Fig. 25. (Pink) Input voltage, (green) input current, and (blue) output voltage of the boost-type power factor correction, with the diode rectifier replaced by the proposed SDSR.

power density) and also improvements in the system lifetime and reliability.

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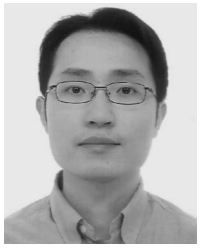

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