

# Adaptive high-bandwidth digitally controlled buck converter with improved line and load transient response

Albert T.L. Lee<sup>1</sup>, Johnny K.O. Sin<sup>1</sup>, Philip C.H. Chan<sup>2</sup>

<sup>1</sup>ECE Department, The Hong Kong University of Science and Technology, Hong Kong SAR, People's Republic of China

<sup>2</sup>Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Hong Kong SAR, People's Republic of China

E-mail: alee@ust.hk

**Abstract:** Digitally controlled switching converter suffers from bandwidth limitation because of the additional phase delay in the digital feedback control loop. To overcome the bandwidth limitation without using a high sampling rate, this study presents an adaptive third-order digital controller for regulating a voltage-mode buck converter with a modest  $2\times$  oversampling ratio. The phase lag because of the analogue-to-digital converter (ADC) conversion time delay is virtually compensated by providing an early estimation of the error voltage for the next sampling time instant, enabling a higher unity-gain bandwidth without compromising stability. An additional pair of low-frequency pole and zero in the third-order controller increases the low-frequency gain, resulting in faster settling time and smaller output voltage deviation during line transient. Both simulation and experimental results demonstrate that the proposed adaptive third-order controller reduces the settling time by 50% in response to a 1 V line transient and 30% in response to a 600 mA load transient, compared to the baseline static second-order controller. The fastest settling time is measured to be about 11.70  $\mu\text{s}$ , surpassing the transient performance of conventional digital controllers and approaching that of the state-of-the-art analogue-based controllers.

## 1 Introduction

As embedded technology proliferates in various electronic devices and systems, digital signal processors (DSPs), general-purpose CPUs, microcontrollers and field-programmable gate arrays (FPGAs) are becoming attractive options for power management in closed-loop control applications, demanding fast processing and feedback. There has been growing interest in digital controllers for switching converters because of their flexibility and reconfigurability to implement various control functions without hardware modification. Digital control is also less vulnerable to aging, noise, process and parameter variations. Despite the advantages of a digital controller over its analogue counterpart, a major challenge with a single-sampling digitally controlled switching converter is bandwidth limitation, which significantly degrades its transient performance. To surmount this bandwidth limitation, researchers have previously proposed the multi-sampling approach that uses a high sampling rate to reduce the overall phase lag in the digital control loop [1–5]. However, the drawbacks of increasing the sampling rate include higher dynamic power consumption, the injection of high-frequency noise into the feedback loop and the possibility of inducing undesirable limit-cycle oscillations.

In this paper, an adaptive third-order digital controller is proposed, to achieve both a large unity-gain bandwidth and

a high low-frequency gain. The proposed prediction scheme generates an early estimation of the error voltage one sampling cycle ahead of the actual measurement. It reduces the total phase lag by virtually eliminating the analogue-to-digital converter (ADC) sampling time delay in the digital feedback control loop, enabling the unity-gain bandwidth to be further extended out while maintaining robust stability margins. Two versions of the proposed prediction method, that is, static prediction (SP) and adaptive prediction (AP) are investigated. The former predicts the error voltage for the next sampling time instant by doing ordinary linear extrapolation using the two most recent samples while the latter also includes an error correction term to modulate the extrapolation function. Unlike the prediction schemes reported in the previous literatures [6–14], the proposed prediction method does not require a priori knowledge of any converter parameters. It only requires the sensing of the output voltage, which is subtracted from the reference voltage to become the error voltage. Therefore it is free from any modelling errors or uncertainties of system parameters. To increase the DC gain, a second-order digital controller [15] is transformed into the third-order one with an additional pair of low-frequency pole and zero. As a result, the line transient response can be improved considerably, resulting in 40–50% reduction in the settling time and more than 20% reduction in the maximum overshoot of the output voltage. The overall improvement of the closed-loop dynamic

performance for line transient response is more pronounced than that for load transient response.

A major benefit of the proposed predictive digital controller is that only a very low sampling rate is required to achieve fast transient response and a stable closed-loop system. Both the ADC and the digital controller are clocked at only twice the switching frequency of the buck converter. The simplicity of the controller design and its ability to enhance the dynamic performance make it especially appealing for practical applications.

The paper is organised as follows: Section 2 explains the purpose of the proposed prediction scheme and shows its effectiveness in reducing the phase lag in the digital feedback loop. Section 3 presents the algorithm for the proposed prediction control scheme. Section 4 performs small-signal analysis with the proposed predictive digital controller. Section 5 contains the simulation results for the line and load transient response. Section 6 presents the experimental results. The conclusion is given in Section 7.

## 2 Purpose of the proposed prediction scheme

Digitally controlled buck converter in single-sampling strategy suffers from bandwidth limitation because of the additional phase delay along the digital feedback path. The sample-and-hold action from the ideal sampler and the digital pulse width modulator (DPWM) introduces a phase lag of  $\omega DT_s$ , where  $D$  and  $T_s$  represent the steady-state duty ratio of a buck converter and the switching period, respectively. The ADC conversion time and the computational delay of the digital controller further increase the phase lag by  $\omega t_d$ , where  $t_d$  represents the total time delay in the digital control loop. Hence, the total phase lag  $\phi_T$  [15] can be expressed as

$$\phi_T = \omega DT_s + \omega t_d = 2\pi D \frac{f_{UGF}}{f_s} + 2\pi n \frac{f_{UGF}}{f_s} = 2\pi \frac{f_{UGF}}{f_s} (D + n) \tag{1}$$

$f_{UGF}$  is the unity-gain frequency,  $f_s$  is the switching frequency, and  $n$  is a fractional number ( $n = t_d/T_s$ ). In conventional single-sampling approach, the output voltage in a voltage-mode buck converter is sampled by the ADC exactly once per switching period to generate a new digital error signal  $E[n]$ . The error signal is then processed by the digital controller and the output of the digital controller goes into the DPWM to produce a constant-frequency duty-ratio signal to control the switching of the power transistors. The timing diagram of the single-sampling strategy with trailing-edge modulation is shown in Fig. 1.

The ADC conversion time is usually predetermined for a given ADC part. The total digital delay is assumed to be no more than half the switching period (i.e.  $t_d \leq 1/2T_s$ ). A new duty ratio is generated at the rising edge of the 1 MHz system clock. Therefore, the duty ratio from the previous switching cycle is always updated a cycle later. Assuming  $f_{UGF}/f_s = 1/9$  and  $D = 0.6$ , the total phase lag  $\phi_T$  in (1) is calculated to be  $44^\circ$ , which severely degrades the stability of the system. In order to maintain sufficient phase margin, the bandwidth of the system has to be reduced at the expense of a much slower transient response. Another possibility is to double the sampling rate by sampling the output voltage twice per switching period. The timing diagram of the double-sampling strategy is depicted in Fig. 2.

The delay times from the three most common types of DPWM modulation have been reported in [16]. For certain duty ratios, trailing-edge modulation is preferred over the symmetric-on time modulation in the double-update scheme because of its smaller equivalent delay across the DPWM. For instance, for  $D = 0.6$ , the delay times for the trailing-edge modulation and the symmetric-on time modulation are  $T_s/10$  and  $T_s/4$ , respectively.  $\phi_T$  is calculated to be  $24^\circ$  for the double-sampling case. In other words, the phase margin increases by  $20^\circ$ . Nonetheless, a phase lag of  $24^\circ$  is quite large especially if a higher bandwidth is required. Hence, it leads to the investigation of the proposed prediction method in which the error voltage for the next sampling method instant is estimated one cycle earlier. The main objective is to provide the necessary phase boost by eliminating the time delay  $t_d$  in the digital

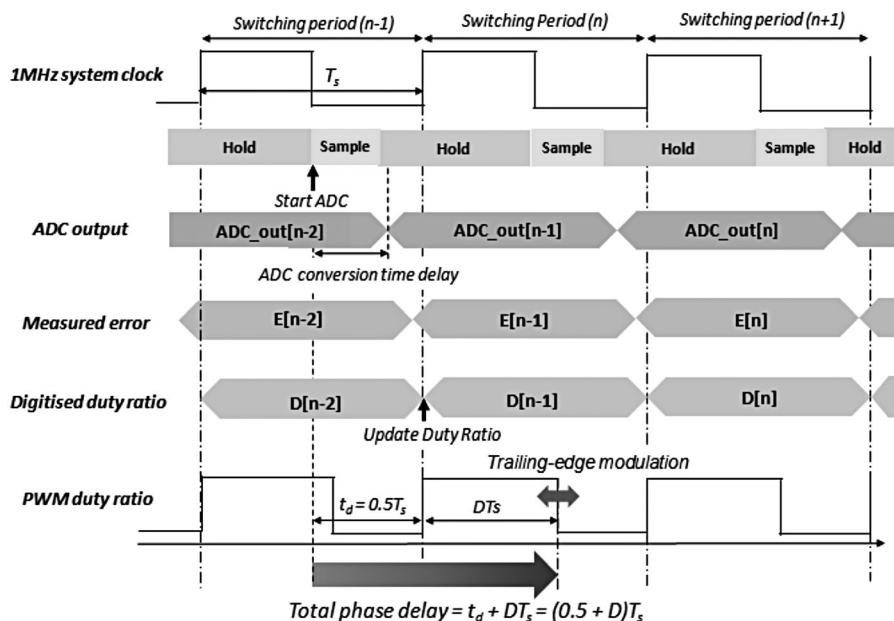


Fig. 1 Timing diagram of the single-sampling digital control strategy

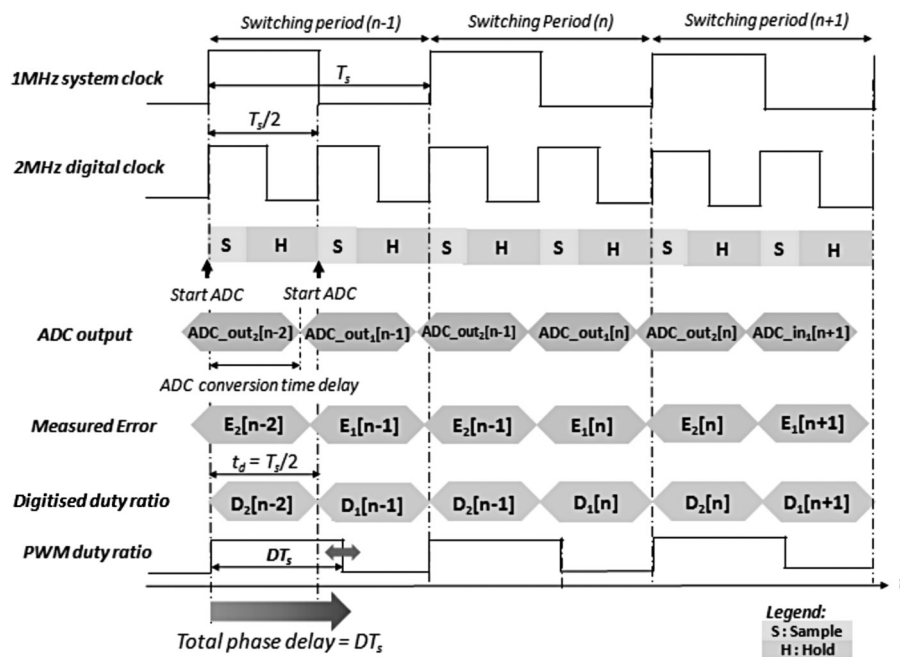


Fig. 2 Timing diagram of the double-sampling digital control strategy

feedback loop, thereby enabling sufficient stability margin at a larger unity-gain bandwidth. Fig. 3 shows the timing diagram of the modified double-sampling strategy with one-sample-ahead error prediction.

In the proposed error prediction method, the duty ratio  $D[n]$  is generated a sampling period earlier. This can be realised by estimating the error signal  $E^{\wedge}[n]$  one sampling cycle earlier. The total phase delay is reduced to  $T_s/10$ , which translates to a sufficiently small phase lag of  $4^\circ$ . The phase margin is increased by  $20^\circ$  with respect to the original double-sampling approach. In general, the total phase lag  $\phi_T$  can be expressed in terms of the duty ratio  $D$  and the

oversampling ratio  $N$  in (2) with trailing-edge modulation.

$$\phi_T = 2\pi \left( D - \frac{\text{floor}(ND)}{N} \right) \frac{f_{UGF}}{f_s} \quad (2)$$

In particular,  $N=2$  for the double-sampling case. Hence, by substituting  $N=2$ ,  $D=0.6$  and  $f_{UGF}/f_s = 1/9$  into (2),  $\phi_T$  is calculated to be  $4^\circ$ . It should be noted that a higher unity-gain bandwidth at a fixed switching frequency results in only a modest increase in the total phase lag. For instance, if  $f_{UGF}/f_s$  is increased from  $1/9$  to  $1/5$ ,  $\phi_T$  increases by only

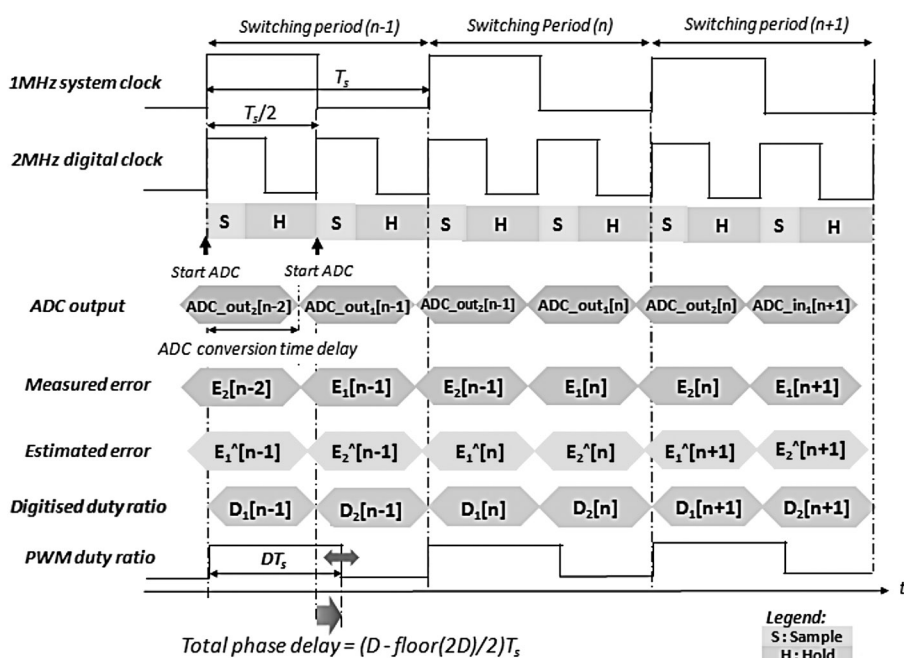


Fig. 3 Timing diagram of the modified double-sampling digital control strategy with prediction

3.2°. The trailing-edge modulation produces a smaller  $\phi_T$  than the symmetric-on time modulation for  $0 \leq D < 0.25$  and  $0.5 \leq D < 0.75$  [16]. Since the duty ratio of the proposed buck converter is 0.6, trailing-edge modulation is used here. It is also interesting to note that the same prediction scheme can also be applied to the single-sampling strategy. By substituting  $N=1$ ,  $D=0.6$  and  $f_{\text{UFG}}/f_s = 1/9$  into (2), the total phase lag  $\phi_T$  is reduced from  $44^\circ$  to  $24^\circ$ .

### 3 Algorithm of the proposed SP and AP control schemes

Fig. 4 shows the block diagram of the proposed digitally controlled voltage-mode buck converter. The predictor is implemented as a two-tap finite impulse response (FIR) filter. It periodically monitors the digital error signal  $E[n]$ , which is the difference between the digital reference  $V_{\text{ref}}[n]$  and the digitised feedback voltage  $V_{\text{fb}}[n]$ . The two most recent known error signals are used to estimate the future error for the next sampling cycle. A prediction error correction signal  $\Delta E_c[n]$  is also defined as the difference between the actual measured error and the predicted error in the present sampling cycle. The prediction error always stays within a very small window centred at zero in steady state (determined by the value of  $\varepsilon$ ) since the difference between the actual error and the predicted error is negligible. Simple fixed linear extrapolation can therefore be used to estimate the future error based on the last two error samples and is referred to as static prediction (SP). However, when the closed-loop system is perturbed by a transient, the prediction error goes beyond the steady-state window tending to a sudden change in the actual error. To enable better tracking of the predicted error with the actual error, the ordinary linear extrapolation is adjusted by the error correction term multiplied by a fudging factor  $1/2^k$  (where  $k$  is a positive integer). This is referred to as adaptive prediction (AP). Mathematically, the AP control law is defined as

$$E_1^{\wedge}[n+1] = 2E_2[n] - E_1[n] \pm \frac{1}{2^k} |\Delta E_c[n]| \quad (3)$$

$$\Delta E_c[n] = E_2[n] - E_2^{\wedge}[n] \quad (4)$$

The predicted error  $E_1^{\wedge}[n+1]$  is a linear combination of the last two known errors modulated by the error correction term

$\Delta E_c[n]$ . To ensure a conditionally stable system during transient,  $\Delta E_c[n]$  is bounded such that  $|\Delta E_c[n]| \leq E_2[n]$ . By defining  $E_1[n] = m \times E_2[n]$ , where  $0 \leq m \leq 2$ , (3) and (4) can be rewritten as (5) and (6), respectively.

$$E_1^{\wedge}[n+1] = \left(2 + \frac{1-m}{2^k}\right) \times E_2[n] - E_1[n] \quad (5)$$

$$\Delta E_c[n] = (1-m) \times E_2[n] \quad (6)$$

Intuitively, the error correction term dynamically adjusts the slope of the linear extrapolation function to achieve fast convergence of the estimated error towards the real error. For a particular value of  $k$ , the first coefficient  $a_1$  of the AP function in (5) is being modulated by the value of  $m$ , that is,  $(2 - 1/2^k) \leq a_1 \leq (2 + 1/2^k)$  whereas the second coefficient,  $a_0$ , has a fixed value of  $-1$ . In other words,  $a_1$  and  $a_0$  become the coefficients of a two-tap FIR filter. This FIR filter is adaptive since the value of its leading coefficient  $a_1$  changes during transient. In general, a higher unity-gain bandwidth results in faster transient response in the closed-loop system, provided that there is sufficient stability margin [17]. Several modified versions of proportional–integral–differential (PID) controllers [18, 19] have been proposed to increase the bandwidth during transient for improved performance while reverting to a lower bandwidth with increased phase margin in steady state. However, these adaptive PID controllers [18, 19] require the maintenance of two unique sets of gains, namely one set for transient and another set for steady state, with a total of six variables. The selection and optimisation of the PID gains is rather *ad hoc* and depends largely on the accuracy of the small-signal modelling from prior knowledge of the system. On the contrary, the proposed predictor does not require any predetermination of the FIR filter coefficients. The only design variable is  $k$  in (5) which defines the lower and upper bound of the leading coefficient  $a_1$  in the FIR filter. Given a particular value of  $k$ ,  $a_1$  is adaptively determined online during the operation without requiring any prior knowledge of system parameters such as input and output voltages, inductor and output capacitor values. It leads to a much simpler design and is less prone to any modelling errors or parameter variations. The value of  $k$  is chosen such that the unity-gain bandwidth is

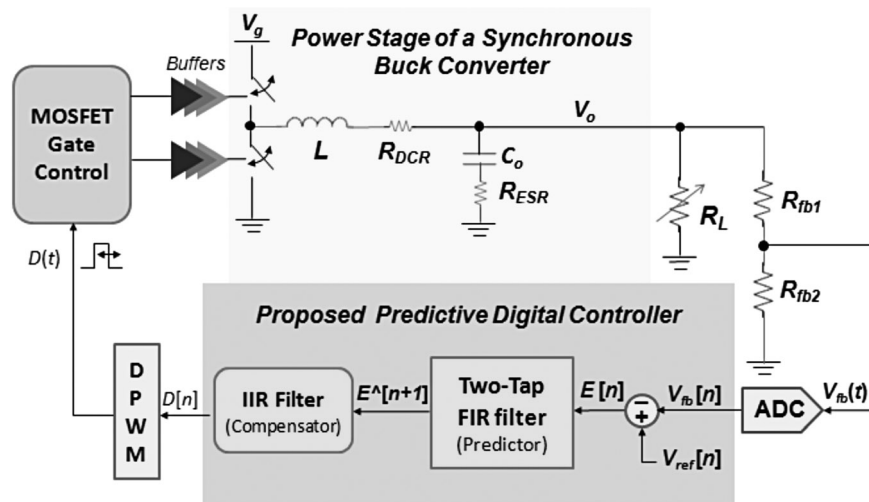
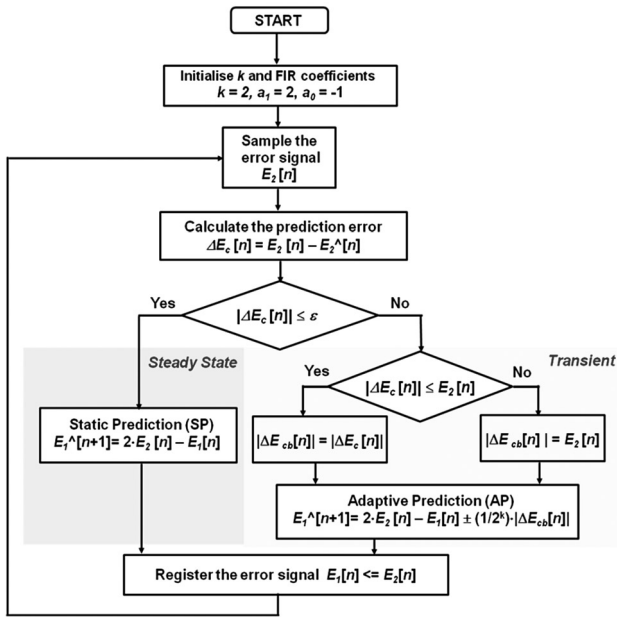


Fig. 4 Block diagram of the proposed digitally controlled voltage-mode buck converter

**Table 1** Design specification for the proposed low-voltage buck converter

| Parameter  | Value | Unit             |
|--|-------|------------------|
| input voltage ( $V_g$ )                            | 3     | V                |
| output voltage ( $V_o$ )                           | 1.8   | V                |
| inductor ( $L$ )                                   | 4.7   | $\mu\text{H}$    |
| inductor DCR ( $R_{\text{DCR}}$ )                  | 200   | $\text{m}\Omega$ |
| output capacitor ( $C_o$ )                         | 4.7   | $\mu\text{F}$    |
| capacitor ESR ( $R_{\text{ESR}}$ )                 | 50    | $\text{m}\Omega$ |
| maximum load step ( $\Delta I_{\text{LOAD,max}}$ ) | 600   | $\text{mA}$      |
| switching frequency ( $f_s$ )                      | 1     | $\text{MHz}$     |



**Fig. 5** Simplified flowchart showing the algorithm for the proposed prediction method

increased for faster response during transient while maintaining a phase margin above  $45^\circ$  [19–21]. The limits of  $k$  will be discussed in Section 4. Towards the end of a transient response, the magnitude of the prediction error  $|\Delta E_c[n]|$  should eventually fall within the small window centred at zero, indicating that the system has reached the steady-state condition. Hence,  $m=1$  in (6) since  $E_2^{\hat{}}[n] \simeq E_2[n]$ . The AP controller essentially becomes the SP controller in quiescent operation condition. Fig. 5 shows the simplified flowchart of the algorithm for the proposed prediction method.

#### 4 Small-signal analysis with the predictive digital controller

A small-signal model in the discrete-time domain is derived to investigate the stability and transient performance of the proposed digital controller for regulating a voltage-mode buck converter operating in continuous conduction mode. Table 1 shows the target specification of the proposed buck converter for low-voltage portable applications.

The direct digital design methodology [22] is employed in designing the proposed digital controller. First, the equivalent discrete-time transfer function of the continuous-time power stage of a buck converter is determined. Second, the proposed digital controller is designed directly in the discrete-time domain using the standard Bode plot analysis. This method offers the modelling convenience by representing the total delay of the digital control loop in the continuous-time domain prior to controller design. Hence, the ADC and the digital controller can be treated as if they

were delay-free. It enables the compensated pole and zero assignments of the digital controller to be performed directly in the  $z$ -domain, leading to a more predictable and consistent result from modelling to implementation. Fig. 6 depicts the small-signal model with the proposed digital controller.

The output voltage sensing and conditioning circuitry is modelled as  $H_{\text{sense}}(s)$ , which is represented by the feedback resistor divider ratio,  $R_{\text{fb}2}/(R_{\text{fb}1} + R_{\text{fb}2})$ , from Fig. 5. Let  $R_{\text{fb}1} = R_{\text{fb}2}$  and  $H_{\text{sense}}(s) = 1/2$ . The DPWM is inherently a uniformly sampled modulator, since the input modulating signal  $V_{\text{fb}}(t)$  undergoes a sample-and-hold action before being compared to the carrier signal  $V_c(t)$ . Its small-signal transfer function can be represented as

$$G_{\text{DPWM}}(s) = \frac{D(s)}{M(s)} = \frac{1}{V_{c,pp}} e^{-st_d(D,N)} \quad (7)$$

For trailing-edge modulation, the DPWM modulator delay  $t_d$  is a function of the duty ratio  $D$  and the oversampling ratio  $N$  [16].  $V_{c,pp}$  represents the amplitude of the carrier signal  $V_c(t)$ . For simplicity, it is assumed to be unity. The continuous-time transfer function of the uncompensated loop gain (uncompensated loop gain is defined as the loop gain with unity compensator gain, that is,  $G_c(s) = 1$  [20]) can be expressed as

$$T_U(s) = G_{\text{DPWM}}(s)G_{\text{vd}}(s)H_{\text{sense}}(s) e^{-s\Delta t_{\text{digital}}} \quad (8)$$

By substituting (7) and  $H_{\text{sense}}(s) = 1/2$  into (8), we have

$$\begin{aligned} T_U(s) &= \frac{1}{2} G_{\text{vd}}(s) e^{-s(t_d(D,N) + \Delta t_{\text{digital}})} \\ &= \frac{1}{2} G_{\text{vd}}(s) e^{-s(\Delta t_{d,\text{total}})} \end{aligned} \quad (9)$$

$G_{\text{vd}}(s)$  represents the control-to-output transfer function, which can be written as (see (10))

Equation (10) can be approximated as (11) by neglecting the on-resistance of the power switches  $R_{\text{sw}}$  and the DC resistance

$$\begin{aligned} G_{\text{vd}}(s) &= \frac{\hat{v}_o}{\hat{d}} = V_g \cdot \left( \frac{R_{\text{LOAD}}}{R_{\text{LOAD}} + R_{\text{ESR}}} \right) \\ &\cdot \left( \frac{1 + sC_oR_{\text{ESR}}}{((R_{\text{LOAD}} + R_{\text{sw}} + R_{\text{DCR}})/(R_{\text{LOAD}} + R_{\text{ESR}})) + s(((L + C_oR_{\text{ESR}}R_{\text{LOAD}})/(R_{\text{ESR}} + R_{\text{LOAD}})) + C_oR_{\text{sw}} + C_oR_{\text{DCR}}) + s^2LC} \right) \end{aligned} \quad (10)$$

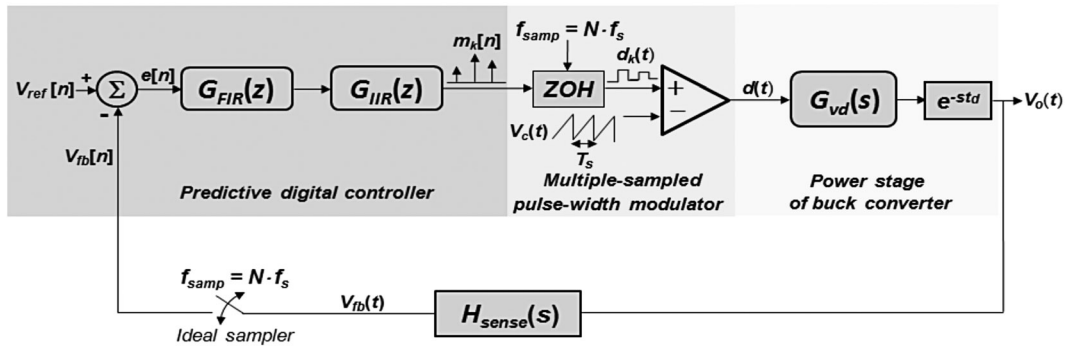


Fig. 6 Small-signal model with the proposed digital controller

of the inductor  $R_{DCR}$ .

$$G_{vd}(s) \approx \frac{V_g(1 + sC_o R_{ESR})}{1 + s((L/R_{LOAD}) + C_o R_{ESR}) + s^2 LC_o(1 + (R_{ESR}/R_{LOAD}))} \quad (11)$$

The equivalent small-signal z-domain model for the uncompensated loop gain in double-sampled loop is given by

$$T_U(z) = \frac{T_s}{2} Z_{(T_s/2)} \left[ \frac{1}{2} G_{vd}(s) e^{-s(\Delta t_{d, total})} \right] \quad (12)$$

where  $Z_{T_s/N} [ \cdot ]$  denotes the Z-transform operator with the switching period being an integer multiple of the sampling

period. The discretisation of the uncompensated loop gain in (12) can be computed conveniently using the c2d command from the MATLAB control toolbox. For a light load current of 50 mA, the z-domain transfer function in (12) is obtained as

$$T_U(z) = z^{-1} \times \frac{0.007789z^2 + 0.004162z - 0.0008149}{z^2 - 1.959z + 0.9699} \quad (13)$$

The proposed digital controller consists of the predictor and the digital compensator. The z-domain transfer function of the static predictor based on the proposed SP scheme is given by

$$G_{FIR}(z) = 2 - z^{-1} \quad (14)$$

It can be realised as a simple two-tap FIR filter with a fixed set of coefficients [2, -1]. In addition, a second-order digital compensator generates a dominant pole  $\omega_{p0}$  at DC to provide the integral action and two zeros ( $\omega_{z2}, \omega_{z3}$ ) to offset the complex resonant poles from the LC output filter in the power stage of the buck converter. The two compensated zeros enable the unity-gain bandwidth to be extended beyond the complex resonant pole frequency  $\omega_{LCO}$ . A high-frequency pole  $\omega_{p2}$  from the inverse impulse response (IIR) filter is offset by the high-frequency zero  $\omega_{z4}$  from the FIR filter. The digital compensator is implemented as a

Table 2 Stability margin and unity-gain frequency between light load and heavy load current conditions

| Parameter                   | Light load current, (50 mA) | Heavy load current, (650 mA) |
|-----------------------------|-----------------------------|------------------------------|
| phase margin, deg           | 50.12                       | 56.37                        |
| gain margin, dB             | 17.65                       | 18.00                        |
| unity-gain frequency, rad/s | $6.94 \times 10^5$          | $6.80 \times 10^5$           |

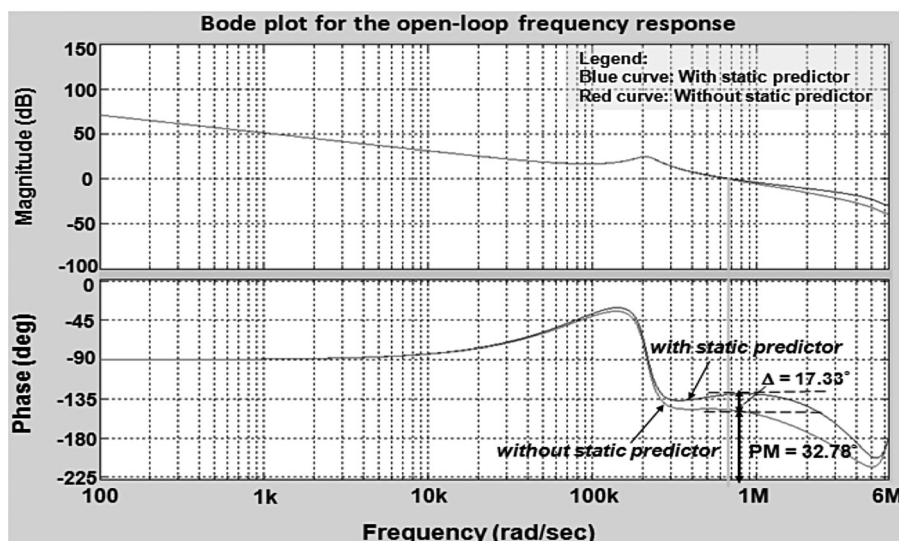


Fig. 7 Open-loop Bode plot (with and without static predictor) in light load current condition

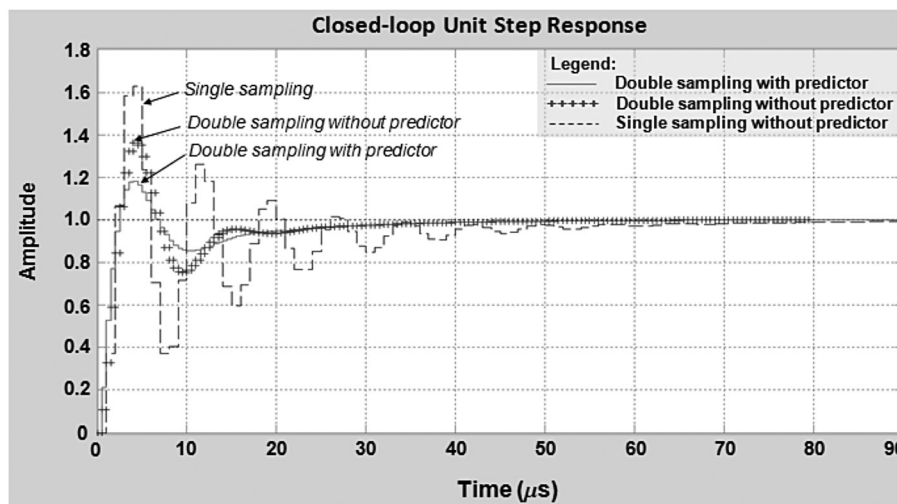


Fig. 8 Unit step response for single-sampling loop, double-sampling loop and double-sampling loop with static predictor under light load current condition

three-tap IIR filter. The  $z$ -domain transfer function for the second-order digital compensator is obtained as

$$G_{IIR}(z) = \frac{9.166 - 16.69z^{-1} + 7.582z^{-2}}{1 - 1.516z^{-1} + 0.5156z^{-2}} \quad (15)$$

Hence, the  $z$ -domain transfer function of the loop gain can be expressed as

$$T(z) = T_u(z)G_{FIR}(z)G_{IIR}(z) \quad (16)$$

Table 2 summarises the phase margin, gain margin and unity-gain frequency for the light load current ( $I_{LOAD} = 50$  mA) and heavy load current ( $I_{LOAD} = 650$  mA) conditions from the Bode plot analysis. It shows that the system has

sufficient stability margins within the operating load current range.

It is interesting to note that if the static predictor in (14) is removed from the double-sampled control loop, the phase margin is reduced by more than  $17^\circ$ . In the case of light load current, the phase margin drops to  $32.78^\circ$  ( $<45^\circ$ ) as illustrated in Fig. 7. The degradation of the phase margin is caused by the absence of the compensated zero  $\omega_{z4}$ . This shows the importance of the static predictor in stabilising a high-bandwidth system by providing the necessary phase boost.

The unit-step response from the proposed static predictor is compared with those from the original single-sampling and double-sampling loops without prediction. Fig. 8 shows that the unit-step response of the single-sampling loop is highly oscillatory due to poor stability margins. The maximum overshoot in the unit-step response from the original

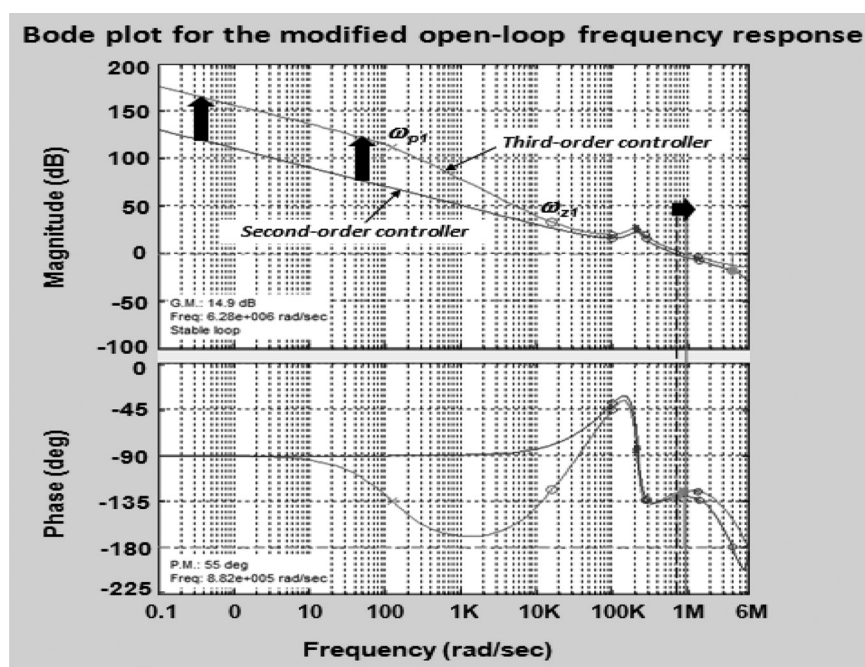


Fig. 9 Modified open-loop Bode plot with a higher DC gain and larger unity-gain bandwidth

single-sampling loop is more than 35% larger than that from the modified double-sampling loop with prediction. The proposed static predictor leads to improved dynamics with sufficiently damped and fast transient response. It has a maximum overshoot within 20% and a 2% settling time of 33  $\mu$ s.

It is also useful to study the effects of an input disturbance on the closed-loop system. Such kind of input disturbance is equivalent to a change in the input (line) voltage which is also referred to as line transient. In general, the continuous-time transfer function of the input disturbance to the output is expressed as

$$G_{oi}(s) = \frac{\hat{v}_o}{\hat{v}_i} = \frac{G_{vd}(s)}{1 + T(s)} = \frac{G_{vd}(s)}{1 + T_u(s)G_c(s)} \quad (17)$$

where  $T(s)$  is the compensated loop gain,  $T_u(s)$  is the uncompensated loop gain,  $G_{vd}(s)$  is the transfer function of the power stage of the buck converter and  $G_c(s)$  is the transfer function of the digital controller. Ideally,  $|G_{oi}(s)|$  should be zero for maximum input noise rejection. Since  $G_{vd}(s)$  and  $T_u(s)$  are usually predetermined by the design specification, the only design variable in (17) is  $G_c(s)$ . To achieve a strong rejection of the input disturbance, the DC gain of  $G_c(s)$  needs to be increased considerably, which implies  $|T(s)| \gg 1$ . This can be accomplished by inserting a pair of low-frequency pole and zero ( $\omega_{p1}$ ,  $\omega_{z1}$ ) to raise the DC gain by at least 50 dB. The unity-gain frequency is also increased to  $8.8 \times 10^5$  rad/s, which is around one-seventh of the switching frequency. The phase margin is 55° and the gain margin is 14.9 dB for the light load current condition. Fig. 9 shows the Bode plots of the modified open-loop frequency response.

This additional pole-zero pair transforms the second-order digital compensator in (15) into a third-order one whose transfer function is obtained as

$$G_{IIR3}(z) = \frac{12.5 - 35.14z^{-1} + 32.89z^{-2} - 10.25z^{-3}}{1 - 2.515z^{-1} + 2.03z^{-2} - 0.5153z^{-3}} \quad (18)$$

In Fig. 9, the loop gain with the third-order controller rolls off at -20 dB/dec from DC to the low-frequency pole  $\omega_{p1}$ . The gain slope then increases to -40 dB/dec between  $\omega_{p1}$  and  $\omega_{z1}$ . Once the radian frequency becomes larger than  $\omega_{z1}$ , the gain slope returns to -20 dB/dec. The placement of this

particular pole-zero pair gives the designer an extra degree of freedom to increase the low-frequency gain in order to reduce the maximum deviation from steady state. Fig. 10 compares the unit-step response between the second-order and third-order controllers when an input disturbance is injected into the closed-loop system. The overshoot from a third-order controller is much less pronounced than that from its second-order counterpart. Hence, the former offers a much stronger input noise rejection and faster settling to zero error than the latter.

The pure static predictor is replaced with the adaptive one based on the proposed AP scheme. The value of  $k$  in (5) needs to be selected carefully in such a way that the closed-loop system remains stable under the target operating conditions. Suppose  $k=1$  for  $\Delta E_c[n] \geq \epsilon$  and  $k=2$  for  $\Delta E_c[n] < \epsilon$ , where  $\epsilon$  is chosen to be 1/32 which is a reasonably small deviation from the steady-state condition. Also,  $|\Delta E_c[n]| \leq E_2[n]$ . Hence, the lower and upper bound of  $E_1[n+1]$  in (5) is given by

$$1.75E_2[n] - E_1[n] \leq E_1[n+1] \leq 2.5E_2[n] - E_1[n] \quad (19)$$

The discrete-time transfer function of the adaptive FIR filter can be expressed as

$$G_{FIR}(z) = a_1 - z^{-1}, \quad \text{for } 1.75 \leq a_1 \leq 2.5 \quad (20)$$

For fixed-point implementation,  $a_1$  is a binary number. Small-signal analysis is performed at the two limits of  $a_1$  to verify the stability of the closed-loop system within the entire operating range. Table 3 summarises the stability margins and the unity-gain frequencies at the maximum and minimum values of  $a_1$  for the light and heavy load current conditions.

As a rule of thumb, a phase margin of at least 45° and a gain margin above 10 dB is required for a robust design [18–21]. Hence, the phase and gain margins in each corner case are shown to satisfy their corresponding minimum requirement, confirming that the system is stable.

The leading coefficient  $a_1$  of the adaptive FIR filter determines the location of the high-frequency zero  $\omega_{z4}$  in the open-loop frequency response. As  $a_1$  becomes larger, the high-frequency zero  $\omega_{z4}$  is shifted to higher frequencies, which increases the unity-gain bandwidth and reduces the phase margin. The phase margin is below 45° for  $a_1 \geq 2.75$ .

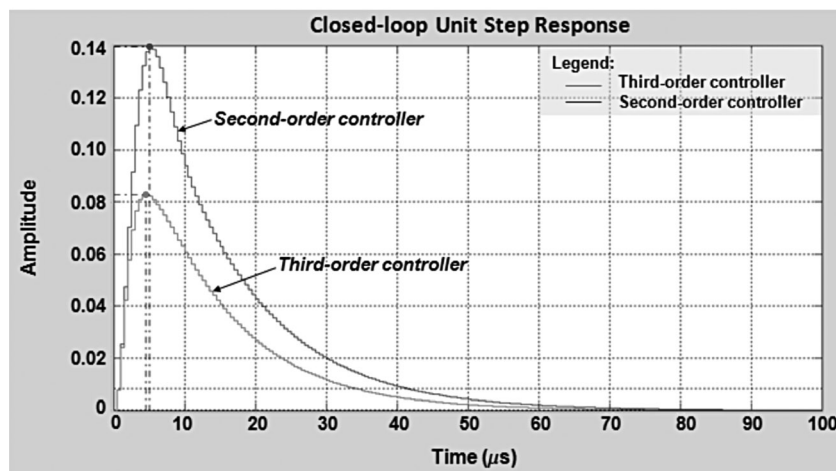


Fig. 10 Unit-step response due to an input disturbance between the third-order controller and the second-order controller



**Table 3** Stability margin and unity-gain frequency at the two limits of  $a_1$

| Parameter                   | Light load current, (50 mA) |                    | Heavy load current, (650 mA) |                    |
|-----------------------------|-----------------------------|--------------------|------------------------------|--------------------|
|                             | $a_1 = 1.75$                | $a_1 = 2.5$        | $a_1 = 1.75$                 | $a_1 = 2.5$        |
| phase margin, deg           | 58.53                       | 48.62              | 64.24                        | 52.30              |
| gain margin, dB             | 15.65                       | 13.55              | 15.74                        | 13.64              |
| unity-gain frequency, rad/s | $7.34 \times 10^5$          | $1.15 \times 10^6$ | $7.18 \times 10^5$           | $1.13 \times 10^6$ |

Hence, the value of  $a_1$  cannot exceed 2.5 for a robust system with sufficient stability margins. Conversely, as  $a_1$  becomes smaller, the high-frequency zero  $\omega_{z4}$  is shifted to lower frequencies which reduces the unity-gain bandwidth and increases the phase margin. The unity-gain bandwidth is reduced by more than 15% if  $a_1 < 1.75$ , making the transient response slower. Hence, the lower and upper limits of  $a_1$  are determined to be 1.75 and 2.5. The bottom line is that the stability of the system must not be compromised with the chosen range of  $a_1$ .

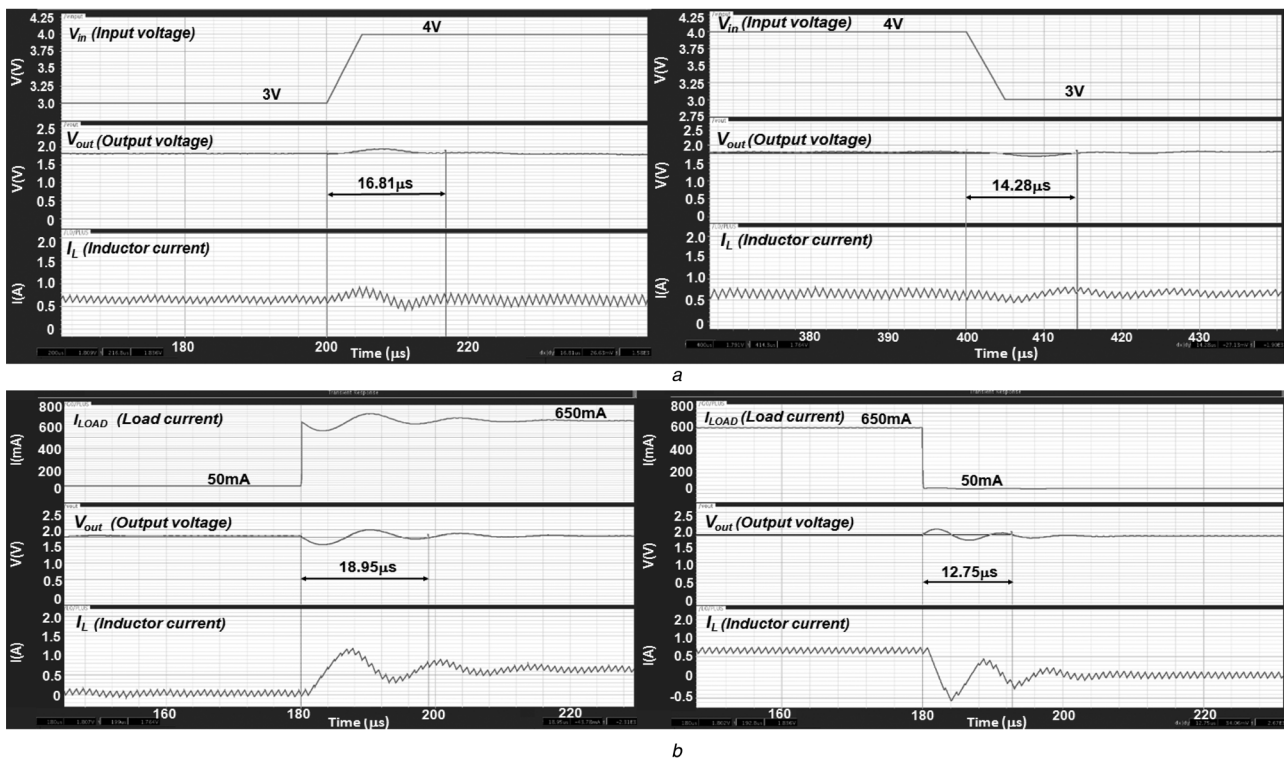
### 5 Line and load transient simulation

A time-domain macro model for the closed-loop system with the proposed digitally controlled buck converter is created according to the design specification in Table 1. It is used to examine the line and load transient response of the closed-loop system. The first-order FIR filter and second-order (or third-order) IIR filter are implemented in Verilog RTL. The power stage of the buck converter is modelled as ideal circuit elements, including the parasitic

**Table 4** Summary of the simulation results in terms of the output voltage settling time and maximum deviation from the steady-state value with the four variants of the proposed digital controller

| Proposed digital controller                   | Line transient response |           | Load transient response |           |
|---|-------------------------|-----------|-------------------------|-----------|
|   | Step-up                 | Step-down | Step-up                 | Step-down |
| <i>2% Settling time, <math>\mu s</math></i>   |                         |           |                         |           |
| static prediction, second-order (SP2)         | 33.81                   | 28.61     | 29.25                   | 19.12     |
| static prediction, third-order (SP3)          | 21.96                   | 18.10     | 26.89                   | 17.15     |
| adaptive prediction, second-order (AP2)       | 27.78                   | 20.30     | 24.66                   | 15.13     |
| adaptive prediction, third-order (AP3)        | 16.81                   | 14.28     | 18.95                   | 12.75     |
| <i>Maximum deviation from steady state mV</i> |                         |           |                         |           |
| static prediction, second-order (SP2)         | 188                     | 169       | 277                     | 222       |
| Static prediction, third-order (SP3)          | 150                     | 121       | 268                     | 204       |
| adaptive prediction, second-order (AP2)       | 190                     | 172       | 277                     | 221       |
| adaptive prediction, third-order (AP3)        | 149                     | 117       | 250                     | 205       |

resistances such as output capacitor ESR, inductor DCR and the on-resistance of the power switches. The buck



**Fig. 11** Simulated step-up or step-down line and load transient responses with the adaptive third-order controller

- a Simulated line transient response
- b Simulated load transient response with the adaptive third-order controller

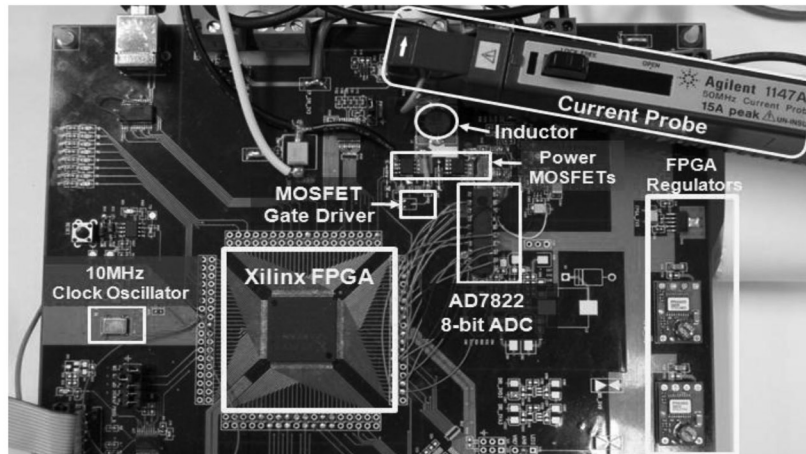
converter switches at 1 MHz while the 8-bit ADC is clocked at 2 MHz. Mixed-mode simulations are performed using Cadence SpectreVerilog simulator. The line transient response is simulated by introducing a 1 V step in the input voltage. The load transient response is simulated with a load step of 600 mA. Fig. 11 shows the simulated step-up or step-down line and load transient responses with the adaptive third-order controller.

The same line or load transient simulation is also performed with three other variants of the proposed digital

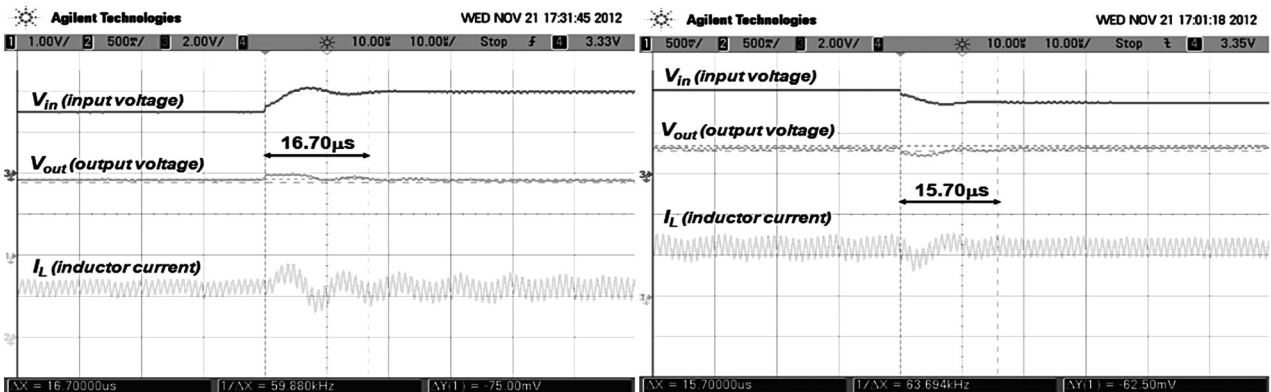
controllers for comparison. Table 4 summarises the simulation results.

The following observations can be made from Table 4.

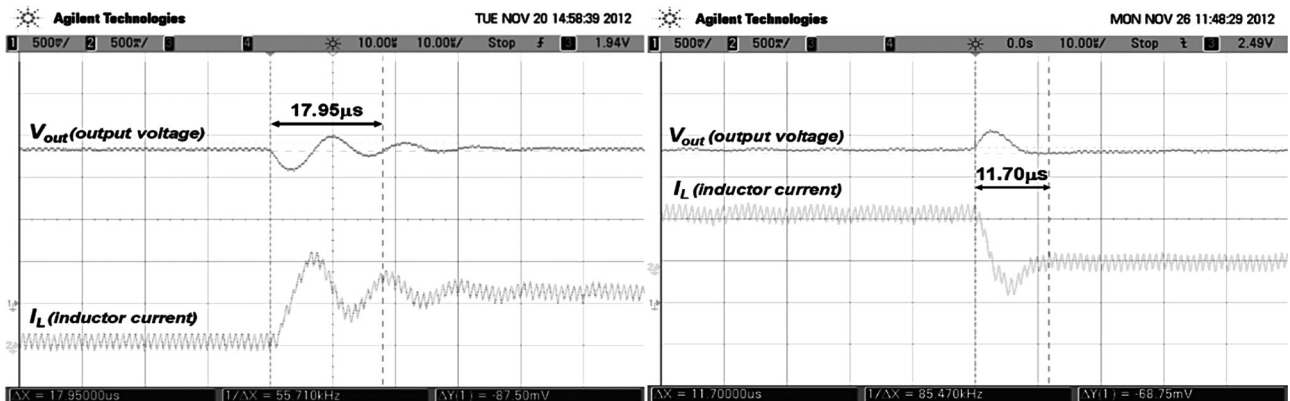
1. The AP3 controller reduces the settling time by 50% in line transient and more than 30% in load transient with respect to the baseline SP2 controller.
2. The third-order controller reduces the maximum deviation of output voltage from its steady-state value by 20–30% in



a



b



c

Fig. 12 Experimental verification

a FPGA-based hardware board for the proposed digitally controlled buck converter

b Actual line transient response with the adaptive third-order controller

c Actual load transient response with the adaptive third-order controller

**Table 5** Comparison of the measured settling times for the four variants of the proposed digital controller

| Proposed digital controller                | Line transient response |           | Load transient response |           |
|--|-------------------------|-----------|-------------------------|-----------|
|  | Step-up                 | Step-down | Step-up                 | Step-down |
| <i>2% Settling time, <math>\mu</math>s</i> |                         |           |                         |           |
| static prediction, second-order (SP2)      | 36.50                   | 26.20     | 28.50                   | 18.00     |
| static prediction, third-order (SP3)       | 23.74                   | 17.85     | 25.08                   | 14.60     |
| adaptive prediction, second-order (AP2)    | 30.20                   | 24.60     | 20.60                   | 15.50     |
| adaptive prediction, third-order (AP3)     | 16.70                   | 15.70     | 17.95                   | 11.70     |

line transient with respect to its second-order counterpart, regardless of whether static or adaptive prediction is used.

3. The maximum error from steady-state in line transient is much less pronounced than that in load transient. This is in consistent with the fact that the third-order controller has a stronger rejection of line noise because of an increased low-frequency gain.

## 6 Experimental verification

To verify the effectiveness of the proposed digital control scheme, an FPGA-based hardware prototype board shown in Fig. 12a is implemented based on the design specification in Table 1. The proposed digital controller is implemented in Xilinx Spartan-3E (XC3S250E) FPGA [23]. The algorithm of the proposed digital controller is described in Verilog hardware description language. The DPWM is realised in the form of a look-up table with a resolution of 3.8 ns by using the digital clock manager in the FPGA. An 8-bit ADC (AD7822 [24] from analogue devices) with a maximum throughput of 2 MSPS and a small input capacitance of less than 15 pF is used. The power stage of the buck converter is constructed using discrete integrated circuits for the two power switches (IRF7828 [25] from international rectifier) and a dual metal-oxide semiconductor field effect transistor gate driver (LTC4444 [26] from Linear Technology) together with surface-mount components for the inductor and output capacitors. Fig. 12b and c shows the actual waveforms for step-up (or step-down) line transient and load transient with the adaptive third-order controller, respectively. Table 5 compares the measured output settling times for all four variants of the proposed digital controller.

Table 5 shows that the AP3 controller produces the fastest transient response in all cases. It reduces the settling time by 40–50% in line transient and 30–35% in load transient with respect to the baseline SP2 controller. The experimental results are in close agreement with the simulation ones. The performance indices of the AP3 controller are compared with those reported in recent literature as summarised in Table 6. It shows that the proposed AP3 controller achieves the fastest settling time among the existing digital controllers [8, 18, 27–32]. Its performance is comparable with those of the state-of-the-art analogue-based controllers [33–37].

**Table 6** Summary of the actual output settling time of the proposed digital controller and prior arts

|                              | Compensator type  | Measured output voltage settling time ( $t_s$ ) | $t_s/T_s^a$ | Load step |
|------------------------------|---|---|-------------|-----------|
| Bibian and Jin [27]          | digital predictive dead-beat  | 2 ms  | 20          | 4 A       |
| Patella <i>et al.</i> [28]   | digital PID   | >70 $\mu$ s                                     | 70          | 500 mA    |
| Xiao <i>et al.</i> [29]      | digital PID   | about 100 $\mu$ s                               | 50          | 100 mA    |
| Chui <i>et al.</i> [30]      | digital PID   | about 50 $\mu$ s                                | 50          | 100 mA    |
| Carrejo <i>et al.</i> [31]   | predictive digital interpolation current control (PDICC)                | about 3 ms                                      | 210         | 700 mA    |
| Soenen <i>et al.</i> [32]    | first-order digital filter  | 1 ms  | 3125        | 200 mA    |
| Zhou <i>et al.</i> [8]       | improved digital peak current predictive control (IDPC)                 | 1180 $\mu$ s                                    | 59          | 1 A       |
| Arikatla <i>et al.</i> [18]  | adaptive digital PID (AD-PID)   | about 40–50 $\mu$ s                             | 14–18       | 7 A       |
| Lee <i>et al.</i> [33]       | analogue (high-pass notch filter)                                       | <16 $\mu$ s                                     | 16          | 500 mA    |
| Chen <i>et al.</i> [34]      | analogue (adaptive compensated error amplifier)                         | <25 $\mu$ s                                     | 12.5        | 400 mA    |
| Wu <i>et al.</i> [35]        | analogue pseudo-type III  | within 7 $\mu$ s                                | 7           | 500 mA    |
| Tseng <i>et al.</i> [36]     | analogue voltage-mode using ramp signal with variable DC-offset (RSVDC) | 10 $\mu$ s                                      | 7           | 800 mA    |
| Malcovati <i>et al.</i> [37] | analogue type III   | <20 $\mu$ s                                     | 50          | 1.9 A     |
| this work                    | adaptive third-order digital controller (AP3)                           | between 12 and 18 $\mu$ s                       | 12–18       | 600 mA    |

<sup>a</sup> $t_s/T_s$  represents the ratio of the settling time ( $t_s$ ) to the switching period ( $T_s$ )

## 7 Conclusion

This paper proposes an adaptive prediction scheme for digitally controlled buck converter which is demonstrated to be effective. Both the line and load transient responses are improved considerably even with a modest 2 $\times$  oversampling, thereby relaxing the requirement of the ADC. The increased low-frequency gain with the third-order controller enables a stronger rejection to line noise. The proposed digital controller does not require any passive components for loop compensation which reduces complexity and cost. It allows precise assignment of the compensated poles and zeros which are reconfigurable for various types of switching converters. Based on the theoretical analysis, simulation and experimental results, we conclude that the proposed adaptive third-order digital controller improves the transient dynamics with faster settling time and smaller deviation from steady state.

## 8 References

- Corradini, L., Mattavelli, P.: 'Analysis of multiple sampling technique for digitally controlled dc–dc converters'. Proc. IEEE 37th Annual

- Power Electronics Specialist Conf., PESC 2006, 18–26 June 2006, pp. 1–6
- 2 Tedeschi, E., Mattavelli, P., Trevisan, D., Corradini, L.: 'Repetitive ripple estimation in multi-sampling digitally controlled dc-dc converters'. 32nd Annual Conf. IEEE Industrial Electronics Society, IECON 2006, 7–10 November 2006, pp. 1685–1690
  - 3 Corradini, L., Mattavelli, P., Saggini, S.: 'Elimination of sampling-induced dead bands in multiple-sampled pulse width modulators for dc-dc converters'. 33rd Annual Conf. IEEE Industrial Electronics Society, IECON 2007, 5–8 November 2007, pp. 1495–1500
  - 4 Corradini, L., Mattavelli, P.: 'Modeling of multisampled pulse width modulators for digitally controlled dc-dc converters', *IEEE Trans. Power Electron.*, 2008, **23**, (4), pp. 1839–1847
  - 5 Corradini, L., Mattavelli, P., Tedeschi, E., Trevisan, D.: 'High bandwidth multisampled digitally controlled dc-dc converters using ripple compensation', *IEEE Trans. Ind. Electron.*, 2008, **55**, (4), pp. 1501–1508
  - 6 Odavic, M., Biagini, V., Zanchetta, P., Sumner, M., Degano, M.: 'One-sample-period-ahead predictive current control for high-performance active shunt power filters', *IET Power Electron.*, 2011, **4**, (4), pp. 414–423
  - 7 Su, J.-T., Liu, C.-W.: 'Gain scheduling control scheme for improved transient response of DC/DC converters', *IET Power Electron.*, 2012, **5**, (6), pp. 678–692
  - 8 Zhou, G., Xu, J., Jin, Y.: 'Improved digital peak current predictive control for switching DC-DC converters', *IET Power Electron.*, 2011, **4**, (2), pp. 227–234
  - 9 Sprock, D., Hsu, P.: 'Predictive discrete time control of switch-mode applications'. 28th Annual IEEE Power Electronics Specialists Conf., PESC 1997, 22–27 June 1997, pp. 175–181
  - 10 Bibian, S., Jin, H.: 'A simple prediction technique for the compensation of digital control time delay in dc switch mode power supplies'. 14th Annual Applied Power Electronics Conf. and Exposition, APEC 1999, 14–18 March 1999, pp. 994–1000
  - 11 Bibian, S., Jin, H.: 'Time delay compensation of digital control for dc switch mode power supplies using prediction techniques', *IEEE Trans. Power Electron.*, 2000, **15**, (5), pp. 835–842
  - 12 Chen, J., Prodic, A., Erickson, R.W., Maksimovic, D.: 'Predictive digital current programmed control', *IEEE Trans. Power Electron.*, 2003, **18**, (1), pp. 411–419
  - 13 Ferdowsi, M.: 'An estimative current mode controller for dc-dc converters operating in continuous conduction mode'. 21st Annual Applied Power Electronics Conf. and Exposition, APEC 2006, 19–23 March 2006, pp. 1133–1136
  - 14 Wan, K., Ferdowsi, M.: 'Reducing computational time delay in digital current-mode controllers for dc-dc converters'. IEEE 30th Int. Telecommunications Energy Conf., INTELEC 2008, 14–18 September 2008
  - 15 Lee, A.T.L., Ho Chan, P.C.: 'Adaptive prediction in digitally controlled buck converter with fast load transient'. The 13th IEEE Workshop on Control and Modeling for Power Electronics, COMPEL 2012, June 2012, pp. 1–7
  - 16 Corradini, L., Tedeschi, E., Mattavelli, P.: 'Advantages of the symmetric-on time modulator in multiple-sampled digitally controlled DC-DC converters'. Power Electronics Specialists Conf., PESC 2007, June 2007, pp. 1974–1980
  - 17 Chang, Y.-T., Lai, Y.-S.: 'Effect of sampling frequency of A/D converter on controller stability and bandwidth of digital-controlled power converter'. Seventh Int. Conf. Power Electronics, October 2007, pp. 625–629
  - 18 Arikatla, V.P., Abu Qahouq, J.A.: 'Adaptive digital proportional-integral-derivative controller for power converters', *IET Power Electron.*, 2012, **5**, (3), pp. 341–348
  - 19 Guo, L., Hung, J.Y., Nelms, R.M.: 'PID controller modifications to improve steady-state performance of digital controllers for buck and boost converters'. The 17th Annual IEEE Applied Power Electronics Conf. and Exposition, March 2002, pp. 381–388
  - 20 Erickson, R.W., Maksimovic, D.: *Fundamentals of Power Electronics*, Second Edition, University of Colorado, Boulder, Colorado, publishing as Springer Science+Business Media, LLC, 233 Spring Street, New York, 2001
  - 21 Mohan, N., Undeland, T.M., Robbins, W.P.: *Power electronics: converters, applications, and design* (Wiley, New York, 1995)
  - 22 Duan, Y., Jin, H.: 'Digital controller design for switch mode power converters'. 14th Annual Applied Power Electronics Conf. and Exposition, APEC 1999, March 1999, vol. 2, pp. 967–973
  - 23 Datasheet: Xilinx Spartan-3E FPGA Family, 'Spartan-3E FPGA Family Data Sheet'. Xilinx Inc. [Online] Available at: [http://www.xilinx.com/support/documentation/data\\_sheets/ds312.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds312.pdf)
  - 24 Datasheet: AD7822, '3 V/5 V, 2 MSPS, 8-Bit, 1-/4-/8-Channel Sampling ADCs'. Analog Devices Inc. [Online] Available at: [http://www.analog.com/static/imported-files/data\\_sheets/AD7822\\_7825\\_7829.pdf](http://www.analog.com/static/imported-files/data_sheets/AD7822_7825_7829.pdf)
  - 25 Datasheet: IRF7828, 'HEXFET® Power MOSFET for DC-DC Converters'. International Rectifier Corp. [Online] Available at: <http://www.irf.com/product-info/datasheets/data/irf7828pbf.pdf>
  - 26 Datasheet: LTC4444, 'High Voltage Synchronous N-Channel MOSFET Driver'. Linear Technology Corp. [Online] Available at: <http://cds.linear.com/docs/Datasheet/4444fb.pdf>
  - 27 Bibian, S., Jin, H.: 'High performance predictive dead-beat digital controller for dc power supplies', *IEEE Trans. Power Electron.*, 2002, **17**, (3), pp. 420–427
  - 28 Patella, B.J., Prodic, A., Zirger, A., Maksimovic, D.: 'High-frequency digital PWM controller IC for DC-DC converters', *IEEE Trans. Power Electron.*, 2003, **18**, (1), pp. 438–446
  - 29 Xiao, J., Peterchev, A., Zhang, J., Sanders, S.: 'An ultra-low-power digitally controlled buck converter IC for cellular phone applications'. 19th Annual Applied Power Electronics Conf. and Exposition, APEC 2004, 26 February 2004, pp. 383–391
  - 30 Yeung-Kei Chui, M., Ki, W.-H., Tsui, C.-Y.: 'A programmable integrated digital controller for switching converters with dual-band switching and complex pole-zero compensation', *IEEE J. Solid-State Circuits*, 2005, **40**, (3), pp. 772–780
  - 31 Carrejo, C.E., Vidal-Idiarte, E., Giral, R., Martinez-Salamero, L.: 'Predictive digital interpolation current control for DC-DC power converters', *IET Power Electron.*, 2009, **2**, (5), pp. 545–554
  - 32 Soenen, E.G., Roth, A., Shi, J., Kinyua, M., Gaiher, J., Ortynska, E.: 'A robust digital dc-dc converter with rail-to-rail output range in 40 nm CMOS'. 2010 IEEE Int. Solid-State Circuits Conf., 7–11 February 2010, pp. 198–199
  - 33 Lee, H., Mok, P.K.T., Ki, W.-H.: 'A novel voltage-control scheme for low-voltage DC-DC converters with fast transient recovery'. Proc. 2000 IEEE Int. Symp. Circuits and Systems (ISCAS), 2000, 28–31 May 2000, pp. 256–259
  - 34 Chen, K.-H., Huang, H.-W., Kuo, S.-Y.: 'Fast-transient DC-DC converter with on-chip compensated error amplifier', *IEEE Trans. Circuits Syst. II*, 2007, **54**, (12), pp. 1150–1154
  - 35 Wu, P.Y., Tsui, S.Y.S., Mok, P.K.T.: 'Area- and power-efficient monolithic buck converters with pseudo-type III compensation', *IEEE J. Solid-State Circuits*, 2010, **45**, (8), pp. 1446–1455
  - 36 Tseng, T.-J., Wu, C.-H., Chang-Chien, L.-R.: 'Fast transient voltage-mode buck regulator applying ramp signal with a variable DC-offset scheme', *IET Power Electron.*, 2012, **5**, (8), pp. 1408–1417
  - 37 Malcovati, P., Belloni, M., Gozzini, F., Bazzani, C., Baschirotto, A.: 'A 0.18  $\mu\text{m}$  CMOS 91%-efficiency 0.1-to-2A scalable buck-boost DC-DC converter for LED drivers'. 2012 IEEE Int. Solid-State Circuits Conf., Session 16, February 2012, no. 4, pp. 280–281