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Passivation of oxide traps in gallium arsenide (semiconductor) metal-oxide-semiconductor capacitor with high-k dielectric by using fluorine incorporation

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Gallium arsenide (semiconductor) (GaAs) metal-oxide-semiconductor capacitors with fluorine-incorporated TaHfON as gate dielectric are fabricated by pre- or postdeposition fluorine plasma treatment and their electrical and physical properties are compared with a control sample without the treatment. Among the three devices, the one with postdeposition fluorine treatment exhibits better characteristics: low oxide-charge density ($-3.5 \times 10^{12}\,cm^{-2}$), low interface-state density ($2.2 \times 10^{12}\,cm^{-2}eV^{-1}$), small flatband voltage (0.7 V), small hysteresis (45 mV), and good capacitance–voltage behavior. These should be attributed to (1) the passivating effects of fluorine atoms on the acceptorlike interface and near-interface traps, and (2) fluorine-induced suppressed growth of unstable Ga and As oxides on the GaAs substrate during postdeposition annealing. [http://dx.doi.org/10.1116/1.4927483]

I. INTRODUCTION

Future CMOS technology requires highly scaled devices and higher-speed circuits to meet the requirements of higher-performance and lower-power applications.[1] Much attention has been paid to exploring new materials capable of providing high drive current, with III–V compound semiconductor as one of the most promising materials to replace Si.[2,3] Gallium arsenide (semiconductor) (GaAs) metal-oxide-semiconductor (MOS) device with high-k (dielectric constant) gate dielectric has received significant efforts due to its larger bandgap and higher electron mobility than its Si counterpart.[4,5] Among the available high-k materials, TaHfO has been demonstrated to exhibit excellent electrical properties such as relatively high k value, peak electron mobility and crystallization temperature.[6,7] Fortunately, if nitrogen is incorporated in TaHfO, not only its k value could be increased, its oxide charges and border traps could also be reduced.[8] Moreover, effective nitrogen incorporation in high-k films could be achieved by annealing them in NH_3 at a relatively low temperature (~600 °C).[9] Therefore, TaHfON can be considered as a promising high-k gate dielectric.

However, a major concern of fabricating GaAs MOS device is that unstable native oxides are easily formed on the surface of the GaAs substrate, thus decreasing the effective k value of the gate dielectric and inducing high interface-state density (D_{it}) to pin the Fermi level at the gate-dielectric/GaAs interface.[10] Various interlayers made of Si,[11] Ge,[12] ZnO,[13] AlON,[14] TaON,[15] etc., have been tried in order to solve this problem and good results have been obtained. Besides, fluorine incorporation was reported to be capable of passivating the oxygen vacancies of high-k materials,[16] and so should be another good way for passivating the GaAs surface with simpler processing than the use of an interlayer.

Based on the facts above, GaAs MOS capacitors with TaHfON gate dielectric treated by fluorine plasma before or after the deposition of the high-k dielectric are fabricated in this work, and their electrical and interfacial characteristics are compared with those of a control sample without the treatment.

II. EXPERIMENT

MOS capacitors were fabricated on Si-doped n-type GaAs wafers (100) with a doping concentration of 0.5–1.0 $\times 10^{18}\,cm^{-3}$. Wafers were first degreased in acetone, ethanol and isopropanol, respectively, for 5 min each, and then dipped in diluted HCl for 10 min to remove the native oxide, followed by sulfur passivation by dipping in 8% $(NH_4)_2S$ for 40 min at room temperature. After being dried by N_2, the wafers were divided into three groups. Group 1 (denoted as Pre-F) was first treated by fluorine plasma at a flow rate of $CHF_3/O_2 = 10/1$ (sccm) for 3 min. Subsequently, TaHfON dielectric was deposited on the surface of all three groups by cosputtering of Ta (DC) and Hf (RF) targets at room temperature. Then, group 2 (denoted as Post-F) received a fluorine-plasma treatment under the same conditions as group 1. Group 3 without fluorine treatment (denoted as W/O) was

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used as the control sample. Postdeposition annealing (PDA) was carried out at 600 °C for 60 s in NH_3 to increase the nitrogen content in TaHfON (500 sccm). Al electrode was evaporated and patterned with an area of 7.85×10^{-5} cm^2, followed by another Al evaporation on the backside of the wafers. Finally, a forming-gas (95% $N_2 + 5\%$ H_2) annealing was performed at 300 °C for 20 min.

III. RESULTS AND DISCUSSION

High-frequency (1-MHz) capacitance–voltage (C-V) characteristics of the samples are measured by HP 4284A precision LCR meter, and the typical C-V curves swept in both directions (from inversion to accumulation and then backward) are shown in Fig. 1. When comparing with the control sample without fluorine treatment (W/O), a slight reduction of accumulation capacitance (C_{ox}) is found in the sample with fluorine treatment after the deposition of the dielectric (Post-F) and should be caused by the high bonding energy between metal atom and incorporated F atom.[17] However, the C-V curve of the Post-F sample shows a smaller shift (to the positive direction) and a smaller hysteresis, implying reduced defects near/at the high-k/GaAs interface caused by fluorine passivation, and thus the carrier mobility of the Post-F sample could be increased (due to less defect-related carrier scattering), outweighing the slight loss in k value. As for the sample with predeposition fluorine treatment (Pre-F), the large degradation in C_{ox} compared to the W/O sample should mainly result from the formation of a low-k GaO/AsO layer at the GaAs surface during the fluorine treatment in an ambient containing oxygen. Moreover, the Pre-F sample gives poorer characteristics (e.g., larger shift of C-V curve to the positive direction, less steep slope in the depletion-to-accumulation transition region, and worse saturation behavior) than the Post-F sample, which should be due to the traps associated with the unstable Ga/As oxides.[18]

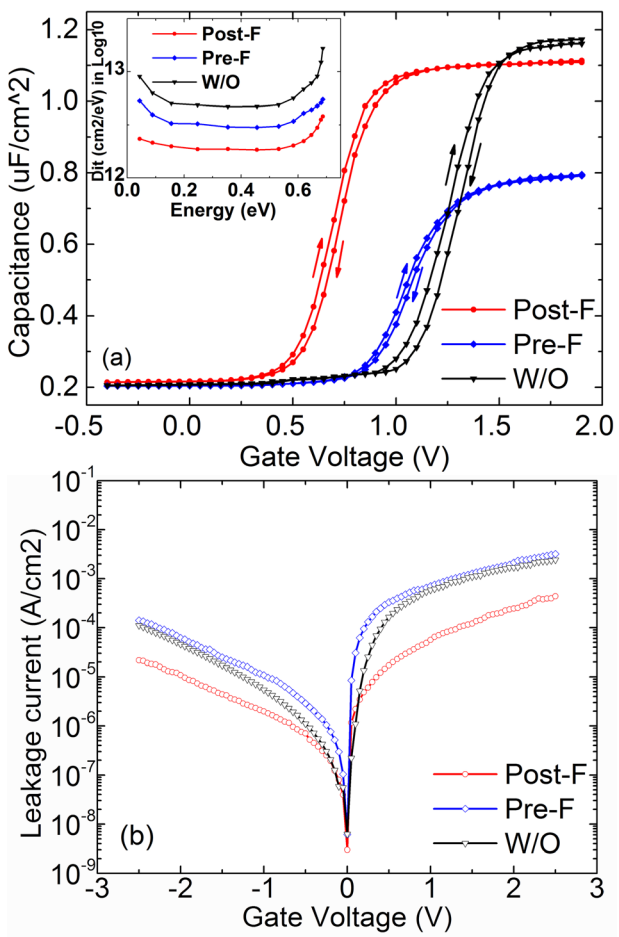

FIG. 1. (Color online) (a) High-frequency C-V curve with interface-state density (D_{it}) in the bandgap (inset) and (b) leakage current characteristics of the three samples.

Device parameters extracted from the HF C-V curves are listed in Table I. The equivalent k value of the gate dielectric can be calculated as

$$k_{eq} = k_{SiO_2} T_{ox}/\mathrm{CET}, \tag{1}$$

$$\mathrm{CET} = k_0 k_{SiO_2}/C_{ox}, \tag{2}$$

where CET is capacitance equivalent thickness; k_0 is the vacuum permittivity; k_{SiO_2} is the dielectric constant of SiO_2; and T_{ox} is thickness of the dielectric layer measured by ellipsometry. The flatband voltage (V_{fb}) determined from flatband capacitance is found to be positive for all the samples, implying the existence of negative charges in the dielectric layer, which means that more negatively charged traps should exist in the oxide layer and near the high-k/GaAs interface than oxygen vacancies (tend to be positively charged in Hf-based high-k materials[19]), consistent with the results in Ref. 14. An obvious decrease of V_{fb} is found after F incorporation in the dielectric, indicating a reduction of negative charges due to the bonding of F atoms to the Hf dangling bonds. With almost the same T_{ox}, the Post-F sample has an even smaller V_{fb} (0.7 V) than the Pre-F sample, implying that the fluorine-plasma treatment after deposition of the gate dielectric can effectively reduce the oxide traps and interface states.[20,21] This can be further supported by the smallest equivalent oxide-charge density (Q_{ox}) of the Post-F sample ($-3.52 \times 10^{12}\,cm^{-2}$), calculated by

$$Q_{ox} = -C_{ox}(V_{fb} - \Phi_{ms})/q, \tag{3}$$

where Φ_{ms} is the work function difference between the Al electrode and GaAs substrate. These can be explained by the capability of fluorine to passivate the oxide traps inherent in the high-k bulk and also the dangling bonds at the high-k/GaAs interface.

TABLE I. Electrical and physical parameters of the samples extracted from HF C-V curves.

Sample	Post-F	Pre-F	W/O
T_{ox} (nm)	13.1	13.5	13.2
V_{fb} (V)	0.7	1.08	1.25
Q_{ox} (cm^{-2})	-3.5×10^{12}	-4.3×10^{12}	-7.8×10^{12}
Hysteresis (mV)	45	33	57
CET (nm)	3.08	4.37	2.91
k	16.7	12.1	17.7

The distribution of interface-state density (D_{it}) in the energy bandgap of the samples is extracted from their HF C-V curves by the Terman's method[22] for the purpose of comparison. With comparable CET for the Post-F and W/O samples (3.08 vs 2.91 nm), the smaller D_{it} of the former ($\sim 2 \times 10^{12}\,cm^{-2}eV^{-1}$) than that of the latter [see the inset of Fig. 1(a)] demonstrates that the quality of the high-k/GaAs interface could be improved to some extent by the F-plasma treatment.

In Fig. 1(b), the smallest leakage current density (e.g., 5.62×10^{-5}A/cm^2 at gate voltage of 1 V) is obtained for the post-F sample. This could be attributed to the reduced trap-assisted tunneling due to its smallest Q_{ox} and D_{it}, as mentioned above. The Pre-F sample shows the largest leakage current (7.04×10^{-4}A/cm^2 at gate voltage of 1 V) probably because the predeposition F treatment induces radiation-related damage to the GaAs surface and also results in excess F interstitials at the interface in the form of gap states.[17,23]

In order to clarify the effects of the fluorine treatment, the chemical states in the dielectric layer and at/near the high-k/GaAs interface after the whole fabrication process are analyzed by XPS. Figure 2 shows the XPS spectrum for Ta 4f. Compared to the control sample, the Ta 4f 7/2 and 5/2 peaks of the Post-F and Pre-F samples shift to higher energies of 0.65 and 0.15 eV, respectively, which should be due to the higher electronegativity of F (4.0) than that of O (3.5). Furthermore, an obvious peak is found at 28 eV for the Post-F sample, corresponding to Ta-F bond according to the National Institute of Standards and Technology database. However, no Ta-F peak is detected for the Pre-F sample, explaining why the shift of the two peaks is much smaller than that of the Post-F sample. This difference in fluorine incorporation between the two samples can be seen more clearly from the F 1s spectrum in Fig. 3(a), which supports that fluorine incorporation in the high-k dielectric is effective only for the plasma treatment after the deposition of the high-k dielectric,

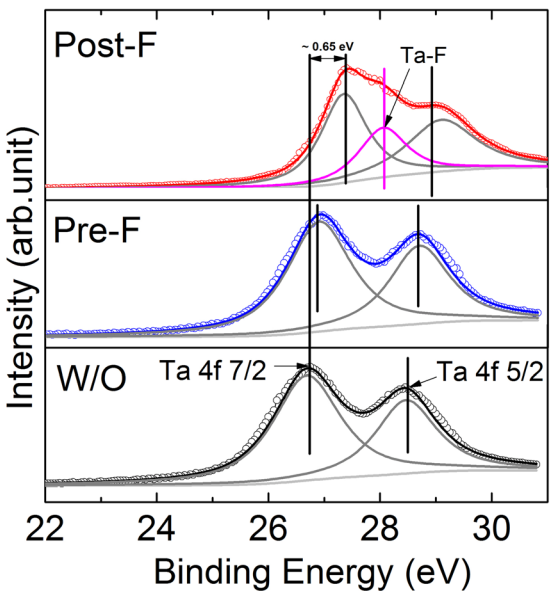

FIG. 2. (Color online) Ta 4f XPS spectrum of the Post-F, Pre-F, and W/O samples.

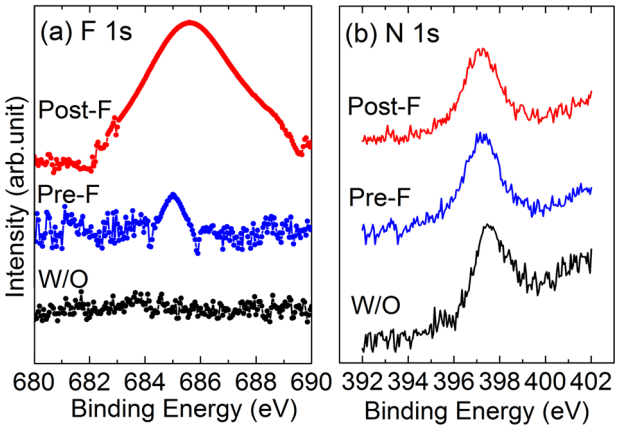

FIG. 3. (Color online) (a) F 1s and (b) N 1s XPS spectra of the Post-F, Pre-F, and W/O samples.

basically consistent with the result in Ref. 23. The not-so clear F 1s peak of the Pre-F sample indicates less F incorporated at/near the high-k/GaAs interface and thus less passivation of dangling bonds there, leading to larger D_{it} than that of the Post-F sample as supported by the data in Table I.

In the N 1s spectrum of the three samples shown in Fig. 3(b), obvious peaks can be observed and the nitrogen percentage of the Post-F, Pre-F, and W/O samples can be extracted to be 8.03%, 7.66%, and 8.00%, respectively. The O 1s XPS spectrum of the samples after different etching times is shown in Fig. 4. In the dielectric layer, the O 1s spectra of the three samples are almost the same initially. But after etching for 540 s, the intensity of the Post-F sample decreases significantly while that of the W/O sample starts

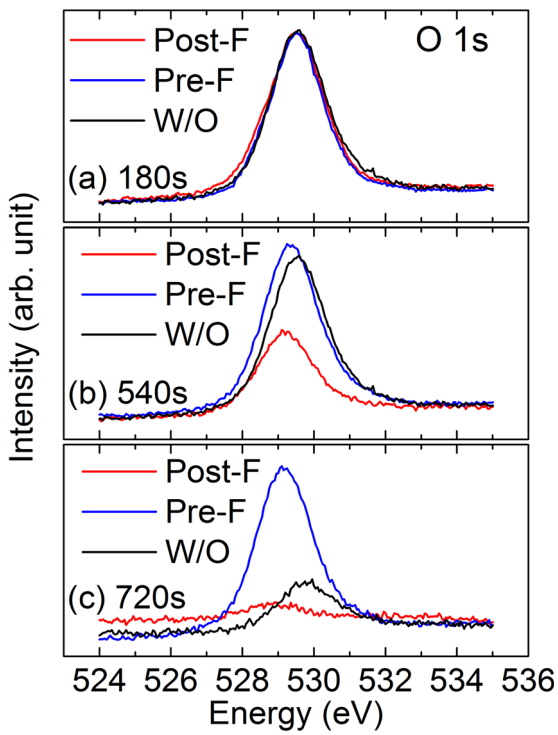

FIG. 4. (Color online) O 1s XPS spectrum of the Post-F, Pre-F, and W/O samples after etching for 180, 540, and 720 s.

to decrease. When the etching process lasts for 720 s and almost reaches the high-k/GaAs interface, the O 1s peak of the Post-F sample nearly disappears while the intensity of the Pre-F sample is still high, indicating that the Post-F sample has the smallest interlayer thickness and the Pre-F sample has the largest. This further proves that postdeposition fluorine incorporation is capable of suppressing the formation of the native oxides (GaO/AsO). Although the Pre-F sample also has some fluorine incorporation, it has the largest interlayer thickness due to the oxygen-containing ambient during the fluorine treatment before the high-k deposition.

Figures 5 and 6 compare the As 3d and Ga 3d XPS spectra of the three samples. As–O bond can be detected in Figs. 5(b) and 5(c) at 44–45 eV, but not in Fig. 5(a). Besides, the intensity of As–As bond in Fig. 5(a) is lower than that in Figs. 5(b) and 5(c). These results indicate that the fluorine treatment can effectively reduce the weak As–O and As–As bonds. The higher As-O intensity for the Pre-F sample than the W/O sample should be due to the growth of native oxide on the GaAs substrate in the oxygen-containing ambient during the fluorine treatment. On the other hand, the peaks of Ga–As, Ga–S, and Ga–O bonds in Fig. 6 are located at 19.5, 20.2, and 20.8 eV, respectively, and Hf-O doublet appears at 18.9 and 17.0 eV. Much weaker Ga-O peak in Fig. 6(a) than in Figs. 6(b) and 6(c) further shows that the growth of the low-k interfacial Ga oxide can be effectively suppressed by fluorine incorporation after the high-k deposition. Moreover, the Hf-O doublet of the Post-F sample is weaker than those of the Pre-F and W/O samples, implying that the fluorine treatment can also block the diffusion of elements (Hf, O) in the dielectric layer toward the substrate surface. Similar to the As-O peak in Fig. 5, the Ga-O peak of the Pre-F sample is stronger than that of the W/O sample, based on the same reason as above, which could explain why the Pre-F sample has the smallest C_{ox} and thus the lowest k value. Also, the large gate leakage current of the Pre-F sample in Fig. 1(b) could be attributed to the high concentrations of As–O and Ga–O bonds at/near the high-k/GaAs interface because the gate leakage current is likely caused by interfacial GaO/AsO-induced lowering of the TaHfON/GaAs conduction-band offset and also trap-assisted tunneling of charge carriers.[24,25]

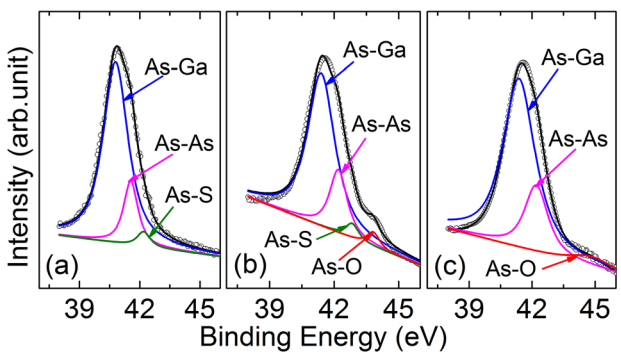

FIG. 5. (Color online) As 3d XPS spectrum of (a) Post-F, (b) Pre-F, and (c) W/O samples near the high-k/GaAs interface.

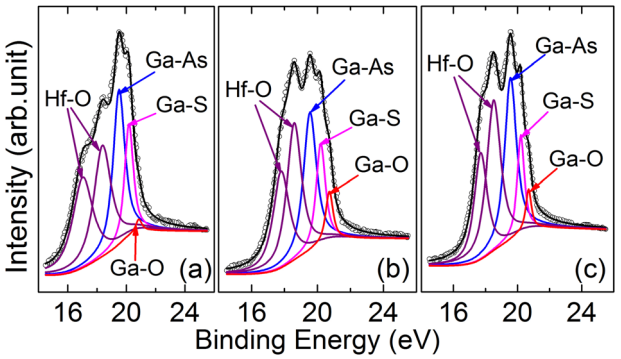

FIG. 6. (Color online) Ga 3d XPS spectrum of (a) Post-F, (b) Pre-F, and (c) W/O near the high-k/GaAs interface.

Both As–S and Ga–S bonds are detected in Figs. 5 and 6, implying that during the sulfur passivation, reactions $(NH_4)_2S + H_2O \rightarrow 2NH_4^+ + S^{2-} + H^+ + OH^-$ and $2GaAs + 12H^+ + 6S^{2-} \rightarrow Ga_2S_3 + As_2S_3 + 6H_2$ happen with Ga_2S_3 and As_2S_3 formed at the GaAs surface, thus decreasing the Ga/As-related vacancies.[26] On the other hand, the concentrations of As–O and As–S bonds in Fig. 5 are obviously much lower than those of Ga-O and Ga-S in Fig. 6 near/at the high-k/GaAs interface, and especially for the W/O sample in Fig. 5(c), no As-S peak exists. The possible reaction of $As_2O_3 + 2GaAs \rightarrow Ga_2O_3 + 4As$ during the PDA leads to the conversion of As oxide to Ga oxide,[27] and similarly many As–S bonds have been probably transformed to stronger Ga–S bonds during the PDA.[28] Compared with Fig. 6(a), Fig. 6(b) has less Ga–S bonds, supporting that more Ga–S bonds are replaced by stronger Ga–F bonds during the fluorine treatment directly on the GaAs surface. This indicates that postdeposition fluorine treatment is capable of maintaining the sulfuration of the GaAs substrate and thus is a very promising method for further passivating the GaAs surface.

IV. CONCLUSIONS

GaAs MOS capacitors with fluorine-plasma treatment before or after the deposition of HfTaON gate dielectric are fabricated and their electrical properties are compared with those of a control sample without the treatment. Measured results show that the fluorine-plasma treatment can result in lower interface-state and oxide-charge densities, which are beneficial to the enhancements of carrier mobility and thus drive current for high-speed applications. The involved mechanisms are analyzed by XPS, which shows that fluorine incorporation in the dielectric can effectively suppress the growth of unstable native oxides at the GaAs surface and also prevent the diffusion of elements in the high-k dielectric toward the GaAs surface. This greatly reduces the relevant defects and improves the interface quality, thus unpinning the Femi level at the interface and giving good electrical properties to the MOS device. Finally, as compared with the predeposition fluorine treatment, the postdeposition treatment can incorporate more fluorine in the dielectric, and thus can produce better electrical properties for the device.

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[1]"International Technology Roadmap for Semiconductors (ITRS), 2013," http://www.itrs.net.
[2]J. J. Gu, O. Koybasi, Y. Q. Wu, and P. D. Ye, Appl. Phys. Lett. **99**, 112113 (2011).
[3]P. Kordos, R. Kudela, R. Stoklas, K. Cico, M. Mikulics, D. Gregusova, and J. Novak, Appl. Phys. Lett. **100**, 142113 (2012).
[4]Y. C. Chang *et al.*, Appl. Phys. Lett. **97**, 112901 (2010).
[5]P. S. Das and A. Biswas, Microelectron. Rel. **52**, 112 (2012).
[6]X. Yu, C. Zhu, and M. F. Li, Appl. Phys. Lett. **85**, 2893 (2004).
[7]X. Lu, K. Maruyama, and H. Ishiwara, J. Appl. Phys. **103**, 044105 (2008).
[8]L. M. Lin and P. T. Lai, J. Mater. Sci. Mater. Electron. **19**, 894 (2008).
[9]M. S. Akbar, H. J. Cho, R. Choi, C. S. Kang, C. Y. Kang, C. H. Choi, S. J. Rhee, Y. H. Kim, and J. C. Lee, IEEE Electron Device Lett. **25**, 465 (2004).
[10]S. Kundu, S. Roy, P. Banerji, S. Chakraborty, and T. Shripathi, J. Vac. Sci. Technol. B **29**, 031203 (2011).
[11]I. Ok *et al.*, IEEE Electron Device Lett. **27**, 145 (2006).
[12]H. Kim *et al.*, Appl. Phys. Lett. **92**, 102904 (2008).
[13]S. Kundu, T. Shripathi, and P. Banerji, Solid State Commun. **151**, 1881 (2011).
[14]L. S. Wang, L. Liu, J. P. Xu, S. Y. Zhu, Y. Huang, and P. T. Lai, IEEE Trans. Electron Devices **61**, 742 (2014).
[15]L. S. Wang, J. P. Xu, S. Y. Zhu, Y. Huang, and P. T. Lai, Appl. Phys. Lett. **103**, 092901 (2013).
[16]K. Tse and J. Robertson, Appl. Phys. Lett. **89**, 142914 (2006).
[17]J. Ha, K. Seo, and P. C. Mclntyre, Appl. Phys. Lett. **90**, 112911 (2007).
[18]M. M. Grank, G. D. Wilk, D. Starodub, T. Gustafsson, E. Garfunkel, Y. J. Chabal, J. Grazul, and D. A. Muller, Appl. Phys. Lett. **86**, 152904 (2005).
[19]H. H. Tseng *et al.*, IEEE Trans. Electron Devices **54**, 3267 (2007).
[20]C. X. Li, C. H. Leung, P. T. Lai, and J. P. Xu, Solid-State Electron. **54**, 675 (2010).
[21]Q. B. Tao and P. T. Lai, Phys. Status Solidi RRL **7**, 434 (2013).
[22]L. M. Term, Solid-State Electron. **5**, 285 (1962).
[23]W. J. Maeng, J. Y. Son, and H. Kim, J. Electrochem. Soc. **156**, G33 (2009).
[24]V. V. Afanas'ev and A. Stesmans, Appl. Phys. Lett. **84**, 2319 (2004).
[25]F. Gao, S. J. Lee, D. Z. Chi, S. Balakumar, and D. L. Kwong, Appl. Phys. Lett. **90**, 252904 (2007).
[26]M. K. Lee and C. F. Yen, Appl. Phys. A **116**, 2051 (2014).
[27]H. L. Lu, L. Sun, S. J. Ding, M. Xu, W. Zhang, and L. K. Wang, Appl. Phys. Lett. **89**, 152910 (2006).
[28]Y. W. Medvedev, Appl. Phys. Lett. **64**, 3458 (1994).