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Device performance simulations of multilayer black phosphorus tunneling transistors

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We report a theoretical investigation of ballistic transport in multilayer black phosphorus (BP) tunneling transistors (TFETs) with HfO_2 as the gate oxide. First-principles calculations show that monolayer BP can be preserved well on HfO_2 (111) surface. For a better device performance, the optimum layer and transport direction at different channel lengths are investigated. It is shown that BP TFETs have larger drain current in the armchair direction (AD) than in the zigzag direction, and the current difference can be several orders of magnitude. On-state current can be enhanced in the BP TFETs using thicker BP film, while the minimal leakage current is increased at the same time. To reduce the leakage current and subthreshold swing in the multilayer BP TFETs, lower source/drain doping concentration and smaller drain voltage should be applied. Compared to monolayer MoS_2, $MoSe_2$, and $MoTe_2$ TFETs monolayer BP TFETs in AD can reach larger on-state current at the same I_{on}/I_{off} ratio. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4935752]

Recently, layered black phosphorus (BP) has received much attention due to its potential applications in electronic, optical, and thermal devices.[1–5] In bulk BP, individual atomic layers are stacked together by van der Waals (vdW) interaction and monolayer BP can be mechanically exfoliated from the bulk BP. Thin film BP field effect transistors (FETs) have shown[1] excellent electrical properties with an on-off current ratio as large as 10^5 and a high mobility of $1000\,cm^2\,V^{-1}\,s^{-1}$. Even with the electron-hole scattering and extrinsic impurity scattering, carrier mobilities extracted from BP FETs are higher than those of transition metal dichalcogenides (TMDCs).[1–4,6] Theoretical investigations also suggested that BP FETs may have a promising ballistic device performance compared with the 2D TMDC devices.[7–9]

To reduce power dissipation in MOSFET, tunneling FET was proposed and various materials are applied.[10,11] Compared with traditional bulk semiconductor tunneling transistors (TFETs), using 2D materials can result in better gate control and smaller leakage current due to the atom thin structure.[12–17] The low on-current is a major issue of all the TFETs, but using 2D material may achieve higher on-state current due to the larger electric field at the tunneling junction.[15–17] Furthermore, since there is no surface dangling bonds in 2D materials, a sharper subthreshold swing (SS) and smaller device dimension may be achieved by 2D TFETs.[18] In comparison to other 2D materials such as the popular TMDCs, BP has a tunable direct band gap from 0.3 eV to 2.0 eV as well as an anisotropic band structure,[19–21] suggesting that a higher on-state current can be expected in BP TFETs than using many other 2D materials.

It has been shown that monolayer BP TFETs can reach SS below 60 mV/decade and a wide range of on-state current.[22] However, the on-current of monolayer BP TFETs is limited by the large band gap. For smaller band gaps, multilayer BP TFETs are expected to achieve a higher on-current. In particular, the layer dependent gate control and the scaling limit of multilayer BP TFETs are still unknown. It is the purpose of this work to investigate the device physics of multilayer BP TFETs towards proper device performance engineering and optimization. Using an atomistic approach based on the nonequilibrium Green's function formalism (NEGF),[23] ballistic device characteristics of multilayer BP TFETs are investigated. We developed a strategy for determining the suitable layer thickness and transport direction in order to achieve very reasonable on/off currents at different channel lengths. We also compared the device performance of BP TFETs with TMDC TFETs and studied the interface between monolayer BP and HfO_2 by first-principles calculations.

We consider the BP TFET schematically shown in Fig. 1(a). The device has double gates with HfO_2 material as the gate insulator whose dielectric constant is 25. The source and drain is p-type and n-type doped with the same doping density $n_0 = 7.0 \times 10^{13}\,cm^{-2}$, respectively. The channel of the TFET is intrinsic with the same length as the gate. Fig. 1(b) shows the atomic structure of bilayer BP. A 4-band tight-binding (TB) Hamiltonian is used to describe multilayer BP materials.[24] For 2L, 3L, and 4L BPs, the nearest interlayer coupling parameter is determined by fitting to the GW band structure:[24] $t_1^{\perp} = 0.355\,eV$, 0.398 eV, and 0.427 eV for 2L, 3L, and 4L, respectively. In our analysis, we solve the Schrödinger equation and Poisson equation self-consistently within NEGF to obtain the potential profile in the channel.[8,23]

For practical device applications, instability and surface degradation of the BP film are inevitable. Recently, techniques of encapsulation by AlO_x layers[25–27] or copolymer capping layers,[28] as well as using solvent exfoliations[29–32] were applied to maintain excellent performance of the BP devices. Reaction between BP and the substrate can also be avoided by covering graphene or h-BN on BP.[33,34] First principles calculations showed that there is perfect monolayer BP crystal on the H-passivated Al_2O_3.[35] We also carried out first

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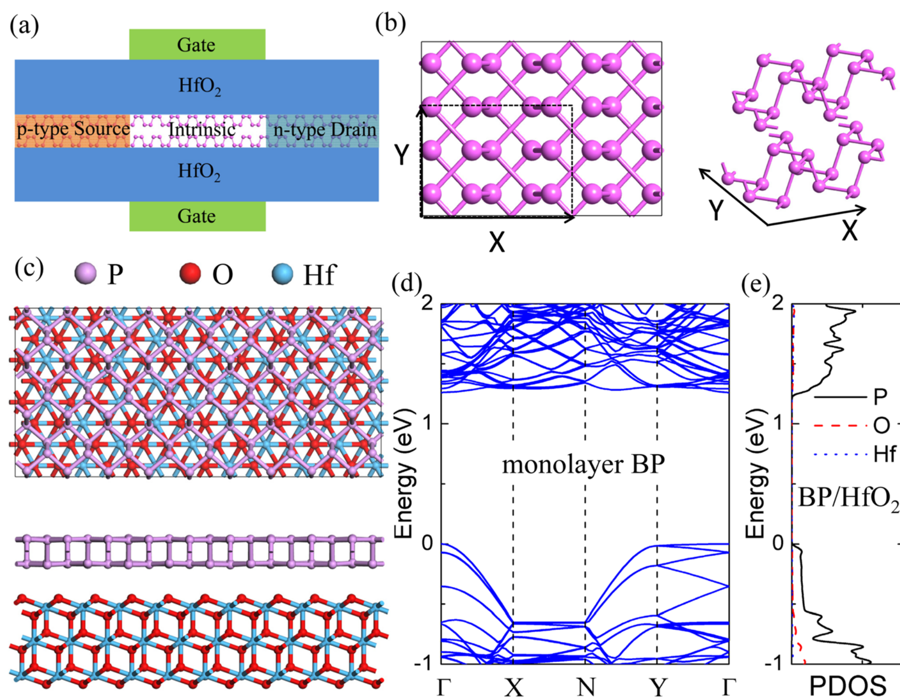

FIG. 1. (a) Device structure of the double gate multilayer BP TFET. The TFET has a p-type source, an intrinsic channel, and a n-type drain–all of them are layered BPs. (b) Top view and side view of the atomic structure of a bilayer BP. (c) Top view and side view of the optimized atomic structure of monolayer BP on HfO_2 (111) surface. (d) The band structure of the isolated monolayer BP and (e) the projected density of states (PDOS) of the BP/HfO_2 hybrid structure.

principles calculations which show that the monolayer BP crystal can be kept well on the HfO_2 (111) surface. Here, the HfO_2 is the cubic crystalline phase which is one of the stable phases of HfO_2. Considering lattice matching in the DFT calculation, the (111) surface of HfO_2 is chosen. The surface is insulating without interfacial gap states and is also energetically favored.[36] Fig. 1(c) plots the relaxed atomic structure of monolayer BP and HfO_2 interface, obtained by density functional theory (DFT) total energy calculations using the Vienna *Ab-initio* Simulation Package (VASP).[37] The exchange-correlation is treated by the generalized gradient approximation (GGA) with the Perdew-Burke-Ernzerhof (PBE) functional,[38,39] and the PBE-optB88 functional[40,41] is applied to handle the vdW interactions between the monolayer BP and HfO_2. Different from O-terminated BP/Al_2O_3 interface where BP becomes oxidized,[35] here the monolayer BP is maintained and has vdW interaction with the HfO_2 (111) surface having a distance 2.9 Å between the two materials. Due to lattice mismatch, there is a 5% in-plane stretching of monolayer BP leading to a change of band gap from 1.1 eV to 1.2 eV (DFT calculation with PBE functional). From the band structure of the isolated monolayer BP in Fig. 1(d) and the projected density of states (PDOS) of the BP/HfO_2 hybrid structure shown in Fig. 1(e), the electric property of BP is well preserved when grown on the HfO_2 (111) surface. The estimated conduction and valence band offsets from the DFT calculation are found to be about 1.2 eV and 1.8 eV, respectively.

We first compare I_D vs V_G of double gate (DG) and single gate (SG, without the bottom gate) 1L AD BP TFETs. These devices have 10 nm gate length and 3 nm gate oxide thickness at $V_D = 0.5$ V. As shown in Fig. 2(a), DG BP TFETs apparently have better device performance and can reach lower minimal leakage current and higher on-state current. Especially, the on-state current at $V_G = 0.75$ V is increased by 82 times in DG BP TFETs. As a result, the subthreshold swing is reduced from 246.6 mV/decade in SG BP TFETs to 119.0 mV/decade in DG BP TFETs. In the following calculations, we focus on studying the device characteristics of DG BP TFETs, and TFETs are DG without specification.

Fig. 2(a) also plots I_D vs V_G for multilayer BP TFETs with $L_G = 10$ nm and $t_{ox} = 3$ nm at $V_D = 0.5$ V. When the number of BP layers increases from mono-layer (1L) to 4-layer (4L), I_D increases by several orders of magnitude as shown in Fig. 2(a). This drastic increase of I_D is mainly due to the change of band gap when BP thickness is increased: band structures obtained by the GW approximation showed band gap to decrease with the number of layers[24] as listed in

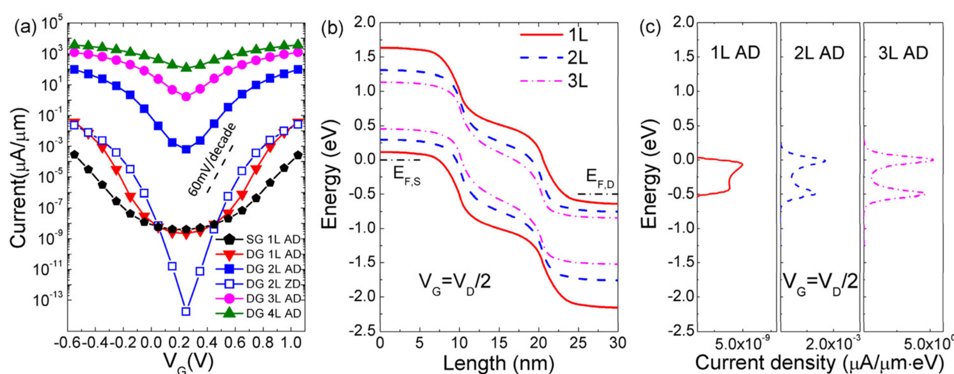

FIG. 2. (a) I_D vs V_G for multilayer BP TFETs having 10 nm gate length at $V_D = 0.5$ V. (b) Potential profiles and (c) current densities of 1L, 2L, and 3L BP TFETs at $V_G = V_D/2$.

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TABLE I. Band gap E_g and electron/hole effective mass $m_{e/h}$ obtained by the TB model of this work.

	E_g (eV)	$m_{e,AD}$	$m_{h,AD}$	$m_{e,ZD}$	$m_{h,ZD}$
1L BP	1.52	0.16	0.18	0.87	1.17
2L BP	1.01	0.14	0.16	1.19	0.75
3L BP	0.68	0.12	0.12	1.37	0.64
4L BP	0.46	0.09	0.09	1.47	0.59

Table I. If the off-state of the TFET is set at $V_G^{off} = V_D/2$ and the on-state at $V_G^{on} = V_G^{off} + V_D$, the on-state current of 1L, 2L, 3L, and 4L n-type BP TFETs in the armchair direction (AD) is 3.5×10^{-5}, 9.6×10^1, 3.6×10^2, and $1.7 \times 10^3\ \mu A/\mu m$, respectively. 1L BP has a band gap of 1.52 eV, and the band-to-band tunneling is therefore substantially suppressed by the large gap. Even though it is easy to get larger current in thicker BP films, it is difficult to obtain a suitable on-off current ratio which decreases from 1.6×10^4 to 1.5×10^1 when the layer number is changed from 1L to 4L for n-type BP TFETs in AD. From the extracted carrier effective masses in Table I, we can see that layered BP has lighter carrier effective mass in AD. Due to the anisotropic band structure of BP material, device performance of all BP TFETs greatly depends on the transport direction: they have larger current in AD than that in zigzag direction (ZD), e.g., in 2L BP TFETs in Fig. 2(a). For the system parameters, we investigated, the current of 1L ZD TFETs is always smaller than $10^{-11} \mu A/\mu m$(not shown). Nevertheless, the BP TFETs in ZD have higher on-off current ratio due to larger carrier effective masses.[10] In 10 nm 2L BP TFETs, the I_{on}/I_{off} ratio is 2.0×10^{10} in ZD with SS $= 48.5$ mV/decade but only 1.6×10^4 in AD.

Figs. 2(b) and 2(c) compare the band edge profiles along the channel and corresponding energy resolved current densities of AD BP TFETs with different layers at $V_G = V_D/2$. Fig. 2(b) demonstrates that with the increasing of the BP layer thickness the tunneling barrier from source to drain gets thinner. Therefore, the leakage current at off-state increases dramatically with the BP layer thickness as shown in Fig. 2(c). Simulated devices in Fig. 2(b) have 10 nm channels under the gate which are smaller than overlaps between the source-channel junctions and the channel-drain junctions. Consequently, the potential profiles under the gate of these BP TFETs are not flat, which is a typical short channel effect in TFETs.[42] For 1L BP TFETs, the band gap of 1.52 eV can cover the energy region between source valance band maximum (VBM) and drain conduction band minimum (CBM), so there is only direct tunneling current from source VB to drain CB (DTSD) and the leakage current is suppressed. However, the energy gaps of 2L, 3L, and 4L are smaller than the energy regions between source VBM and drain CBM corresponding BP TFETs. As a result, there is not only DTSD current but also band to band tunneling current (BTBT) from source VB to channel CB in 2L, 3L, and 4L BP TFETs. The DTSD current can be suppressed in longer channel TFETs, while BTBT current cannot be effectively decreased by extending the channel length as shown below.

Next, we have determined the scaling behavior of multilayer BP TFETs. Fig. 3(a) shows the off-state current of multilayer BP TFETs as a function of the gate length L_G, obtained at $V_G = V_D/2$ and $V_D = 0.5$V. The HfO_2 oxide thickness is fixed to be 3 nm. It can be seen that when BP layer thickness is increased to 4 layers the leakage current can be larger than $10^{-2}\ \mu A/\mu m$, even though L_G is extended to 25 nm. The off-state current of 1L BP TFETs in ZD is smaller than $10^{-20} \mu A/\mu m$ (not shown). In 1L AD BP TFETs the off-state current decreases exponentially with the gate length. While for other layered BP TFETs, I_{off} gets decreasing slowly when L_G reaches 20 nm, especially in ZD. The reason is that the band gaps of these layered BP cannot cover the energy region between source VBM and drain CBM. With the increasing channel length the DTSD current can be effectively reduced, while BTBT current cannot be decreased as shown in Fig. 3(d). Fig. 3(b) compares I_{on}/I_{off} ratio as a function of channel length, where I_{off} and I_{on} are obtained at $V_G^{off} = V_D/2$ and $V_G^{on} = V_G^{off} + V_D$, respectively. I_{on}/I_{off} ratio of 1L ZD BP TFETs is not shown for the extremely small I_{on}. With the reduced leakage current, the I_{on}/I_{off} ratio can get larger than 10^{18} and SS can be 27.7 mV/decade in 25 nm 1L AD BP TFETs. It can also be observed that only 1L AD, 2L AD, and ZD BP TFETs can achieve SS below 60 mV/decade.

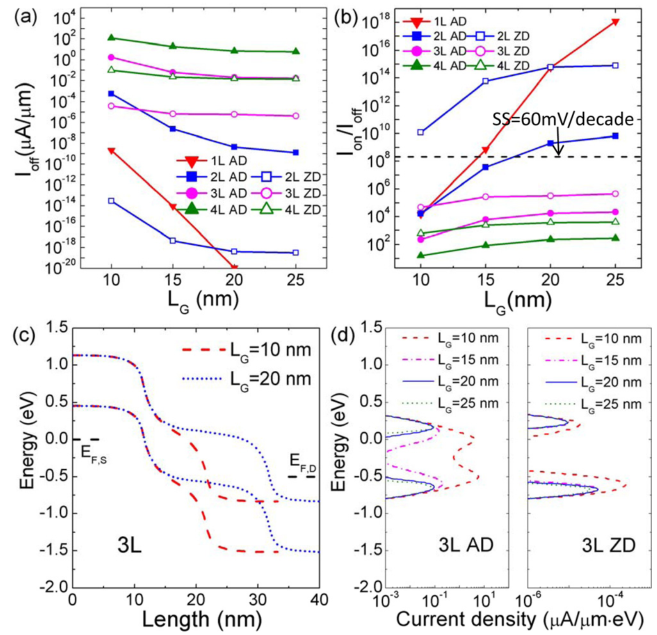

FIG. 3. (a) I_{off} and (b) I_{on}/I_{off} ratio as a function of the gate length for multilayer BP TFETs at $V_D = 0.5$ V. The I_{on}/I_{off} ratio of 2.15×10^8 for SS of 60 mV/decade is obtained by the relation: $\log10(I_{on}/I_{off}) = (V_G^{on} - V_G^{off})$/SS. (c) Potential profiles and (d) current densities for 3L BP TFETs with different gate length(L_G) at $V_G = V_D/2$.

Figs. 3(c) and 3(d) show the band edge profiles along the channel and corresponding energy resolved current densities of 3L BP TFETs with different channel lengths. Compared with 10 nm TFETs, the potential under the gate in 20 nm 3L BP TFETs gets flatter, which means a better gate control. At the same time, DTSD current is effectively suppressed and the leakage current is mainly BTBT current in 20 nm 3L AD BP TFETs as shown in Fig. 3(d). The components of leakage current actually depend on the transport direction. Due to the heavier effective masses in ZD, the current is mainly BTBT current even in 10 nm 3L ZD BP

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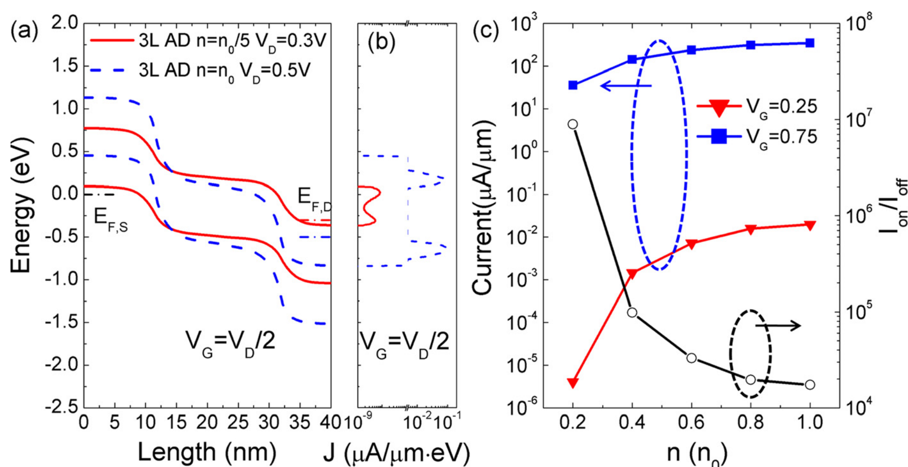

FIG. 4. (a) Potential profiles and (b) current densities for 20 nm 3L BP TFETs at different source/drain doping concentrations and drain voltages. (c) I_{on}, I_{off}, and I_{on}/I_{off} ratio as a function of the doping density in 20 nm 3L AD BP TFETs with $V_D = 0.5$ V.

TFETs as shown in Fig. 3(d), and the BTBT current in ZD nearly does not change when L_G gets larger than 15 nm. Leakage current can be effectively suppressed and smaller SS can be achieved in long channel 1L BP TFETs. However, increasing the channel length is not enough to decrease the BTBT leakage current in 3L BP TFETs as demonstrated in Fig. 3(a). In order to suppress the BTBT leakage current, it is necessary to reduce the energy window between source VBM and drain CBM.

To reduce the leakage current and suppress the short channel effects of BP TFETs with small band gap, we applied lower source/drain doping concentration and smaller drain voltage. As demonstrated in Fig. 4(a), the gate control is deteriorated by the overlap between source-channel junction and channel-drain junction in 20 nm 3L BP TFETs with source/drain doping density $n = n_0$ and $V_D = 0.5$V. With the reduced doping density and drain voltage, the gate control is improved and the potential under the gate gets flatter at $n = n_0/5$ and $V_D = 0.3$ V. At the same time, VBM/CBM edge moves to source/drain fermi level and the tunneling energy window between source VBM and drain CBM gets narrower. Then, the band gap of 3L BP can cover the energy region between the source VBM and drain CBM and there is no BTBT current. The leakage current is effectively suppressed by lower doping concentration and smaller V_D as shown in Fig. 4(b). Fig. 4(c) shows I_{on}, I_{off}, and I_{on}/I_{off} ratio as a function of doping density in 3L AD BP TFETs with $V_D = 0.5$ V and $L_G = 20$ nm. Both I_{on} and I_{off} become smaller as the source/drain doping density is decreased from n_0 to $n_0/5$. I_{off} is decreased significantly from 2.0×10^{-2} to 4.0×10^{-6} $\mu A/\mu m$ while I_{on} is reduced less than one order from 3.4×10^2 to $3.6 \times 10^1 \mu A/\mu m$. Hence, the I_{on}/I_{off} ratio is increased from 1.7×10^4 to 8.9×10^6. Therefore, lighter source/drain doping concentration and smaller drain voltage should be applied in multilayer BP TFETs to reduce the leakage current and achieve higher I_{on}/I_{off} ratio.

The extracted I_{on} as a function of I_{on}/I_{off} ratio for n-type layered BP TFETs is shown in Fig. 5 at $V_D = 0.5$ V, which is obtained by charting along the I_D–V_G curve with the fixed gate voltage window ($V_G^{on} - V_G^{off} = V_D$).[43,44] All TFETs have the same device structure (10 nm gate length and 3 nm HfO_2), drain voltage and doping density (the same dopant number per atom). From the figure optimal transport direction and thickness of BP film can be determined. For example, for a four order I_{on}/I_{off} ratio the largest on-state current can be obtained in 3L BP TFETs in ZD. It is found that the I_{on}/I_{off} ratio utmost limits decreases with the BP thickness. Even though 1L ZD BP TFETs can reach the highest I_{on}/I_{off} ratio, I_{on} is smaller than 10^{-8} $\mu A/\mu m$. In comparison, 2L ZD BP TFETs can achieve the reasonable I_{on}/I_{off} ratio limit with larger I_{on}. In Fig. 5, we also compare device performance of 10 nm BP TFETs with three typical TMDC TFETs: MoS_2, $MoSe_2$, and $MoTe_2$ whose band gaps are 1.66 eV, 1.43 eV, and 1.07 eV, respectively. Here, we just compared BP TFETs with 1L TMDC TFET because TMDC materials (e.g., MoS_2, etc.) undergo a band gap transition from direct (for 1L) to indirect (for 2L TMDC and more layers).[45] The Hamiltonians of these TMDC materials are described by three band tight binding model.[8,46] We found that the I_{on} of 1L AD BP TFETs is larger than 1L MoS_2 TFETs by 4 orders of magnitude at the same I_{on}/I_{off} ratio $< 10^6$: this large difference is interesting since the materials have comparable band gaps. Importantly, even compared to TFETs made of $MoTe_2$ which has a smaller band gap of 1.07 eV, 1L AD BP TFETs can reach a larger I_{on}. By using 2L ZD BP, better device performance can be obtained at high I_{on}/I_{off} ratio which can be as large as 10^9.

In this work, we have investigated ballistic transport properties of multilayer BP TFETs. We applied HfO_2 as the gate oxide and revealed that clean interface is obtained between monolayer BP and the (111) surface of HfO_2.

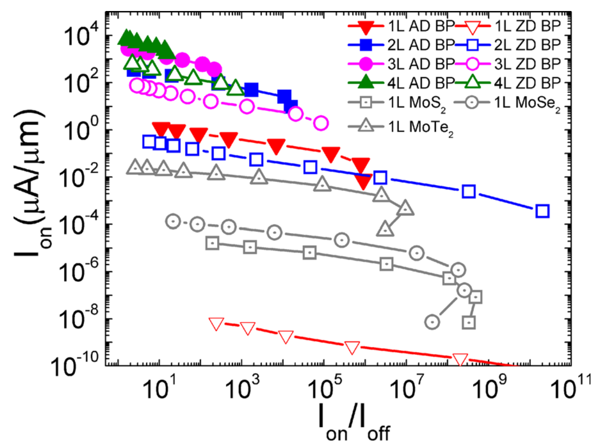

FIG. 5. I_{on} as a function of I_{on}/I_{off} ratio for 10 nm multilayer BP TFETs and TMDC TFETs with $V_D = 0.5$ V.

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The drain current of BP TFETs is found to greatly depend on the transport direction and the thickness of the BP film. There is an optimal combination of transport direction and thickness of the BP film for achieving optimal device performance. On-current can be improved by using thicker BP in TFETs, while leakage current is increased at the same time. It is shown that lower doping concentration and smaller drain voltage have to be applied to suppress the leakage current in multilayer BP TFETs. Compared with three typical monolayer TMDC (MoS_2, $MoSe_2$, and $MoTe_2$) TFETs, the monolayer BP TFETs in AD give promising performance of higher on-state current at the same I_{on}/I_{off} ratio. Note that the ballistic transport reported here sets the device performance limit. On the other hand, for practical systems there are other factors affecting the eventual outcome, including contact resistance, BP-substrate interaction, interface charge traps, scattering, as well as other fabrication and structural issues. Further theoretical and experimental investigations on these factors are necessary for an ultimate assessment of device performance of phosphorene TFETs.

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