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Fluorinated Graphene as High Performance Dielectric Materials and the Applications for Graphene Nanoelectronics

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There is broad interest in surface functionalization of 2D materials and its related applications. In this work, we present a novel graphene layer transistor fabricated by introducing fluorinated graphene (fluorographene), one of the thinnest 2D insulator, as the gate dielectric material. For the first time, the dielectric properties of fluorographene, including its dielectric constant, frequency dispersion, breakdown electric field and thermal stability, were comprehensively investigated. We found that fluorographene with extremely thin thickness (5 nm) can sustain high resistance at temperature up to 400 °C. The measured breakdown electric field is higher than 10 MV cm⁻¹, which is the highest value for dielectric materials in this thickness. Moreover, a proof-of-concept methodology, one-step fluorination of 10-layered graphene, is readily to obtain the fluorographene/graphene heterostructures, where the top-gated transistor based on this structure exhibits an average carrier mobility above 760 cm²/Vs, higher than that obtained when SiO₂ and GO were used as gate dielectric materials. The demonstrated fluorographene shows excellent dielectric properties with fast and scalable processing, providing a universal applications for the integration of versatile nano-electronic devices.

Graphene is a potential candidate material for use in building next-generation nanoelectronic and optoelectronic devices due to its unique properties (e.g., optical transparency, mechanical flexibility and superior high carrier mobility)^{1–6}. Mono- or few-layer graphene is typically used to build field effect transistors (FETs) on oxidized silicon wafers (graphene-on-insulator architecture); these devices can then be used to investigate the carrier transport properties of such component materials^{7–9}. However, graphene-on-insulator architectures, so-called pseudo-MOS structures, are not realistic device architectures. To be compatible with standard CMOS and IC architectures, top-gated graphene transistors are required. Top-gated FETs based on graphene are made by first depositing SiO₂ as gate dielectric material¹⁰. Unfortunately, SiO₂ dielectric layers degrade the carrier mobility of graphene due to the trapping charge density at the interface and damaging the graphene itself. Uniform gate insulators with a reduced number of interfacial defects and trapping states must be fabricated for use in graphene-based devices. For instance, uniform Al₂O₃ and HfO₂ layers with well-defined thickness can be deposited using atomic layer deposition (ALD) systems. However, seed layers composed of materials such as oxidized aluminum and low-*k* polymers are required for H₂O-based ALD deposition on graphene because of the hydrophobic nature of the graphene surface^{11–13}. Recently, hexagonal boron nitride (*h*-BN) has been utilized as a novel gate dielectric; this material shows promising electrical and dielectric properties in transistor devices, but integration and scaling are still challenging¹⁴. One type of graphene-based insulator, graphene oxide (GO), is often applied as a gate dielectric material in electronic devices, such as resistive random-access memory (RRAM) and thin film transistors^{15–20}. However, the low thermal stability of GO reduces its dielectric resistivity, which is a drawback since thermal processing steps are often used during device fabrication. Thus, it is of great challenge to find new suitable dielectric materials for use in the fabrication of nano-scale devices.



Fluorinated graphene (fluorographene), one of the thinnest insulators known, is an attractive 2D material. Fluorographene exhibits a mechanical strength comparable to that of pristine graphene, and its conductivity can be modulated from semi-metallic to insulating by tuning its stoichiometry (i.e., its carbon-to-fluorine ratio (C/F))²¹. A theoretical calculation reveals that by partially fluorinating graphene (from C₃₂F to C₄F) the energy bandgap of the material can be modulated from 0.8 to 2.9 eV. Several experimental results have demonstrated the band gap and electronic transport properties of fluorinated graphene^{22–24}. As a result, versatile graphene-based devices have been fabricated by chemically insulating pristine graphene. Withers et al. demonstrate the approach to selectively reduce insulating fluorinated graphene to conducting and semiconducting graphene by electron beam irradiation²⁵. Lee et al. selectively fluorinated graphene using irradiating a fluoropolymer-covered graphene sample with a laser²⁶. Graphene nano-ribbon (GNR) transistors with 35 nm channel widths were also realized using probe lithography. Specifically, a polymer nanowire mask was used to selectively expose graphene to ambient XeF₂ gas ambient²⁷. Recently, we have successfully fabricated a unique semi-metal/semiconductor/insulator heterojunction structure directly using a single graphene sheet via a selective fluorination process²⁸. This technique can potentially be used for the integration of electronics at the single atomic layer scale. Herein, we present a novel graphene-based field effect transistor architecture in which fluorographene is introduced as the gate dielectric material. The CVD-grown graphene was fluorinated using a low-damaged CF₄ plasma treatment, which allows for its integration with IC fabrication to achieve large-area processing²⁸. During this process, a filter is inserted between the CF₄ plasma and graphene sheet to reduce damage caused by high energy radicals and UV photons.

The dielectric properties of multi-layer fluorographene (e.g., dielectric constant, frequency dispersion, breakdown electric field (E_{BD}) and thermal stability) were comprehensively investigated. We found that fluorographene with extremely thin thickness (5 nm) can sustain high effective resistance when it is annealed at temperatures up to 400°C in an ambient environment. The dielectric constant was found to be ~ 1.2 , and the breakdown electric field (E_{BD}) was found to be higher than 10 MV cm⁻¹. This E_{BD} value is much higher than that reported for stacked graphene oxide, and it is comparable to that of bulk Si₃N₄ and SiO₂²⁹. More importantly, a proof-of-concept methodology, one-step fluorination of 10-layered graphene, is used to obtain the fluorographene/graphene heterojunction structure, where the top-gated transistor based on this structure exhibits an average carrier mobility above 760 cm² V⁻¹ s⁻¹ (higher than that of graphene oxide and AlO_x). The proposed device fabrication is very promising for future integration of scaled and high-density electronics.

Results

Metal-insulator-metal (MIM) capacitors with a Ti/fluorographene/Ti sandwich structure were fabricated to study the gate dielectric properties of fluorographene. The fluorographene was made by transferring and stacking 10-layers (10-L) of fluorinated graphene monolayer that was initially grown on Cu by CVD (see experimental section for details). It is worth noting that stacks of fluorographene less than 10-L thick show high leakage currents (~ 150 nA). Therefore, the measured dielectric properties shown in this work are based on 10-L of fluorographene (thickness ~ 5 nm as measured by TEM). Figure 1a shows the measured capacitance and the dielectric constant as a function of the applied voltage (-3 to $+3$ V). A stable capacitance value of ~ 210 nF/cm² (normalized to 1 cm²) was observed; variations in the capacitance up to a voltage bias of ± 3 V were not observed. Moreover, the dielectric constant of fluorographene was found to be ~ 1.2 , independent of the sweep in the bias voltage. These results suggest the stable dielectric properties of this multi-layered fluorographene. Figure 1b shows the capacitance-

dependent frequency dispersion of 10 L of fluorographene. The capacitance of fluorographene decreased from 230 to 200 nF cm⁻² as the frequency increased from 20 to 100 kHz, indicating that this material could be steady under high frequency operation. The reported frequency dispersion based on GO as the dielectric material is indicated by the red star in Figure 1b for comparison¹⁶. As concluded from the data shown in Figure 1c, the capacitance of both fluorographene and GO are reduced by about 10% when the frequency is increased up to 100 kHz. Moreover, the breakdown strength of fluorographene was measured by varying the electric field from 0 to 20 MV cm⁻¹ at room temperature. The statistical data compiled in Figure 1d reveal that the breakdown electric fields of GO¹⁶ and fluorographene were found to be 1.5 MV cm⁻¹ and 12 MV cm⁻¹, respectively. The fluorographene sample with 10 L is highly insulating with a low electric field-dependent leakage current 46.2 μ A cm⁻² at a bias field up to 10 MV cm⁻¹ (Figure 1e). The dielectric performance of the fluorographene sample (5 nm thick) is superior to that of the GO sample (70 nm thick). It is unexpected that the as-prepared thin fluorographene sample could sustain a high electric field comparable to bulk silicon dioxide²⁹. To further investigate the thermal stability of dielectrics made from fluorographene, we prepared a two-terminal diode using Ti contact electrodes by annealing the samples in a furnace using temperatures ranging from 100°C to 400°C in an ambient environment. According to their I–V curves, those samples subjected to temperatures less than 200°C retained high dielectric resistivities, showed non-ohmic contact behavior, and sustained measured currents of a few pAs. At higher annealing temperatures (up to 400°C), the samples exhibited diode-like behavior with currents as high as 200 pA. It is likely that in this case, the as-synthesized fluorographene was beginning to decompose because the C-F bonds become unstable at temperatures above 260°C³⁰. However, the effective resistivity ($R = V/I$) of the sample at 400°C was measured to be 1.45 G Ω ; thus, the sample was still highly insulating (the applied source-drain voltage is normally less than 10 V). The maintain of insulating character is possibly due to the formation of highly defective (vacancies) layers, where CF₄ and C₂F₆ gas are evolved during thermal defluorination resulting in defects and disruption within the layer. Dielectric materials used in IC and CMOS fabrication must be able to withstand high temperature post-annealing processes. The fluorographene dielectrics in this work maintain high resistivities up to temperatures of 400°C; thus, their properties are comparable to those of Teflon® and superior to those of GO, which rapidly undergoes oxygen desorption at 200°C³¹. Moreover, it is important to investigate the dependence of the electric field stress on the device resistance. Fluorographene exhibits insulating behavior ($\sim 10^9 \Omega \text{ sq}^{-1}$)²¹, while the resistivity of GO³² is only few 10 s of M $\Omega \text{ sq}^{-1}$. GO has been used as a dielectric material in resistive random-access memory (RRAM)¹⁵, but GO becomes unstable under electric field stress because conductive paths are formed as oxygen migrates along the GO stacking layers. Therefore, GO dielectric materials at least 70 nm thick must be used so that leakage currents are eliminated¹⁶. Table S1 compares the electrical performance of graphene-based FETs composed of various dielectric materials, including thermally evaporated SiO₂, ALD-synthesized Al₂O₃ and HfO₂, CVD-synthesized Si₃N₄, *h*-BN films, and GO films. The amount of drain-induced barrier lowering (DIBL), an effect of short-channel effect in MOSFETs, is often quantified to evaluate the integrity of a device upon downscaling. The electrostatic scaling length can be modeled as $\lambda = (\epsilon_s t_s t_{ox} / \epsilon_{ox})^{1/2}$ for a planar device structure³³, where t_s and t_{ox} are the thicknesses of the channel and gate oxide, respectively, and ϵ_s and ϵ_{ox} are the dielectric constants of the channel and gate oxide, respectively. The common approach to suppressing this DIBL effect is to decrease the scaling length λ by reducing the channel thickness; thus, a reduced Si thickness was pursued by the extremely thin silicon-on-insulator (ETSOI) method. Unfortunately, the mobility decreased as the thickness was scaled

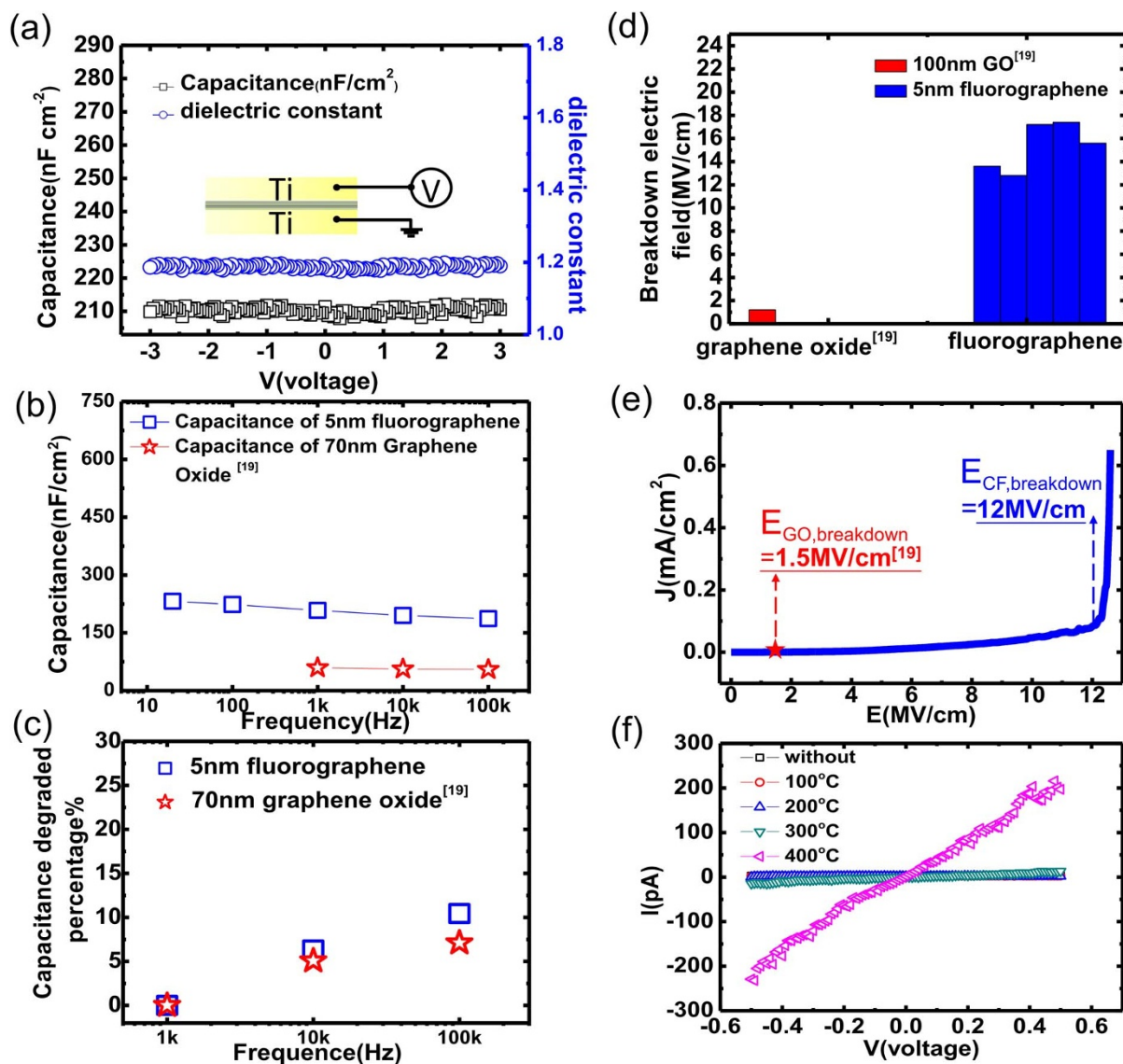


Figure 1 | Analysis of the dielectric properties of fluorographene: (a) Capacitance value and dielectric constant of fluorographene. The inset shows a schematic of a MIM capacitor. (b) and (c) Frequency dependence and the percentage of capacitance degradation for fluorographene and GO. (d) Dielectric breakdown of 10 L of fluorographene and graphene oxide (GO). (e) The current density of the fluorographene capacitor in (d). (f) Current-voltage measurement of single-layer fluorographene subjected to different annealing temperatures.

down³⁴. Alternatively, this issue can be addressed by reducing the thickness of the channel and gate dielectric, preserving the high gate dielectric constant. Our presented structure, composed of atomically thin graphene and fluorographene as channel and dielectric materials, respectively, is therefore a promising candidate in this regard. The data indicate that, although they are very thin (<10 nm), the fluorographene samples studied here are sustainable at high gate voltages. Moreover, lower sub-threshold swing (SS) implies the channel current can be efficiently gated by applying lower gate voltage, suggesting the less power dissipation to operate a transistor³⁵. For transistor with fluorinated graphene as dielectric layer, larger capacitance and lower sub-threshold swing could be achieved. A device made from such an extremely thin material would have the potential to be scaled down to the atomic level and be operated with less power dissipation.

Discussion

The fluorographene dielectric film studied here is made by stacking ten individual fluorographene layers (a transfer process was performed 10 times). This process is complicated and could hinder

the use of such a material in particular applications. Consequently, we devised a way to synthesize the dielectric layer using a one-step fluorination process (a 60 min treatment) on a multi-layered graphene film, composed of either 3, 5, or 10 layers of graphene (the schematics shown in Figure 2a). Briefly, multi-layered fluorographene is created when high energy fluorine radicals induced by the plasma diffuse into the multi-layer graphene film. Figure 2b shows a typical Raman spectrum of a fluorinated multi-layer graphene sample, where the G peak (at $\sim 1585\text{ cm}^{-1}$) and 2D peak (at $\sim 2700\text{ cm}^{-1}$) are characteristic of the sp^2 -hybridized C-C bonds in graphene. Compared with pristine graphene, the D peak of the fluorographene at 1358 cm^{-1} is much more intense, indicative of lattice disorder. Moreover, the G peak of the fluorographene is broad, and the shoulder D' peak is pronounced due to intra-valley scattering³¹, indicative of the formation of sp^3 -defects (C-F bonding) on the graphene plane. Figure 1c shows a typical XPS spectrum of a fluorinated graphene sample; the C 1s peak at 288.2 eV and the F 1s peak at 688.8 eV indicate the formation of C-F bonding states. The detail bonding states, including C-CF(286.3 eV), CF(289.4 eV), CF₂(292.2 eV), CF₃(293.1 eV), were also observed from the de-

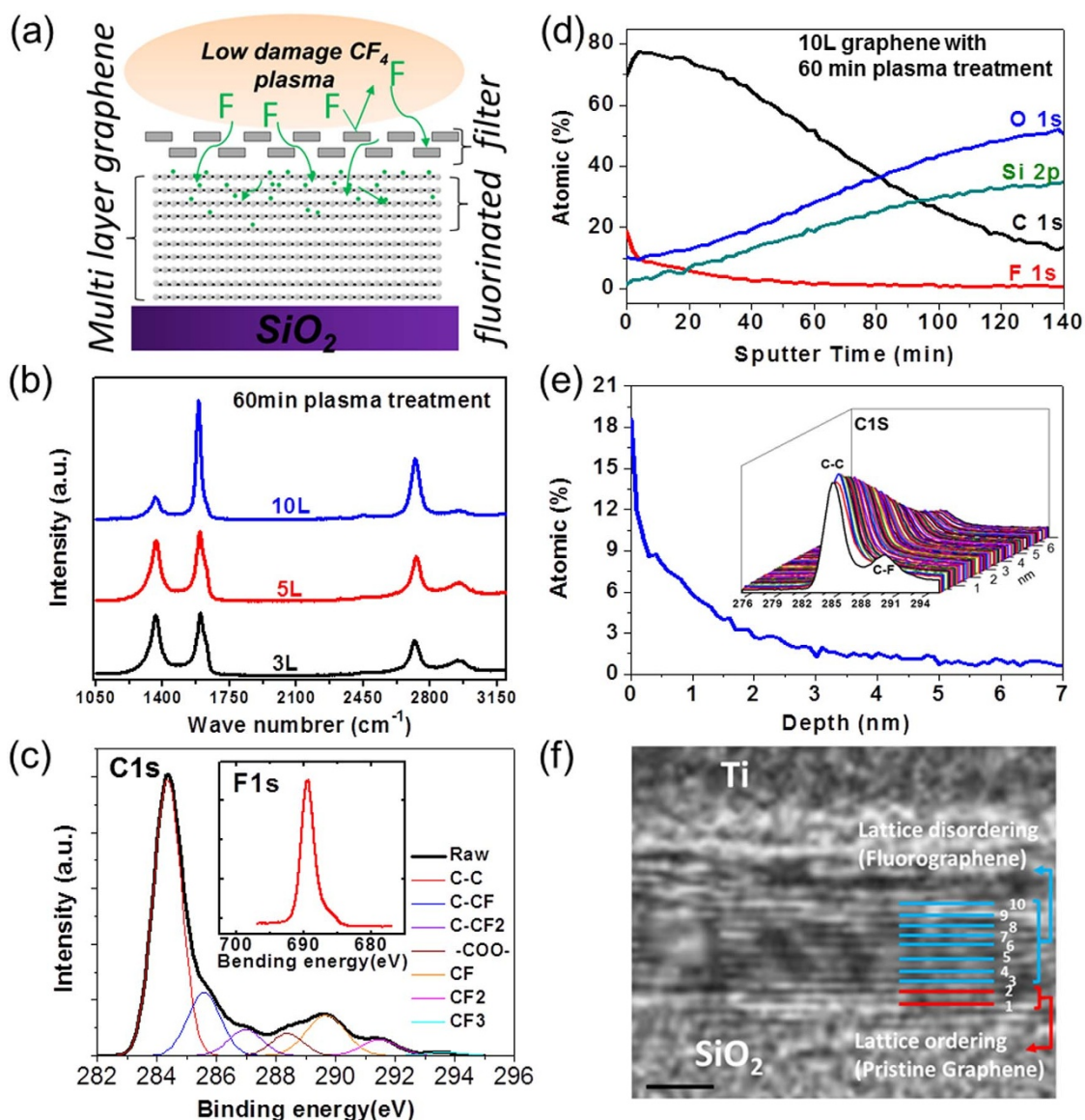


Figure 2 | (a) A schematic of multilayer graphene during CF_4 plasma treatment. (b) The evolution of the Raman spectra of 3 L, 5 L and 10 L of graphene after 60 min of plasma treatment. (c) XPS analysis of fluorographene, where the C 1s core level and several carbon-fluorine components are labeled. The inset shows the fluorine peak (F 1s) at 688.8 eV. (d) The elemental distribution of XPS depth profile for 10 L graphene and (e) the magnification of the changes for F at%, the inset shows the C1s spectra acquired along sample depth. (f) A TEM image of 10 L of fluorographene subjected to one-step fluoridation. The top 6–8 layers exhibit disordered lattice fringes (fluorographene) while the bottom 2–3 layers exhibit a highly ordered lattice (pristine graphene). The inset scale bar is 2 nm.

convolution of C1s spectrum. The spectra of fluorographene samples that are 3 and 5 layers thick are shown in Figure S1. According to XPS on 3 L sample, the estimated F/C ratio is 0.25, higher than that of 5 L (0.22) and 10 L (0.21). To further clarify the stoichiometric distribution along the depth profile of multi-layer fluorographene, we performed XPS depth profile analysis on the samples. The C and F signals from this spectral survey on the sample surface are clearly observed (Figure S2). The XPS depth profile shows that the distribution of fluorine atoms (Figure 2d and 2e) decreases as deeper sample depths are probed (from 15.9 ± 2.6 at% on surface to 0.06 ± 0.014 at% near the bottom), suggesting that different degrees of fluorination are achieved (e.g., from high near the surface to low near the bottom) during this one-step fluorination process. The F/C and CF_2/CF ratio for this sample have been concluded in Table S2. The C-F₂ and C-F₃ indicate the structural defects on graphene and occurs mainly at defect such as vacancies, edge, or graphene boundaries²¹. The defects were introduced from the graphene transfer process.

Therefore, it is reasonable that more transferred graphene layers result in higher ratio of CF_2/CF ratio. The stacking layer preserves its layer structure (Figure 2f), indicating that CF plasma treatment does not severely harm the sample. Moreover, the bright-field TEM image (Figure 2f) of the top 6–8 atomic layers shows a disordered lattice fringe, while the bottom 2–3 layers exhibit a highly ordered lattice arrangement. The disordered arrangement can be attributed to the formation of fluorographene, where the lattice distortion resulted from the introduction of carbon fluoride bonds (C-F₂, C-F₃ and C-F), while the unfluorinated graphene (i.e., pristine graphene) is characterized by a highly ordered lattice. This result is consistent with the reported work on fluorinated carbon nano-fibers (CNF), for which the fluorinated part located near the surface and the unfluorinated CNF core can be distinguished by their lattice ordering³⁷.

We characterized the electrical transport properties of 3-, 5- and 10- layered fluorographene samples (60 min plasma treatment; the resistor shown in inset in Figure 3c). Prior to the fluorination of these

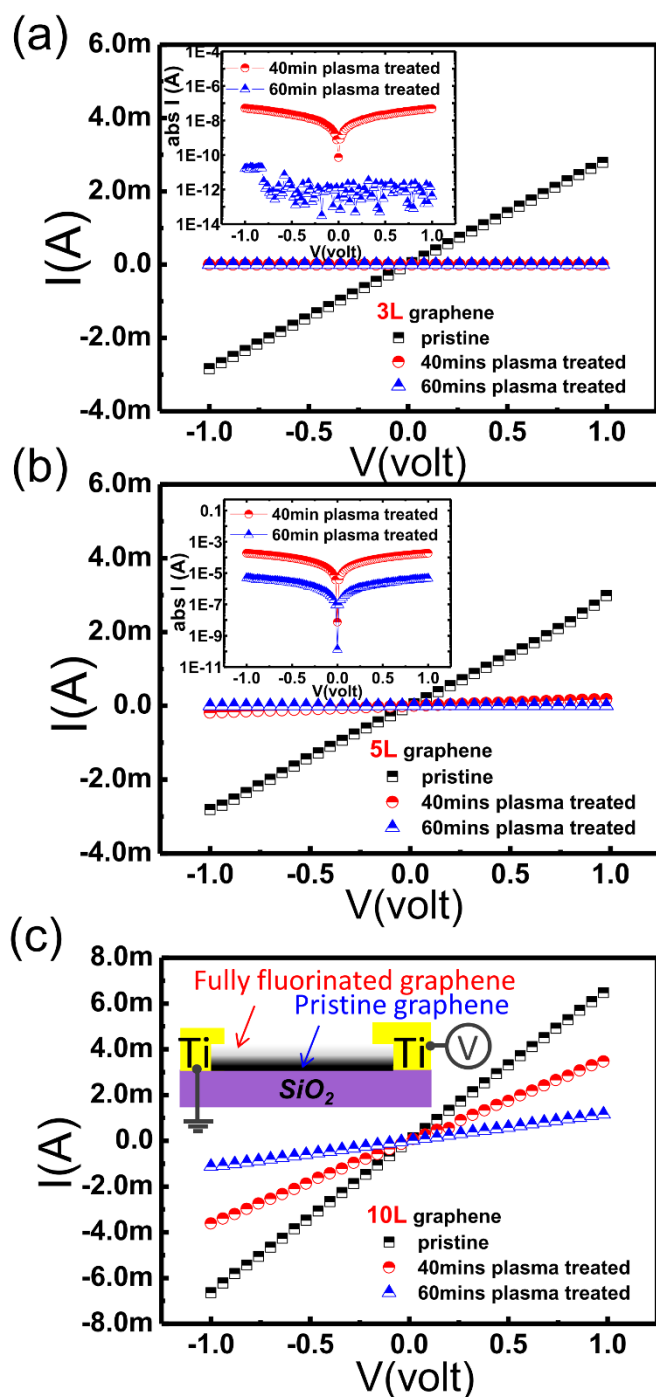


Figure 3 | Current-voltage curves for (a) 3 L, (b) 5 L and (c) 10 L of graphene after different durations of plasma treatment. The insets in (a) and (b) are the log-scaled I - V curves for 40 and 60 min fluorinations, respectively. The inset in (c) shows a schematic of the graphene resistor.

multi-layered graphene (MLG) samples, their I - V curves shows perfect ohmic contact (Figure 3). The current values (at 1 V) obtained were proportional to the number of graphene layers. The current values decreased when the fluorination time was increased from 40 to 60 min. For 3-layer fluorographene, the currents decreased from the μA to the pA level as the fluorination time was increased from 40 to 60 minutes, indicating that the sample was highly fluorinated (F/C:0.25). For the 5-layer fluorographene sample, the measured current did not decrease to the pA level, implying that the top 3 layers of the sample were highly fluorinated (insulating), while the bottom 2 layers were partially fluorinated (semiconducting) (Figure 2b). Here,

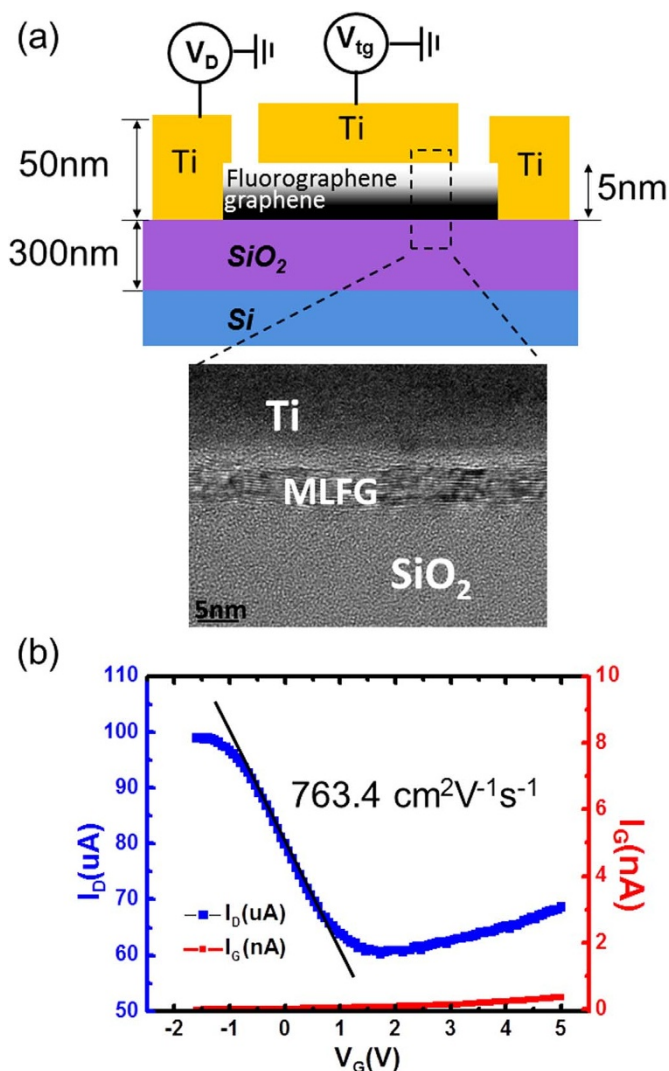


Figure 4 | (a) An illustration of a graphene-based FET composed of a fluorographene gate dielectric and the corresponding TEM cross-sectional image. (b) The transfer characteristics and the monitored gate current (I_G) of these transistors, which demonstrate hole mobilities of $760 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at $V_D = 0.5 \text{ V}$.

it was found out that fluorination occurs deep within the bottom layers of a multi-staked graphene sample, while fluorination in previous work employing XeF_2 exposure was limited to the top layer of the sample²¹. In Figure 3c, currents of a few mini-amperes are observed for both the fluorinated and unfluorinated 10-L graphene samples, indicating that highly conductive pristine graphene persists in the bottom few layers of the sample (near the SiO_2 /graphene interface) even after 60 min of plasma treatment. These results are consistent with those obtained from the XPS depth profile and TEM analysis (Figure 2e-f).

As a proof-of-concept, the 10-layered fluorographene sample was investigated as a dielectric material in a graphene-based FET. Figure 4a shows a schematics of the device structure; the channel (length = $20 \mu\text{m}$, width = $4 \mu\text{m}$) was patterned using traditional photolithography techniques. The cross-sectional TEM image clearly shows that multi-layered graphene, composed of fluorographene and pristine graphene (Figure 2f), is formed between the top gate (Ti) and the SiO_2 substrate. Figure 4b shows the transfer curves for this device, where the drain-source voltage (V_{DS}) was kept at 0.5 V and the gate voltage was swept from -2 to 5 V. The neutrality point appears at a positive voltage, indicating p -type doping on the gra-



phene channel likely because there is a strong electron acceptor above the fluorographene. Moreover, the leakage current is less than 0.5 nA when gate voltages up to 5 V are applied, suggesting that the sample has excellent dielectric properties. The equation, $\mu = (L/WC_{ox}V_D)(\Delta I_D/\Delta V_G)^{38}$, was used to extract the field effect carrier mobility from the linear regime of the transfer curves, where L , W and C_{ox} are the channel length, the channel width and the gate capacitance, respectively. The field effect hole mobility was measured to be greater than $763.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (detailed calculation in S3), higher than that obtained when SiO_2 and GO were used as gate dielectric materials^{16,17,20}. Thus, the fluorographene devices investigated here have superior mobilities compared to silicon-based FETs composed of ultra-thin Si films (3.7 nm) (silicon-on-insulators (SOIs)) that typically have mobilities of $60 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-139}$. These fluorographene devices are promising for device scaling in CMOS applications.

Conclusion

In summary, fluorographene was utilized as the gate dielectric in a graphene-based field effect transistor. The fluorographene dielectric exhibited a high breakdown electric field (10 MV cm^{-1}), and it is promising for use in applications and, in principle, for wafer-scale fabrication. Moreover, a one-step process for fluorinating multi-layered graphene (5 nm thick) that could be used to form a unique vertical heterostructures was demonstrated. This structure could readily be used as graphene-based FET, and it was found to have a high carrier mobility ($760 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$). This present method has the potential to be used in the fabrication of next-generation nano-electronic devices.

Methods

CVD growth and transfer process. We described a detailed process for using CVD to grow graphene on Cu in previous work²⁴. Briefly, copper (Cu) foil was loaded into a tube furnace. The growth temperature was set to 1000°C . A gas composed of methane and hydrogen ($\text{CH}_4/\text{H}_2 = 20 \text{ sccm}/20 \text{ sccm}$) was introduced for 20 min. The system was then cooled down to room temperature (cooling rate $\sim 5^\circ\text{C s}^{-1}$), completing the growth process. The transfer process was based on the conventional poly(methyl methacrylate) (PMMA) method.

Graphene fluorination. The PECVD chamber was evacuated to $\sim 5 \text{ mTorr}$, and the temperature was increased from room temperature to 200°C . After the CF_4 gas was introduced into the chamber, the gas flow and pressure were controlled. The degree of fluorination of the sample was adjusted by controlling the exposure time (from 40 to 60 min) after the plasma was ignited.

Ti/fluorographene/Ti capacitor. The MIM capacitor was made according to the following steps: (i) evaporate Ti (100 nm) onto SiO_2/Si (300 nm) to make the bottom electrode, (ii) grow graphene on Cu foil and fluorinate the sample for 30 min, (iii) transfer the fluorinated graphene onto the Ti (10 times) and (iv) deposit the Ti top electrode and pattern it using a lift-off technique.

Graphene-based field effect transistor. The device was made using the following process: (i) 10 layers of CVD-grown graphene (on SiO_2/Si) sheets were stacked using a transfer process and the device channel was patterned using traditional lithography followed by a O_2 plasma etching step, (ii) the source and drain Ti electrodes (50 nm) were deposited using a thermal evaporator, (iii) the fluorographene dielectric layer was completed after 60 min of fluorination and (iv) the Ti top gate electrode (50 nm) was formed during thermal evaporation and lift-off.

Raman scattering spectral analysis. Raman scattering spectra were collected using a NT-MDT confocal Raman microscope system (laser excitation wavelength = 473 nm ; laser spot-size $\sim 0.5 \mu\text{m}$). The Raman scattering peak of Si at 520 cm^{-1} was used as a reference for wavenumber calibration.

X-ray photoelectron spectroscopy. The chemical configurations were determined using an X-ray photoelectron spectrometer (XPS, Phi V6000). The XPS measurements were performed using a Mg K α x-ray source for sample excitation. The energies were calibrated relative to the C 1 s peak to eliminate the charging of the sample during analysis. The XPS depth profile analysis was carried out by comprised of Ar ion sputtering (Iron gun: 3 kV , $1 \mu\text{m}$) and the X-ray probe (probing energy of X-ray: 108 W and 15 kV). The etching rate is 0.1 nm/sec and it was more than 70 points been acquired for 10 L graphene sample.

Electrical measurement. The electrical measurements were performed in an ambient environment using an Agilent B1500A semiconductor device parameter analyzer.

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Author contributions

K.I.H. performed the major part of the experiments. C.H.H. and J.H.L. help on XPS and device fabrication. W.Z. and L.J.L. help to do Raman characterization on graphene sample.

C.S.L. analysis the device performance. C.Y.S. conceived the idea and wrote the paper. All the authors discussed the results, commented on and revised the manuscript.

Additional information

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