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Wafer-Scale, Highly Uniform Surface Functionalization from Vapor Phase and Applications to Organic Transistors

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The surface functionalization by self-assembled monolayers (SAMs) favors well-packed organic semiconductor growth and reduces interfacial traps, which assists in developing high-performance organic thin-film transistors (OTFTs). Herein, the conventional SAM growth from the vapor phase is ameliorated and systematically studied. With 1H,1H,2H,2H-Perfluorodecyl-trichlorosilane as an example, it is found that deposition temperature of no less than 120 °C and deposition pressure of up to 0.02 bar is preferred for SAM deposition without morphological defects. The optimized SAMs are ultrasmooth with a surface roughness of 0.09 nm and can be escalated to wafer scale. It is verified that the growth condition is universal for other trichlorosilane species. Finally, it is shown that the OTFTs with defect-free SAMs can achieve an average mobility of 1.79 cm^2 V^{-1} s^{-1} using dinaphtho(2,3-b:2′,3′-f) thieno(3,2-b)thiophene as the active layer, which is 2.06 times to the devices with defective SAMs and paces up the large-area and high-performance organic electronics.

1. Introduction

The surface functionalization by self-assembled monolayers (SAMs) provides fine control over superficial/interfacial properties and enables a wide range of applications, including nanoimprint technology,[1] microelectromechanical systems, etc.[2] Particularly, it is believed that surface functionalization could alter the surface energy and reduce the interfacial trap states and hence is broadly integrated into the fabrications and optimizations of the organic thin-film transistors (OTFTs). For example, octadecyltrichlorosilane (OTS) with low surface energy is employed for enabling well-oriented organic semiconductor thin films.[3–7] The phenyltrichlorosilane (PTS) is frequently utilized for the solution-processed single-crystalline organic layer growth owing to the higher surface energy over the common organic semiconductor solvents (heptane, toluene, *m*-xylene, etc.) and ensures a good wettability.[8–11] The highly ordered active layer and the high-quality organic semiconductor-dielectric interface with negligible trap states are the essential building blocks to enable high-performance OTFTs and OTFT-based applications, which cover over a wide range of areas, including the logic circuits,[6,12–14] sensors,[15–17] memory devices and display drivers.[5,18,19] Moreover, it is fascinating that surface functionalization can effectively modulate the channel carrier density and provide fine control over the threshold voltage,[20,21] which necessitates high-quality surface treatment. However, due to the complexity of the fabrication process, the morphological defects generated during the growth of SAMs immensely affect the quality of the surface functionalization and the OTFT performance. Accordingly, surface functionalization with negligible morphological defects is highly desired.

The surface functionalizing SAMs are typically grown from either solution or vapor phase.[22] In the liquid phase method, the substrates are generally immersed into the SAM solutions for several hours and even up to tens of hours.[4–6,8,10] Although the quality of the surface functionalization based on the immersion method could be improved by optimizing the deposition temperature and the solvent,[23,24] the long processing time allows the organosilane molecules to form aggregations, and the subsequent deposition on the substrate surface leads to the irregular defects on the substrate surface. The phenomena have been observed and reported previously.[6,25,26] As the solvents-free approach, the surface functionalization by vapor phase avoids the issues associated with the solution method,[27] such as effects originated from viscosity and polarity of the solvent,[24] the diffusion-limited transport of the organosilane molecules onto the substrate, the uncertain reaction of organosilanes in

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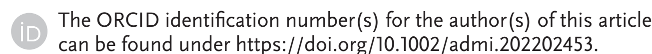
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the solvents, etc.[28] In the vapor phase approach, the silane liquids evaporate and the molecules are deposited on the substrates to form the SAMs. Normally, control over temperature and vacuum degree is required to accelerate the silane vaporization. One more distinct feature of the vapor phase is the better reproducibility and scalability, compatible with the manufacture of large-area electronics,[27,29] which hence meets the commercialization requirement. Although many efforts have been devoted to SAM deposition, how to provide a favorable growth environment and optimize the processing conditions to eliminate the morphological defects and ultimately reach wafer-scale functionalization remains unclear.

The conventional vapor phase approach is usually suffering from contamination from the reaction vessel. We have found that the employment of an extra glass petri dish covered with aluminum (Al) foil could effectively reduce the contamination from the vessel and confine the vapor in a localized area, eventually attaining high-quality SAMs without morphological defects. Herein, the vapor phase growing approach is systematically studied with 1H,1H,2H,2H-perfluorodecyltrichlorosilane (FDTS) for high-quality surface functionalization. The processing parameters are adopted based on the derived vapor pressure of the FDTS and ameliorated by varying the processing parameters, including the deposition temperature (T_D) and the deposition pressure (P_D). After optimization, morphological defects-free and up-to-wafer-scale SAMs are attained with a surface roughness (R_q) of 0.09 nm. It was found that this protocol is universal when applied to other trichlorosilane materials, that is, OTS and PTS. The defect-free surface functionalization of OTS is then employed in the organic thin-film transistors for achieving a high-quality organic semiconductor-dielectric interface with the organic semiconductor of dinaphtho(2,3-b:2′,3′-f)thieno(3,2-b)thiophene (DNTT). The transistors with defect-free SAMs show an average carrier mobility (μ) of 1.79 $cm^2\ V^{-1}\ s^{-1}$, which is 2.06 times compared to the devices fabricated from defective SAMs. This study provides a general approach for surface functionalization without morphological defects to improve charge carrier mobility. In addition, the wafer-scale depositions have enabled large-area device fabrication and foreshadowed the high integration and mass production of organic electronics. Not only limited to OTFTs, but the defect-free SAMs are also favorable for diverse applications regarding surface functionalization.

2. Results and Discussion

The silanes utilized are identical in the -$SiCl_3$ head to be specifically anchored onto the silicon (Si) substrate but differ in the functional groups. **Figure 1**a depicts the molecular structures of PTS, FDTS, and OTS with distinct terminal groups. Herein, the frequently used FDTS with highly nonpolar characteristics is employed for the growth study.[29–31] As would be discussed in the following, the highly dispersive feature allows the evaluation of the saturated vapor pressure and favors the deposition parameter determination. As shown in Figure 1b, surface functionalization is accomplished by allowing an aluminum foil-covered glass petri dish standing in the vessel, which contains both the silane solution and the Si substrates. To facilitate the FDTS vaporization, the vessel is heated and pumped down to a high vacuum degree (0.02 bar). As presented in Figure 1c, the FDTS vapor diffuses and is adsorbed onto the substrate to form the self-assembled monolayer by covalent bonding (the inset in Figure 1c).

The evaporation behavior of FDTS is correlated to the vapor pressure (p), which relies on both the deposition temperature, and the boiling points (T_B) of the silanes. As shown in Equation (1), the dependence of vapor pressure on the

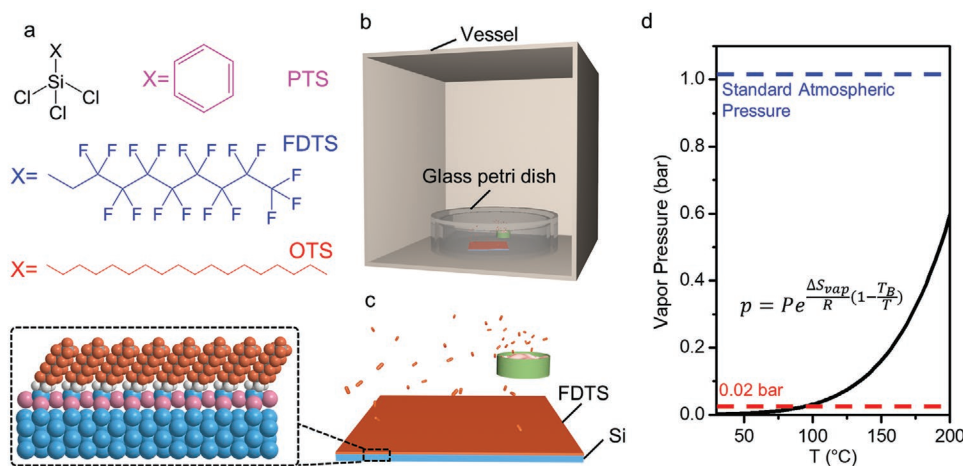

Figure 1. The deposition of silanes from the vapor phase. a) Molecular structure of silanes utilized in the study. Apart from the $-SiCl_3$ head, the terminals of X are the functional groups. Typically, the molecules represent PTS (pink), FDTS (blue), and OTS (red) by varying the functional groups. b) Schematic diagram of the surface functionalization with FDTS. A glass petri dish containing both FDTS and oxygen plasma-treated Si is placed inside the reaction vessel. The Al foil covering the glass petri dish is omitted for better clarification. c) Surface functionalization process inside the glass petri dish. As the precursor evaporates under environments of high temperature and high vacuum degree, the FDTS molecules are deposited on the substrate. The inset shows the schematic illustration of the molecules packing of FDTS on the substrate as depicted by the rectangle in black dash line. d) Vapor pressure of FDTS with respect to the temperature by plugging the parameters into the equation as shown in the plot. The two dash lines represent the standard atmospheric pressure (blue dash line) and 0.02 bar (red dash line), respectively.

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temperature (T) is well described by the Clausius-Clapeyron equation:[32,33]

$$\ln\left(\frac{p_2}{p_1}\right) = -\frac{L_H}{R}\left(\frac{1}{T_2} - \frac{1}{T_1}\right) \tag{1}$$

where the subscripts of 1 and 2 denote different states, L_H is the latent heat or enthalpy of vaporization (ΔH_{vap}) and R is the ideal gas constant (8.314 J mol^{-1} K^{-1}). As state 1 reaches the equilibrium evaporation state, the p_1 and T_1 could be replaced by the standard atmospheric pressure (P) and boiling point, namely $p_1 = P$ and $T_1 = T_B$. The Equation (1) is then reduced to:

$$\ln\left(\frac{p}{P}\right) = -\frac{L_H}{R}\left(\frac{1}{T} - \frac{1}{T_B}\right) \tag{2}$$

Here we have removed the subscript of 2 and p and T represent pressure and temperature at arbitrary states. In the equilibrium state, the Gibbs free energy (ΔG) is zero and that is:

$$\Delta G = \Delta H_{vap} - T_B\,\Delta S_{vap} = 0 \tag{3}$$

In Equation (3), ΔS_{vap} is entropy at an equilibrium state. The L_H is then expressed by:

$$L_H = \Delta H_{vap} = T_B\,\Delta S_{vap} \tag{4}$$

The vapor pressure in exponential form is obtained by incorporating Equations (2),(4):

$$p = P\,e^{\frac{L_H}{R}\left(\frac{1}{T_B} - \frac{1}{T}\right)} = Pe^{\frac{\Delta S_{vap}}{R}\left(1 - \frac{T_B}{T}\right)} \tag{5}$$

Similar expressions have been derived elsewhere.[34] Thereafter, Trouton's law (i.e., $\Delta S_{vap} \approx 10.5R$) is applied for the estimation of the heat of evaporation at one atmospheric pressure, which generally agrees well with no polar compound.[35] The surface energy of FDTS is a dispersive term dominated with low polar components, validating the applicability of Trouton's law. By plugging the T_B information of FDTS (Table S1, Supporting Information) into Equation (5), the vapor pressure is outlined in Figure 1d. It can be seen that in the temperature range from 30 to 200 °C, the vapor pressure of FDTS is far below the standard atmospheric pressure (blue dash line), suggesting negligible evaporation. To facilitate the vaporization, the deposition pressure is greatly reduced to 0.02 bar (red dash line), which is comparable to the saturated vapor pressure.

The influence of the deposition temperature is investigated while maintaining the deposition pressure at 0.02 bar. Prior to the surface treatment, the morphology and surface energy of the original Si substrate are characterized. As shown in Figure S1 (Supporting Information), the surface scanned by the Atomic Force Microscope (AFM) is highly uniform with a low surface roughness of 0.09 nm and provides a superb platform for SAM growth. In addition, the surface energy of the unfunctionalized Si substrate is found to be 49.78 mJ m^{-2} (Figure S2, Supporting Information). **Figure 2**a–d depicts the surface morphology of FDTS film-covered Si substrate deposited from four different T_D, including 40, 80, 120, and 160 °C. The water contact angles are measured as shown in Figure 2e–h. All the contact angle values reveal a hydrophobic feature, indicating the successful deposition of FDTS. However, under the deposition temperature of 40 °C, the FDTS features island morphology and becomes dense for T_D = 80 °C, while a flat FDTS surface appears at high T_D (120 and 160 °C). As depicted by the profile along the white dash line, the height of the FDTS island is ≈2.6 nm, identical to the bilayer thickness. The bilayer phenomenon has been observed and reported previously, which could attribute to the formation and rupture of the inverse vesicles.[26] On the other hand, deposited from low temperatures, the FDTS molecules interact with each other and the substrate primarily by hydrogen bonding in between −Si−OH and are prone to move under thermal processing. The high T_D is required to eliminate the island structures and the FDTS film is condensed and locked to the substrate via cross-linked −Si−O−Si− bonding.[26]

To explore the effect of deposition pressure on the FDTS morphology, four distinct deposition pressures are applied at a constant high temperature of 120 °C. Figure 2i–l shows the AFM images of the FDTS-treated Si substrates under different pressures. Although the FDTS is successfully deposited as verified by the water contact angle (Figure 2m–p), the surface morphology differs greatly. As the degree of vacuum level escalates, the amount of the aggregates decreases gradually and ultimately vanishes when the P_D reaches 0.02 bar, implying that the high degree of vacuum level is imperative for the elimination of the aggregation defects. The height of the aggregates exceeds 10 nm as measured by the cross-section profile in the inset of Figure 2k, which differs from the bilayer defects. The contact angles do not change significantly and the dependence of contact angles on the processing variables and defects is not investigated here. The result here reveals that the contact angle measurements could not reflect the microscopic feature of surface modification. Normally, the deposition of SAMs involves hydrolysis and condensation steps.[26,36] The hydrolysis is essential for the deposition of SAMs since the silanetriols have a strong affinity to the hydroxyl substrate via hydrogen bonding.[26,37,38] In hydrolysis, the $-SiCl_3$ components of FDTS molecules interact with the water to form the −SiOH groups. The molecules with hydroxyl groups then form the −Si−O−Si− bonds in both the lateral direction to each other and the vertical direction to the Si substrate. Given the observed inverse relationship between the number of irregular spots and the vacuum degree, the aggregation is attributed to the high amount of water and enhanced hydrolysis associated with the deposition pressure.[24] When P_D is high, namely low vacuum degree, plenty of water molecules remain in the vessel and strengthen the hydrolysis reaction to generate the aggregates, which then fall on the substrate. The growth study of FDTS suggests that particular attention to the deposition temperature ($T_D \geq 120$ °C) and pressure ($P_D \leq 0.02$ bar) should be paid for spot-free surface functionalization.

As a significant property of surface functionalization, the surface energy of the FDTS films on Si substrate without morphological defects is determined by measuring the contact angles. Two standard liquids are employed, as shown in **Figure 3**a,b. The contact angles are 109.07 ± 2.08° and 97.75 ± 1.63° for water and diiodomethane, respectively. Both the contact values indicate the hydrophobic feature. The surface energy of 10.33 mJ m^{-2} including the dispersive term of 7.58 mJ m^{-2} and the polar term of 2.75 mJ m^{-2} is obtained for FDTS on Si substrate based on the Owen–Wendt–Rabel–Kaelble model. It is

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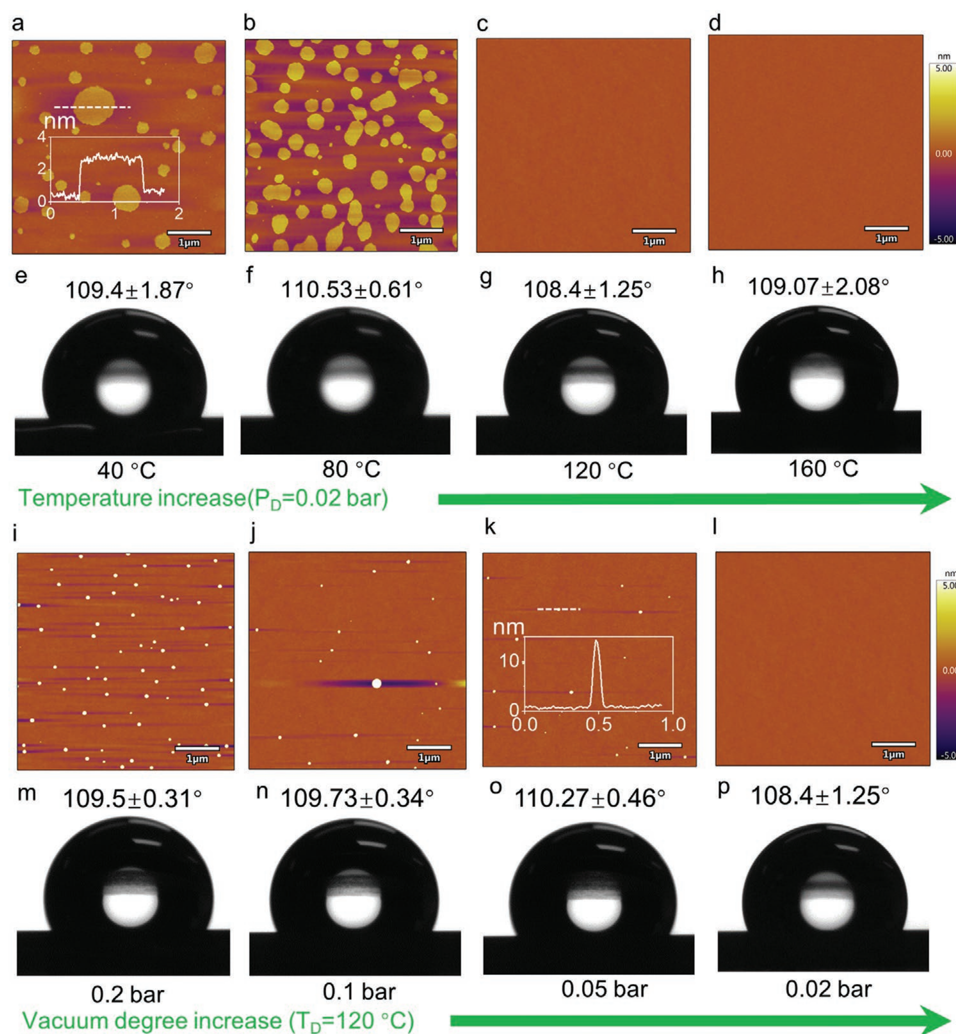

Figure 2. The surface functionalization study by varying the deposition parameters. a–d) Morphology of the FDTS films as a function of the T_D of a) 40, b) 80, c) 120, and d) 160 °C in an increasing succession (green arrow) under a constant P_D of 0.02 bar. In addition, the corresponding contact angles are measured, as shown in (e–h). The inset in (a) shows the height profile as indicated by the white dash line and the contact angle values are labeled. i–l) AFM image of FDTS growth as a function of the pressures, including i) 0.2, j) 0.1, k) 0.05, and l) 0.02 bar. The surface roughness of (l) is 0.09 nm. In (k), the inset depicts the outline along the white dash line. Herein, the T_D is maintained at 120 °C. The water contact angles are illustrated in (m–p). In the bottom of the figures, the green arrow represents the vacuum degree elevation sequence.

worth noting that the polar component is ≈3 mJ m^{-2}, indicating the weak polar characteristic and validating the utilization of Trouton's law as discussed in the previous vapor pressure derivation.[35] The deposition of the FDTS is further examined by X-ray photoelectron spectroscopy (XPS), together with the bare Si substrate. Three elements are measured, including C, F, and Cl. Other than the C—C peak located at 284.8 eV, the FDTS-modified Si substrate exhibits two extra C peaks at 290.9 and 293.3 eV, compared to the untreated Si substrate (Figure 3c). These two peaks are designated to the moieties of CF_2 and CF_3. In the meantime, an obvious F peak is observed, indicating the successful deposition of FDTS (Figure 3d). No Cl signals could be seen for both the FDTS-treated or non-treated Si substrates, divulging the hydrolysis reaction of FDTS during the surface functionalization process. The thickness of the defect-free FDTS is measured to be 1.31 nm by ellipsometer, which agrees well with the monolayer of the reported values.[26,39,40] Other than pure Si substrates, the functionalization process is usually applied to the SiO_2 surface to meliorate the interface properties between the organic semiconductor and dielectric layer. As such, we have performed the SAM growth on the Si substrate with 300 nm thermally grown SiO_2. The Si/SiO_2 is subjected to oxygen plasma treatment and functionalization with FDTS (Figure S3, Supporting Information). At each stage, the surface morphology characterizations manifest an almost identical surface roughness, imparting the perfect SAM deposition. Moreover, the low surface energy of 10.69 mJ m^{-2} confirms the successful FDTS deposition on the SiO_2 surface as well (Figure S4, Supporting Information). Furthermore, the large area scalability is accomplished with the 4-inch wafer as the functionalized substrate. All the AFM images scanned at different locations reveal even morphology, indicating the good scalability of the current deposition process (Figure 3f). The high-quality surface functionalization should lead to the high performance, stability,

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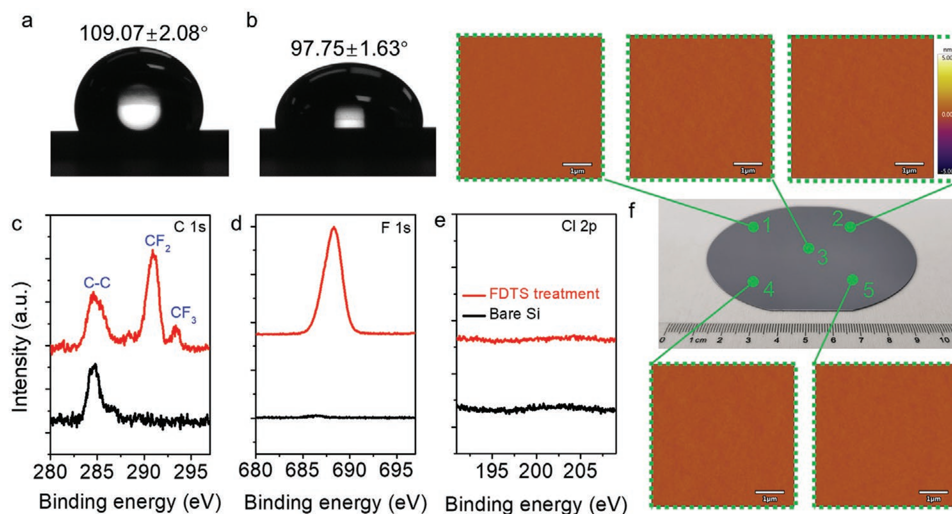

Figure 3. Characterization of the wafer-scale defect-free FDTS modified Si substrates. a,b) Contact angle measurement from a) water and b) diiodomethane for the surface energy determination. From these contact angle values shown, the surface energy is calculated to be 10.33 mJ m^{-2}. The dispersive term is 7.58 mJ m^{-2} and the polar term is 2.75 mJ m^{-2}. c–e) XPS characterization of the FDTS treated Si (red lines), together with the pure Si substrate (black lines) regarding the elements of c) C, d) F and e) Cl. In (c), the chemical bonding of C—C, CF_2, and CF_3 are labeled. f) AFM characterization of the wafer-scale FDTS growth. Different areas from 1 to 5 show uniform and smooth surface morphology.

and well repeatability of the organic electronic devices, and wafer-scale scalability sheds the light on the mass production of the large-area, highly integrated electronics.

The generality is verified by applying the growth conditions to the other two frequently used SAMs, including both OTS and PTS (**Figure 4**). Figure 4a depicts the molecular structure of OTS on the Si substrate. Under the deposition temperature of 120 °C and the deposition pressure of 0.2 bar, irregular spots are dispersive on the surface (Figure 4b). As discussed previously, the low degree of vacuum allows a large amount of moisture residing in the vessel and enhances the hydrolysis to form large aggregates. The quality of the OTS is greatly improved

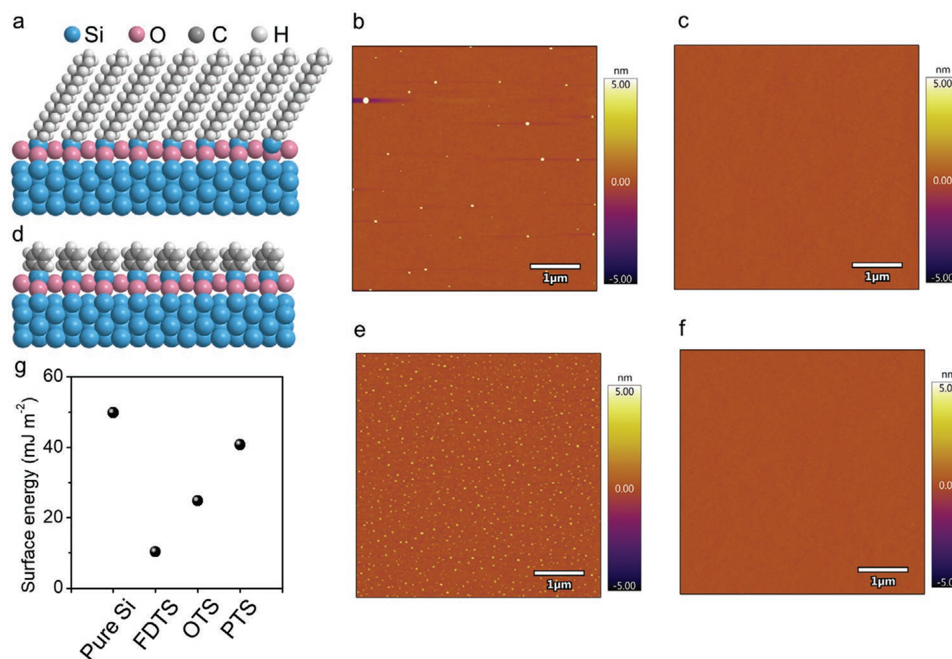

Figure 4. The generality of the processing conditions to frequently used trichlorosilanes. a) Molecular packing of OTS on Si substrate. The elements are labeled. b,c) AFM images of the OTS (b) with aggregates (processed at 120 °C and 0.2 bar) and (c) without aggregates (processed at 160 °C and 0.02 bar). d) Illustration of molecular packing of PTS on the Si substrate. e,f) Surface morphology of PTS SAM characterized by AFM, which is deposited at e) 120 °C and 0.2 bar and f) 160 °C and 0.02 bar. g) Surface energies of the pure Si substrate and the trichlorosilane treated substrates used in the current investigation.

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by reducing the P_D to 0.02 bar. Due to the high boiling point of OTS (Table S1, Supporting Information), herein, the processing temperature is increased to 160 °C to assist the evaporation. Figure 4c presents the surface morphology of OTS after the optimizations of the deposition parameters. Similarly, a high-quality PTS (Figure 4d) is obtained by optimizing the variables. The functionalization at a low degree of vacuum (0.2 bar) displays scattered dots (Figure 4e), while defect-free PTS SAM is realized with the increased degree vacuum of 0.02 bar (Figure 4f). The high-quality OTS and PTS SAMs are characterized based on the surface energy and the XPS analysis (Figures S5, S6, Supporting Information). The XPS results are similar for OTS and PTS with only a C peak detected, whereas different results are found for the surface energy. From the contact angle values using water and diiodomethane, the surface energies are assessed, showing the values of 24.49 and 40.7 mJ m^{-2} for OTS and PTS, respectively (Figure 4g). The defect-free functionalization by FDTS, OTS, and PTS shows a wide range of surface energy from ≈10 to 40 mJ m^{-2}, hence providing an outstanding approach for effective surface modification.

To explore the effect of high-quality interface on the OTFT performance, the SAMs were incorporated into the OTFT devices using DNTT as the semiconductor material (**Figure 5**a,b). The bottom-gate/top-contact (BG/TC) architecture

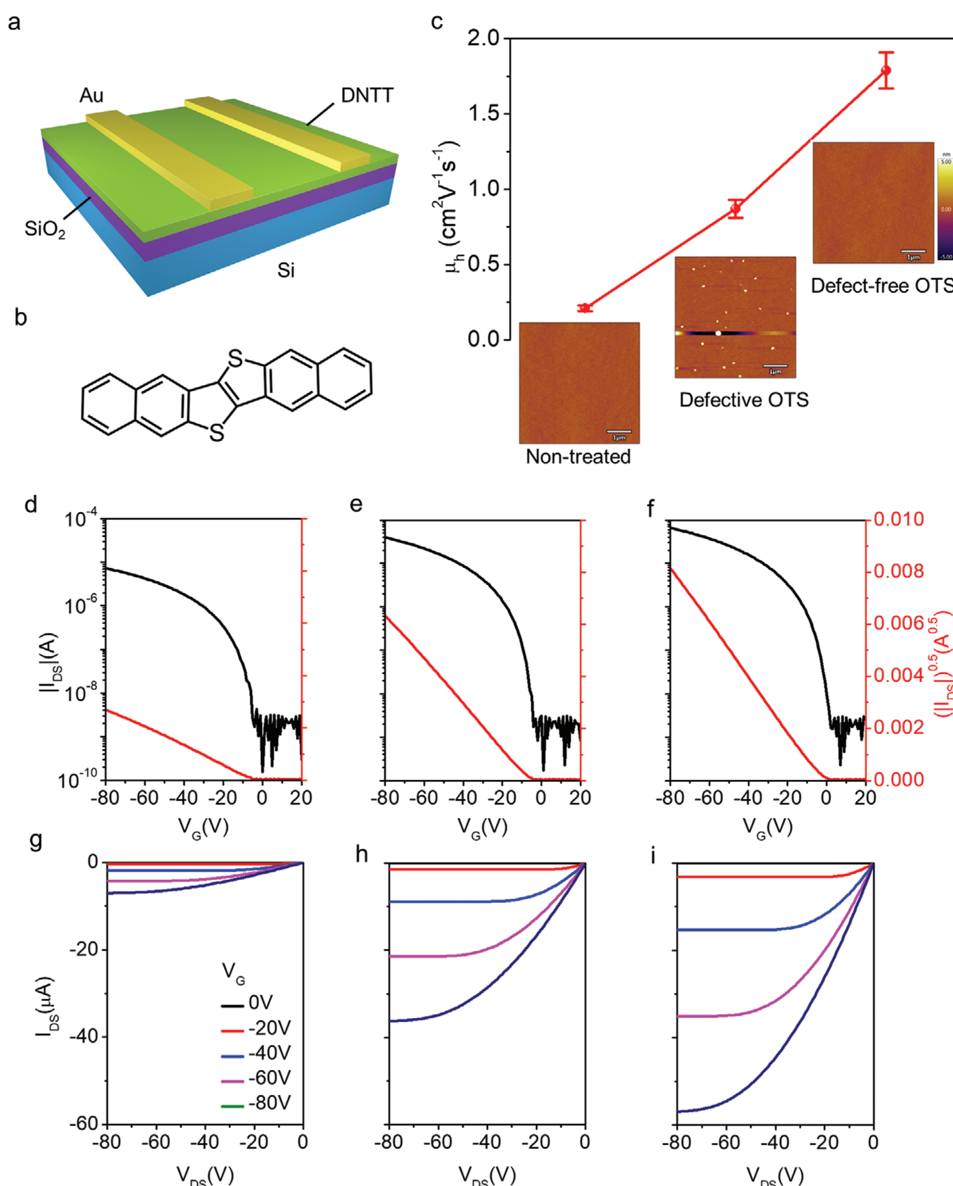

Figure 5. The application of defect-free OTS to the organic thin-film transistors. a) Schematic diagram of the staggered OTFT device with the semiconducting layer of DNTT. b) Molecular structure of DNTT. c) Carrier mobilities by optimizing the organic semiconductor-dielectric interface. Inset shows the AFM images of the interfaces, including (i) non-treated SiO_2, (ii) defective OTS treatment, and (iii) defect-free OTS treatment with a surface roughness of 0.2, 2.1, and 0.19 nm, respectively. d–f) Typical transfer curves from the device fabricated with (d) non-treated SiO_2, (e) defective OTS, and (f) defect-free OTS. Apart from the logarithm scale (black curves), the square root of the I_{DS} is plotted for carrier mobility extraction. The drain to source voltage (V_{DS}) used here is −80 V. g–i) Corresponding output curves to (d–f). The gate voltage (V_G) is swept from 0 to −80 V with a step of −20 V.

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is constructed by thermally evaporating a 40 nm organic semiconductor layer and 30 nm gold (Au) source/drain electrodes (Figure 5a). As defined by the shadow mask, the conduction channel has a width (W) of 249 µm and a length (L) of 218 µm, yielding a W/L ratio of ≈1.14. Three surface treatments are utilized prior to the active layer deposition, including i) non-treated, ii) defective OTS and iii) defect-free OTS and their surface morphologies are presented (inset of Figure 5c) with an R_q of 0.2, 2.1, and 0.19 nm, respectively. To eliminate the fringe current, the active layers were scratched along the Au electrodes.[41] The electrical characterizations of the OTFTs were then performed and the carrier mobilities were extracted, as shown in Figure 5c. With the functionalization of the defective OTS, the average hole mobility (μ_h) is drastically increased from 0.21 ± 0.02 cm^2 V^{-1} s^{-1} to 0.87 ± 0.06 cm^2 V^{-1} s^{-1}, albeit the surface is quite coarse. The mobility is further improved when the OTFTs are fabricated with the defect-free OTS SAM, yielding an average μ_h of 1.79 ± 0.12 cm^2 V^{-1} s^{-1}, which shows 2.06 times compared to the μ_h of the defective OTS-based devices. As the conduction channel is near the DNTT/OTS interface, the defect-free OTS favors the carrier flow, leading to higher current and hole mobility. Basically, the hole mobility is independent of the silane thickness provided the surface roughness maintains the same. The typical transfer and output curves are illustrated in Figure 5d–i. A distinctive difference is that the device without any treatment shows much low current values, which is attributed to the substantial surface traps, such as —OH groups presented in the non-treated SiO_2 surface.[6,42] Such interface effect has also been observed in the high-mobility organic semiconductor of 2,9-didecyldinaphtho(2,3-b:2′,3′-f)thieno(3,2-b)thiophene (C_{10}-DNTT) (Figures S7, S8, Supporting Information). The traps in the SiO_2 surface could be eliminated by the OTS treatment and thereby the drain current (I_{DS}) is significantly increased, validating the critical role of surface functionalization in the OTFTs. It is worthwhile to mention that the organic thin-film transistors fabricated from FDTS SAMs manifest larger drain currents and threshold voltage shifts (Figure S9, Supporting Information), which is attributed to the accumulation of holes in the conduction channel by SAMs with fluorine groups.[20]

3. Conclusion

In summary, the surface functionalization of FDTS is comprehensively studied by varying the vapor phase growing condition. It is confirmed that a high deposition temperature ($T_D \geq 120$ °C) is required to eliminate the defect on the surface of the SAM-modified substrate. Meanwhile, the high vacuum degree ($P_D \leq 0.02$ bar) is essential to reduce the moisture and remove the aggregation defects. The successful deposition of the FDTS layer on Si substrate is verified by XPS with a surface energy of 10.33 mJ m^{-2} and a thickness of 1.31 nm. It is appealing that the surface functionalization could be scaled up to 4-inch wafer scale. The generality of the growth condition is validated by applying the frequently used SAMs, including OTS and PTS. Finally, surface functionalization is employed in the fabrication of organic transistors. The devices with defect-free OTS show a high mobility of 1.79 ± 0.12 cm^2 V^{-1} s^{-1} using the DNTT active layer, which is 2.06 times compared to that achieved in the devices with defective OTS treatment. The current study offers a universal guideline for high-quality surface treatment, which favors the implementation of high-mobility OTFTs. In addition, the wafer-scale depositions have foreshadowed the large-area fabrication of organic electronic devices.

4. Experimental Section

Surface Functionalization and Characterization: The Si substrates without further cleaning were treated with oxygen plasma at 150 W for 5 min (PDC-MG). After the hydrophilic treatment, both the substrate and 100 µL FDTS (Aladdin) liquid were then placed into an aluminum foil-covered glass petri dish, which was then put into the vessel with the temperature of T_D immediately. The glass petri dish was utilized to reduce the contamination from the reaction vessel. Then, the vessel was pumped down to P_D and maintains the T_D and P_D for 10 min. After the reaction, the residual FDTS vapor was pumped out and the samples were taken out after the inflation. Different parameters were selected for the growth investigation, including i) T_D = 40, 80, 120, and 160 °C when P_D = 0.02 bar and ii) P_D = 0.2, 0.1, 0.05, and 0.02 bar when T_D = 120 °C. The thickness of FDTS was measured by an ellipsometer (TF-UVISEL). The refractive index of FDTS was 1.35 and the Cauchy dispersion model (A = 1.35, B = 0, C = 0) was utilized for the thickness determination for FDTS on the Si/SiO_2 (2.1 nm)/FDTS layer structure.[30,43] Besides, Si with 300 nm oxide was functionalized with FDTS. The application to OTS (J&K Scientific) and PTS (J&K Scientific) was carried out with100 μL of the liquids under two disparate conditions, comprising i) T_D = 120 °C and P_D = 0.2 bar and ii) T_D = 160 °C and P_D = 0.02 bar. Detailed determination of the processing parameters was discussed in the main text. The current study was conducted under relative humidity from 60% to 80%. Since the atmospheric moisture could influence the amount of water in the reaction vessel and the quality of the surface functionalization, fine-tuning over the deposition factors was required subject to the relative humidity.

The AFM images were scanned by the Asylum MFP-3D system in tapping mode and the contact angles were measured by the drop shape analyzer (KRÜSS). The surface energy was calculated by Owen–Wendt–Rabel–Kaelble model. XPS results were taken by an X-ray photoelectron spectrometer (Escalab Xi+) and analyzed by the software of Advantage.

Fabrication and Characterization of Organic Thin-Film Transistors: The OTFT with staggered bottom gate architecture was constructed on the SiO_2/Si. Three interfaces were integrated into the fabrication of the organic transistors, including non-treated, defective OTS (processed at T_D = 120 °C and P_D = 0.2 bar) and defect-free OTS (processed at T_D = 160 °C and P_D = 0.02 bar). Forty nanometers of DNTT/C_{10}-DNTT (Luminescence Technology Corp.) were thermally evaporated as the active layer with an evaporation rate of 0.3 Å s^{-1} and a substrate temperature of 60/80 °C. The top contact was realized by evaporating 30 nm Au on the organic layer through the shadow mask. The evaporation rate was 0.3 Å s^{-1} while the base pressure was 9×10^{-7} mbar. Both thermal evaporations were carried out in the glove box. After fabrication, the active layers were scratched by needles to reduce the fringe and gate leakage current. The electrical tests were performed by a parameter analyzer (Keithley 4200). The transfer characteristics were measured at V_D = –80 V and the μ_h was determined from the following equation:

$$I_{DS} = \frac{\mu_h C_i}{2} \frac{W}{L} (V_G - V_{TH})^2 \tag{6}$$

where the areal capacitance C_i is 11 nF cm^{-2} for 300 nm SiO_2, W/L is 1.14 and V_{TH} is the threshold voltage. In addition, the output curves were tested by sweeping V_{DS} while changing the V_G from 0 to –80 V with the step of –20 V.

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Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

organic transistors, self-assembled monolayers, surface functionalization

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