

# A study of various oxide/silicon interfaces by Ar<sup>+</sup> backsurface bombardment

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(Received 8 October 1998; accepted for publication 5 November 1998)

A low-energy (550 eV) argon beam is used to bombard the backsides of 6 kinds of metal-oxide-semiconductor capacitors, and the resulting effects on their interface characteristics are then investigated. The gate oxide of these capacitors includes thermal oxide, trichloroethylene (TCE) oxide, NH<sub>3</sub>-nitrided oxide, reoxidized-nitrided oxide, rapid-thermal-nitrided oxide, and N<sub>2</sub>O-nitrided oxide. Measurements show that for bombardment times up to 45 min the interface-state density of all the devices, in general, decreases with increasing bombardment time/dose, and the midgap energy at the silicon surface tends to rise. Moreover, the bombardment is more effective in reducing acceptor-type than donor-type interface states. On the other hand, the change of fixed-charge density is more complex. For TCE, N<sub>2</sub>O-nitrided and reoxidized-nitrided oxides, fixed-charge density decreases initially with increasing bombardment time, but then increases, while the trend is reversed for the other gate oxides. A model with stress compensation and weak bond breaking is suggested to explain the results. © 1999 American Institute of Physics.

[S0021-8979(99)02004-6]

## I. INTRODUCTION

In the development of ultra-large-scale integration, the effects of interface characteristics of metal-oxide-semiconductor (MOS) structure on the mobility of inversion-layer charge carriers are still important issues.<sup>1-3</sup> It is well known that the lattice-damaged layer induced by high-energy (>10 keV) ion implantation with subsequent high-temperature (>800 °C) and long-time (>1 h) annealing can effectively getter crystal defects, as well as metal impurities in silicon wafers,<sup>4-7</sup> which can then be used to make better devices. Recently, low-energy (550 eV) argon-ion bombardment on the device backside was used to improve the characteristics of *n*-MOS devices.<sup>8,9</sup> In this work further investigation was carried out for six kinds of MOS capacitors with different gate oxides. The changes of their interface-state and fixed-charge densities, as well as the midgap energy at the silicon surface with bombardment time were characterized and a model including stress compensation and weak-bond breaking was proposed to explain the results.

## II. EXPERIMENT

The MOS capacitors (100×100 μm<sup>2</sup>) used in this work were fabricated on *p*-type (100)-oriented silicon wafers (6–8 Ω cm) using conventional *n*<sup>+</sup>-polysilicon-gate self-aligned MOS technology. A 21-nm-thick oxide was thermally grown by argon-diluted dry oxidation at 950 °C (denoted as OX sample). Some of the samples were nitrided in pure NH<sub>3</sub> either by rapid thermal annealing at 1200 °C for 1 min or by

furnace annealing at 1000 °C for 60 min (denoted as RTN and NO samples respectively), with part of NO samples then reoxidized in O<sub>2</sub> for 30 min (denoted as RON sample). Moreover, gate oxides were also thermally grown at 1000 °C in O<sub>2</sub> with trichloroethylene (denoted as TCE sample) for suppressing oxide defects and at 1050 °C in pure N<sub>2</sub>O (denoted as N<sub>2</sub>O sample) to about the same thickness, 24 and 22 nm, respectively. After completing the top electrodes of the MOS capacitors, the wafers were put into a closed chamber and a low-energy (550 eV) Ar<sup>+</sup> beam with 0.5 mA/cm<sup>2</sup> intensity was used to bombard their backsides under a vacuum of 3.2 mPa at room temperature. Four different bombardment times (0, 15, 30, 45 min) were performed and the corresponding bombardment dose was 0, 2.79, 5.58, and 8.37×10<sup>18</sup> cm<sup>-2</sup> respectively. Finally, a layer of aluminum was evaporated on the backs of the wafers and then the devices were annealed in nitrogen at 450 °C for 20 min. Interface characteristics of the devices were determined by high-frequency and quasi-static capacitance-voltage (*C*-*V*) techniques.

## III. RESULTS AND DISCUSSIONS

Figure 1 shows the interface-state density  $D_{it}$  (at midgap) for the six kinds of MOS capacitors versus bombardment time, with a typical curve of  $D_{it}$  versus the energy in the silicon bandgap for RTN sample illustrated in Fig. 2. Among all the nonbombarded oxides, the N<sub>2</sub>O-grown oxide has the highest  $D_{it}$  because it has an initial accelerated growth phase before the linear growth region, which can generate lots of defects.<sup>10,11</sup> Moreover, it is seen that, in general, the longer the bombardment time, the lower is  $D_{it}$  for all

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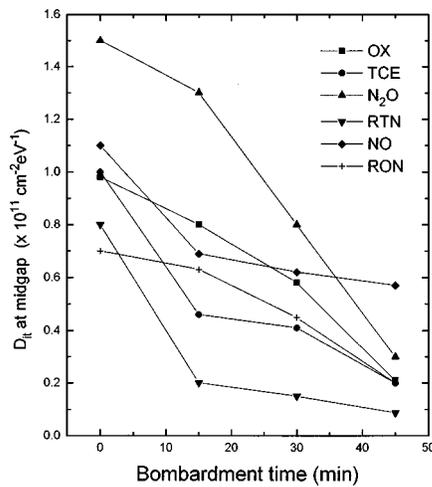


FIG. 1. Interface-state density vs bombardment time for MOS capacitors with six different gate oxides.

the devices. The fixed-charge density  $Q_f$  of all the samples versus bombardment time is depicted in Fig. 3, together with typical high-frequency and quasistatic  $C-V$  curves for RTN sample given in Fig. 4. Relatively high  $Q_f$  in  $N_2O$ , NO, and RON samples is related to the heavy nitridation of their gate oxides, which significantly roughens their oxide/Si interfaces. Also, the results indicate that the change of  $Q_f$  with bombardment time presents a turnaround behavior. For OX, NO, and RTN samples,  $Q_f$  increases at the beginning and then decreases with increasing bombardment time, while the change of  $Q_f$  for the other samples has an opposite trend.

In order to explain these observations, a model of stress compensation and weak-bond breaking is suggested as follows. After the  $Ar^+$  bombardment, a lattice-damaged layer is produced at the backsurface of the devices and gives rise to a mechanical stress in the vicinity of the oxide/Si interface. This stress can partially compensate the stress created by thermal processing of the gate oxide, polysilicon deposition, aluminum evaporation, lattice mismatching, as well as the original stress in the wafer. Therefore, defects associated with the stress decrease and hence, both  $D_{it}$  and  $Q_f$  decrease. Of course, if overcompensation of stress happens due to

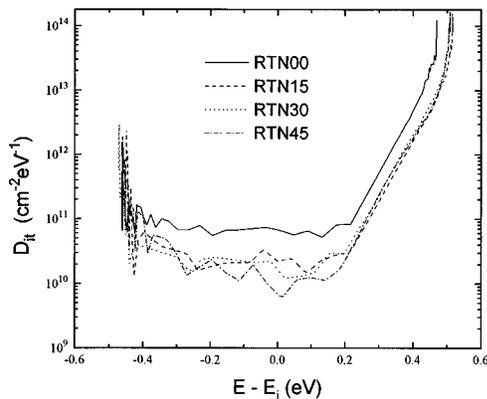


FIG. 2. Interface-state density vs the energy in band gap for a MOS capacitor with RTN gate oxide ( $E_i$  is the intrinsic Fermi energy of bulk silicon). The number after RTN indicates the bombardment time in minutes.

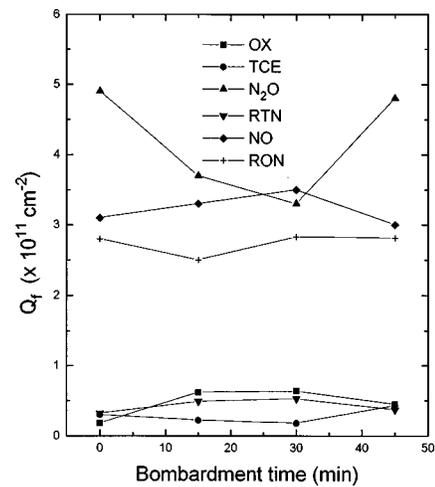


FIG. 3. Fixed-charge density vs bombardment time for all MOS capacitors.

higher bombardment energy and/or longer bombardment time, new defects could be generated and hence,  $D_{it}$  and  $Q_f$  become larger. The changes of  $D_{it}$  for RTN and OX samples are in agreement with previous results.<sup>8,9</sup> However, NO sample with long bombardment time displays opposite behavior,<sup>8</sup> which likely has higher original stress than the previous sample grown at a higher temperature of  $1000^\circ C$ <sup>12,13</sup> and hence, stress overcompensation does not occur yet to increase  $D_{it}$  again even after 45 min bombardment. On the other hand, weak Si-O and/or Si-N bonds not only present at the oxide/Si interface,<sup>14,15</sup> but could also occur in the gate oxide near the interface due to the existence of some microscopic unoxidized silicon regions in the oxide.<sup>16</sup> The breaking of these weak bonds induced by the bombardment could give rise to more dangling bonds at the interface and in the oxide and hence, higher  $D_{it}$  and  $Q_f$ . On the contrary, the oxygen and/or nitrogen released from the weak bond breaking can diffuse from the oxide to the interface and help to reduce  $D_{it}$  by combining with the dangling bonds there. Therefore, if stress compensation plays a bigger role than weak bond breaking,  $D_{it}$  and  $Q_f$  get smaller after the bombardment. But for the case with weak bond breaking as the dominant mechanism and/or the presence of stress overcom-

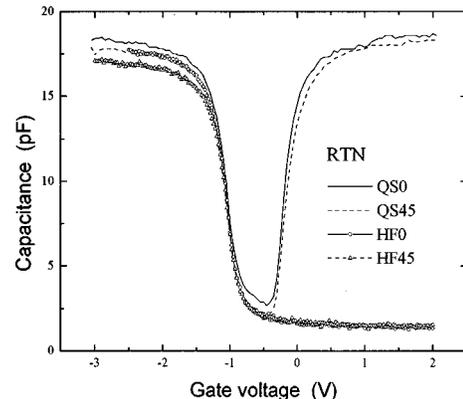


FIG. 4. High-frequency and quasistatic  $C-V$  curves for two MOS capacitors with RTN gate oxide, one before and the other after 45 min bombardment.

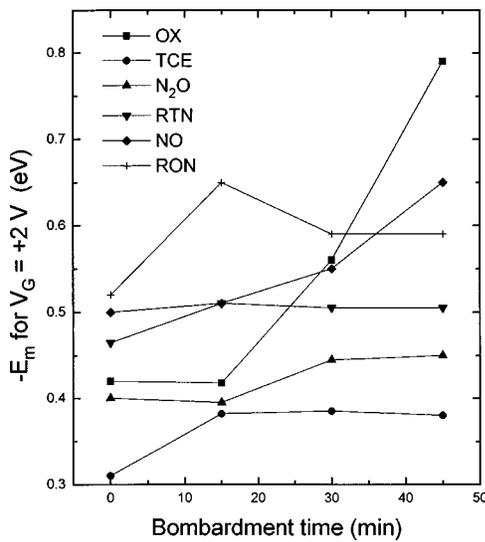


FIG. 5. Midgap energy at silicon surface vs bombardment time for all MOS capacitors with  $V_G = +2$  V.

compensation,  $D_{it}$  and  $Q_f$  could increase. Therefore, the changes of  $D_{it}$  and  $Q_f$  heavily depend on the bombardment energy and time, as well as the original stress, defect density, and bond energy in the devices.

The  $D_{it}$  decrease of all the samples here after the bombardment is likely due to the dominance of stress compensation at the interface. Moreover, the oxygen and/or nitrogen created by bombardment-induced weak bond breaking in the oxide can diffuse to the interface, reducing the dangling bonds there and hence,  $D_{it}$  although a corresponding  $Q_f$  increase is possible. For example, in OX, NO, and RTN samples, the slight  $Q_f$  increase and then decrease with bombardment time are likely due to weak bond breaking in the oxide and stress compensation, respectively. On the other hand, for TCE, N<sub>2</sub>O, and RON samples,  $Q_f$  decreases initially with bombardment time, possibly because the stronger Si-Cl or Si-N bonds at their interfaces and in their oxides

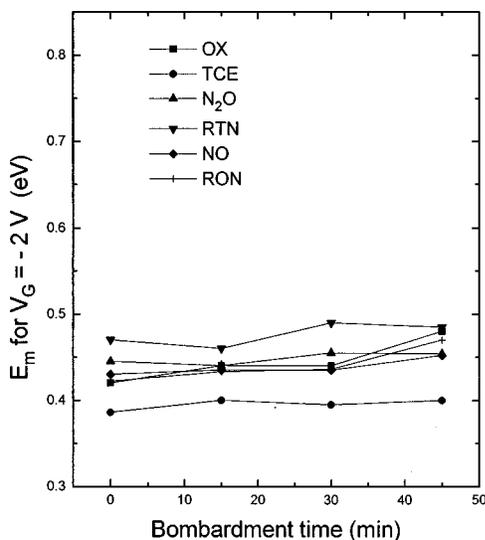


FIG. 6. Midgap energy at silicon surface vs bombardment time for all MOS capacitors with  $V_G = -2$  V.

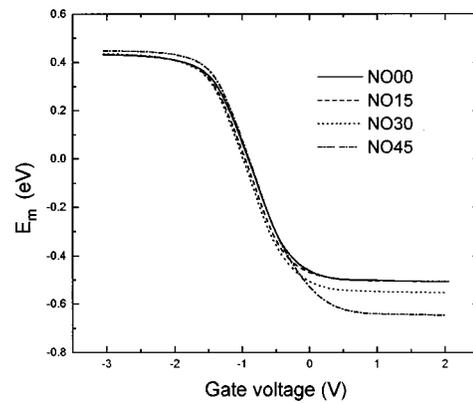


FIG. 7. Midgap energy at silicon surface vs gate voltage for a MOS capacitor with NO gate oxide.

cannot be easily broken due to the special treatments on the oxides and hence, stress compensation should be the major factor. It is interesting to note that the nitrated oxides of NO and RTN samples are not so strong after all, possibly due to the hydrogen species left in the oxide during NH<sub>3</sub> nitridation, which can disrupt the Si-O bonds and thus create weaker Si-H bonds.

For all the devices, their midgap energies ( $E_m$ ) at the silicon surface deviated from the flat-band condition under a gate voltage  $V_G$  of  $+2$  and  $-2$  V versus bombardment time are respectively presented in Fig. 5 and 6, and a typical  $E_m$  vs  $V_G$  for NO sample is given in Fig. 7. From  $E_m - V_G$  plots,  $E_m$  of all 6 nonbombarded devices with  $V_G = 0$  are found to lie within 0.25–0.45 eV ( $-0.5$ – $-1$  V for the flat-band voltage), which is due to the positive  $Q_f$  giving rise to a bending down of the energy band. The  $E_m$  increase after the bombardment should be related to the  $D_{it}$  decrease, which weakens the shielding effect of interface-state charge against electric field and gives rise to more severe band bending under both  $+V_G$  and  $-V_G$  conditions. The changes of  $E_m$  with bombardment time in Figs. 5 and 6 are not quite similar to that of  $D_{it}$  (see Fig. 1), possibly due to the fact that  $E_m$  is also related to the dopant concentration at the silicon surface which remains unchanged after the bombardment. Furthermore, the  $E_m$  increase is larger under  $+V_G$  than  $-V_G$  for all the devices. This implies that the bombardment is more effective in eliminating acceptor-type than donor-type interface states, because the acceptor states are close to the top of the band gap and are charged with electrons due to the bending down of the energy bands under  $+V_G$ .

#### IV. CONCLUSION

In conclusion, low-energy (550 eV) argon bombardment at the back of MOS devices with various gate oxides can lower their interface-state density and raise the midgap energy of the silicon surface for bombardment times up to 45 min. The corresponding change of fixed-charge density with bombardment time can first increase and then decrease, or vice versa. All these behaviors could be explained by the competing effects of stress compensation and weak bond breaking.

## ACKNOWLEDGMENTS

The authors would like to thank C. L. Chan and H. H. Ng for their technical support in the microelectronics laboratory. This work was partially supported by RGC Research Grant, Hong Kong, and the CRCG Grant, The University of Hong Kong, Hong Kong.

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