Standard Cell Layout With Regular Contact Placement

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***Abstract*—The practicability and methodology of applying regularly placed contacts on layout design of standard cells are studied. The regular placement enables more effective use of resolution enhancement technologies, which in turn allows for a reduction of critical dimensions. Although placing contacts on a grid adds restrictions during cell layout, overall circuit area can be made smaller by a careful selection of the grid pitch, allowing slight contact offset, applying double exposure, and shrinking the minimum size and pitch. The contact level of 250 nm standard cells was shrunk by 10%, resulting in an area change ranging from −20% to +25% with an average decrease of 5% for the 84 cells studied. The areas of two circuits, a finite-impulse-response (FIR) filter and an add-compare-select (ACS) unit in the Viterbi decoder, decrease by 4% and 2%, respectively.**

***Index Terms*—Double exposure, fabrication-friendly layout, low k_1 lithography, regularly placed contact, RETs, standard cells.**

I. Introduction

THE SUSTAINED demand for high speed integrated circuits (ICs) results in the continuous increase of transistor density and decrease of the feature size in the past three decades. The critical dimension (CD)—the minimum feature size that can be defined by optical lithography—has been reduced to 130 nm at the end of the last century. As a function of three parameters, the CD can be expressed as [1]:

$$\mathrm{CD} = k_1 \frac{\lambda}{NA}. \tag{1}$$

The CD is proportional to the wavelength of the exposure light λ and the process-related factor k_1, and decreases with increasing numerical aperture (NA) of the projection system. Smaller dimensions can be printed by decreasing the wavelength, increasing the numerical aperture and reducing k_1, or any combination thereof. The ultimate resolution can only be achieved by all three measures.

Over the past three decades, the developments of optical lithography have been successful in reducing the λ from 436 nm in the 1970s to 193 nm in 1999, and increasing the NA to the current value of about 0.85 [2]. However, these improvements alone are insufficient to reduce the feature size exponentially as projected by Moore's law [3].

As the third parameter in (1) and the measure of lithography aggressiveness, the k_1 factor is the only parameter that can be controlled by lithographers for a given exposure system. Its theoretical lower limit is 0.25 [2]. Over the past two decades, the k_1 factor has been reduced by over 0.1 every five years [4]. Because image quality degrades noticeably when k_1 falls below 0.75, resolution enhancement techniques (RETs) such as modified illumination [5], optical proximity correction (OPC) [6], and phase-shifting masks (PSMs) [7] have been used to improve image quality for low-k_1 lithography. These RETs have been successful in reducing the k_1 factor to about 0.5 [8].

However, with k_1 approaching its limit, the additional improvement requires closer communications between the technology and design communities. By considering circuit manufacturability in layout design, it is expected that the k_1 factor can be further reduced by fabrication-friendly layout in which the circuit pattern configurations are limited to facilitate lithography optimization. As an important example, optimization of illumination is essential at low-k_1 imaging for a successful lithography. Image quality depends not only on the size and shape of a pattern, but also on its environment [9]. As one of the most difficult parts in a lithography process, the contact level has the biggest cost weighting and is one of the bottlenecks for circuit area reduction. However, optimization of the illumination configuration is almost impossible for randomly placed contacts because of the simultaneous existence of dense and sparse contacts. No illumination scheme allows optimal imaging of both dense and sparse contacts [9]. By limiting the circuit pattern configuration, a regular contact placement allows lithography optimization, which in turn leads to a shrinkage of the minimum contact pitch and size without the loss of the process latitude [10].

In fact, many advanced lithographic approaches have been proposed over the last few years that employ regular contact placement, pushing the k_1 to about its minimum value [10]–[15]. As an example, Fig. 1 shows one possible approach of the imaging process for regularly placed (fabrication-friendly) contacts [13]. Randomly placed (traditional) contacts are plotted also as a reference. In the randomly placed layout, the layout [Fig. 1(a)] translates to a mask with the same features [Fig. 1(b)], which are imaged onto the die [Fig. 1(c)]. In the regularly placed layout, contacts are snapped to grid points [Fig. 1(d)]. Assist contacts are then placed at grid points that do not have a contact [Fig. 1(e)]. The assist contacts are sized such that they do not print onto the die but nevertheless create a mask spectrum that allows the illumination to be optimized [Fig. 1(f)].

On the other hand, from a layout designer point of view, the regular contact placement imposes extra restriction on layout compaction. Although the contacts can be designed smaller

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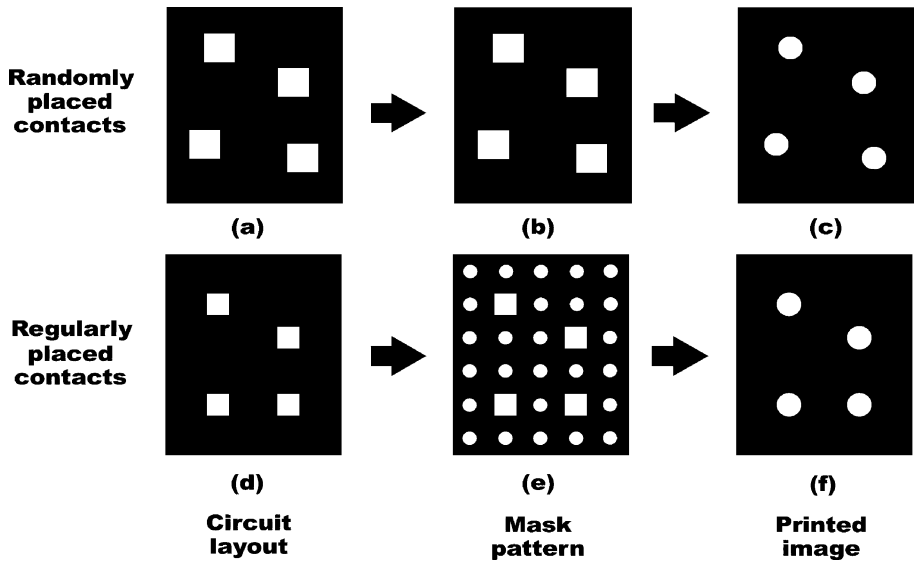

Fig. 1. Imaging process for randomly placed contacts and one scenario for regularly placed contacts.

and packed closer [Fig. 1(d)], the regular placement may be so restrictive on layout compaction that the final circuit area increases unacceptably. This can be a fatal disadvantage for applications of the regularly placed layout. It is therefore critical to seek a fine balance between the lithographic optimization and layout compaction. The effects of regular contact placement on layout design should be carefully studied to estimate the practicability of the regular-layout-based lithography approaches.

This paper examines the practicability and methodology of applying regularly placed contacts on layout design. A 250 nm standard cell library is used in this study to demonstrate the effects of the regularly placed contacts on cell area. Section II and III discusses the standard cells layout methodology with regularly placed contacts. Regular contact placement allows a novel application of the double exposure technique [16], which is necessary for the application of the regularly placed layout on standard cell. Section IV describes this novel double exposure technique. The considerations for physical design are discussed in Section V. Eighty-four standard cells are redesigned using the regularly placed contacts. The new standard cells are then used to design two circuits, a finite impulse response (FIR) filter and an add-compare-select (ACS) unit in the Viterbi decoder, to study the effects on overall circuit area. The results are given in Section VI.

A preliminary version of this work has appeared in *Microlithography World* [17].

II. ASICs and Regular Contact Placement

The effects of regular contact placement on circuit area vary with different layout structures. In this study, we examine the application of regularly placed contacts on standard cells—the elementary building blocks of application-specific integrated circuits (ASICs).

A cell-based structure is an important structure for ASIC design. A cell-based ASIC die typically consists of three types of cells: I/O cells, mega cells and standard cells (Fig. 2). I/O cells are cells laid on the periphery of the die as connection points to outside circuitry. Standard cells are pre-designed micro-logic structures providing basic logic functions (AND gates, OR gates, and flip-flops, for example). Mega cells are typically large predesigned structures such as memory, or microcontrollers used in combination with standard cells. Standard cell circuits also exist in designs such as microprocessors and their peripherals.

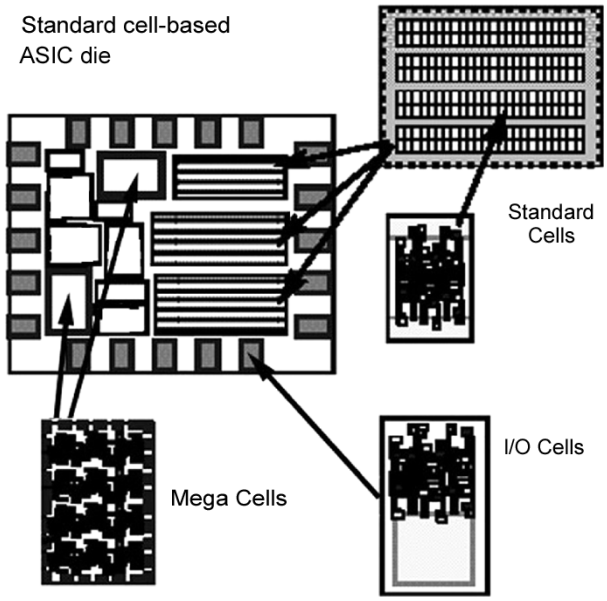

Fig. 2. Cell-based ASIC die typically consists of three types of cells: I/O cells, mega cells (memory or microcontrollers, etc.), and standard cells.

As the two core blocks of cell-based ASICs, memories (mostly SRAMs) and standard cells have different layout structures, and therefore should be studied separately when apply the fabrication-friendly layout design. We focus on the application of regularly placed contacts on standard cell layout in this paper, and investigate the practicability and proper grid pitches for standard cells according to their layout structure. Similar methods can be used for memories, which is outside the scope of this study. Furthermore, the regular placement is

only considered a local constraint. As the optical interaction range is on the order of $(1.2/\sigma)(\lambda/NA)$, where σ is the partial coherence factor of the illumination, layout blocks that are farther apart than the optical interaction range, such as blocks of memories and standard cells, do not need to be on the same grid. It also possible to have randomly placed and regularly placed contacts on one mask at the same time.

A 250-nm standard cell library is used in this study to demonstrate the effects of the regular contacts placement on cell area. The layout strategy, including the determination of grid pitch and offset, is detailed in the next section.

III. Standard Cell Layout

A. Grid Pitches

Fig. 3 shows the structure of a typical standard cell. Each standard cell in a library is rectangular with a fixed height but variable width. Contacts are the connections between different layers inside a cell.

The lower limit of the grid pitch is naturally the minimum pitch allowed by the design rules. The minimum contact pitch of the technology under study is 600 nm. If we assume that the pitch can be shrunk by 10% because of regular contacts placement, 540 nm can be used as the improved minimum contact pitch and the minimum grid pitch in this study.

However, the minimum allowable pitch is not necessarily the grid pitch. The grid pitch should rather be the most common pitch in the layout or an integral fraction of that pitch to minimize the number of affected contacts. Distributions of contact pitches in standard cells were collected in both the height (vertical) and width (horizontal) directions. Plotted in Fig. 4 are four representative pitch distributions of combinational and sequential cells. Fig. 4(a) and Fig. 4(b) show the vertical and horizontal pitch distributions of combinational cells such as NAND gates and multiplexers. Fig. 4(c) and Fig. 4(d) are the vertical and horizontal pitch distributions of sequential cells such as flip-flops. Because the outputs of combinational cells are functions of the inputs only, the layouts of combinational cells are typically simpler and more regular than that of sequential cells, which are circuit elements with memory. The consequence is that the pitch distributions of combinational cells [Fig. 4(a) and Fig. 4(b)] show sharp peaks while the peaks of sequential cells [Fig. 4(d)] are not as distinct. The difference among distributions indicates that the pitches in the vertical and the horizontal directions should be chosen separately according to the layout characteristics in these directions.

1) Vertical (y axis) Grid Pitch: For combinational cells, the strongest peak in the vertical pitch distribution is at the minimum at 600 nm. This peak arises from redundant contacts (covered by the same metal-1 line) used for wide MOSFETs to achieve better yield, as shown in Fig. 5.

For multistage sequential cells, however, MOSFETs in stages other than the output stage are designed to be small to reduce parasitic capacitance. Because there is only one source or drain contact in each narrow MOSFET, most contacts are covered by different metal-1 lines. These contacts can be connections between source or drain to metal-1, poly-silicon or gate to metal-1, or power supply paths to substrate or wells. Six main scenarios

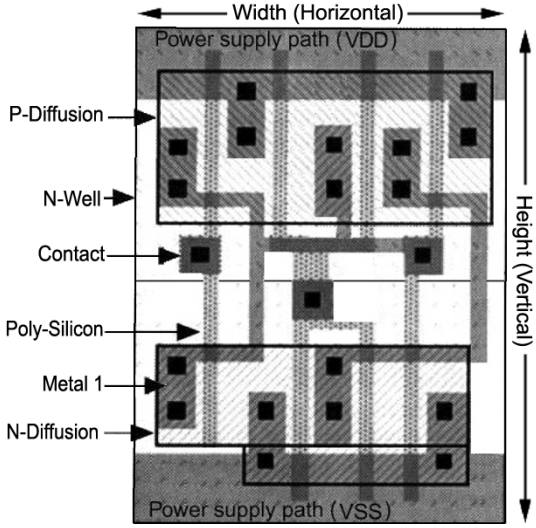

Fig. 3. Structure of a typical standard cell is composed of six layers: N-well, N-diffusion, P-diffusion, poly-silicon, contact and metal-1. The first four layers are primarily used to construct the MOSFETs while the latter three layers are used for intracell connections.

of the placement of two neighboring contacts in the vertical direction are listed in Fig. 6. Since the contacts connect different layers and the minimum spacings of these layers are different, the pitch distribution is more uniform [Fig. 4(c)].

It appears reasonable that the pitch of the metal-1 track, 640 nm, can be chosen as the vertical grid pitch so that the height of standard cells can be made an integer multiple of the metal-1 track. This pitch can also be used in combinational cells by reducing the number of redundant contacts in multicontact scenarios. The typical height of standard cells corresponds to 10 metal-1 tracks, giving 10 grid points in the height direction.

Yet ten points are often inadequate for regular contacts placement. To be consistent with the metal-1 pitch and to provide more grid points in the y direction, it is desirable to use 320 nm—half of 640 nm—as the vertical grid pitch. However, even as we assume a 10% shrinkage by the regular contacts placement, the improved pitch resolution for the normal process is still 540 nm, well above the value desired. Thus a lithographic innovation would be needed to use the 320 nm grid directly. We introduce a double exposure method in Section IV to address this issue.

2) Horizontal (x axis) Grid Pitch: The horizontal pitch distribution for both combinational [Fig. 4(b)] and sequential [Fig. 4(d)] cells show peaks near 1000 nm. This is because the MOSFETs are mostly placed in series in the horizontal direction with contacts placed in both the source and drain regions, as shown in Fig. 7. For a MOSFET with contacts connected to both source and drain, the pitch between two contacts can be calculated by the equation below:

$$P_{c\to c} = 2 \cdot S_{c\to g} + L_g + W_c \tag{2}$$

where $P_{c\to c}$ is the contacted pitch of a MOSFET, $S_{c\to g}$ is the space between the contact and the gate, L_g is the length of the gate, and W_c is the size of the contact. For combinatorial cells, the two dominant peaks in the horizontal pitch distribution are 980 nm and 1100 nm [Fig. 4(b)]. These peaks correspond to the

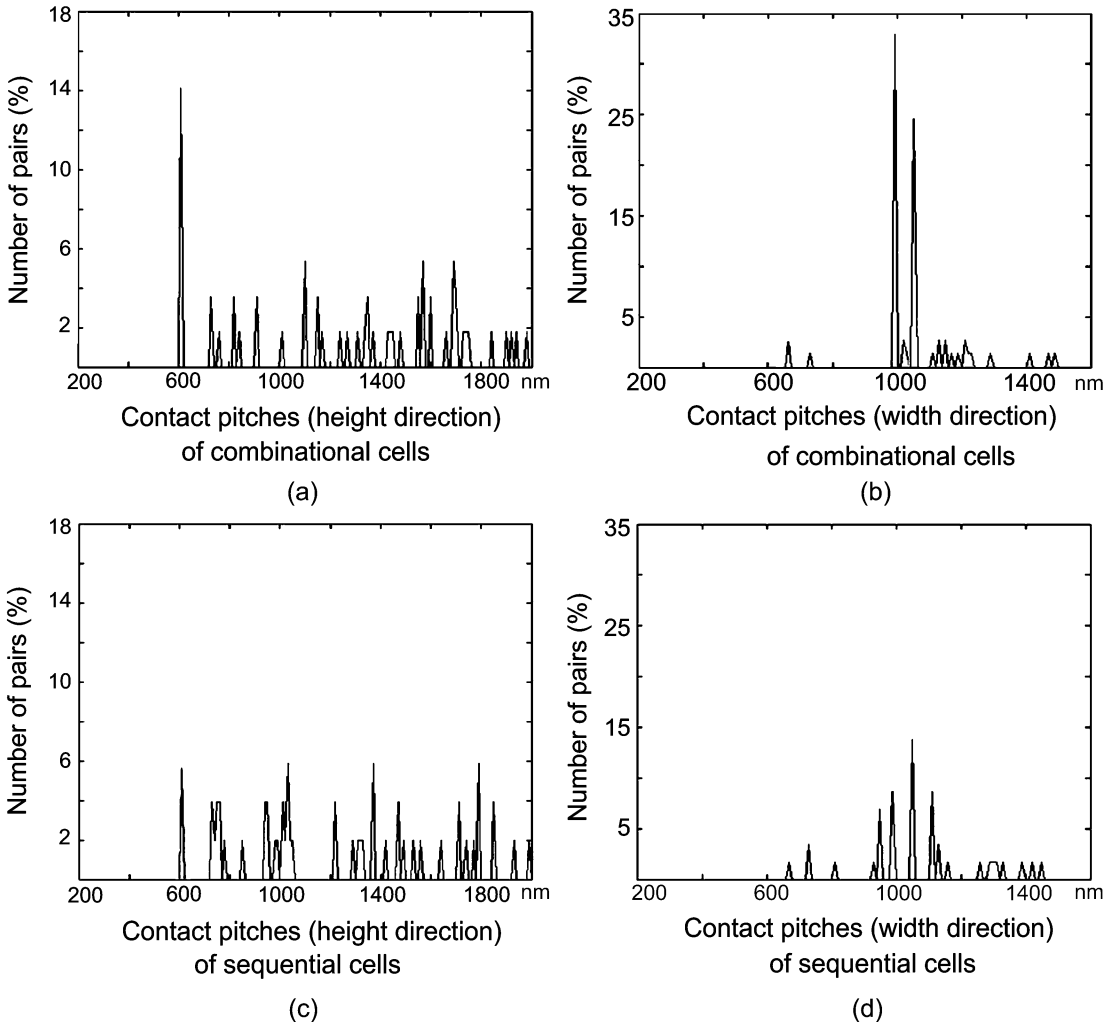

Fig. 4. Representative pitch distributions of standard cells. (a) and (b) are for combinational cells; (c) and (d) are for sequential cells.

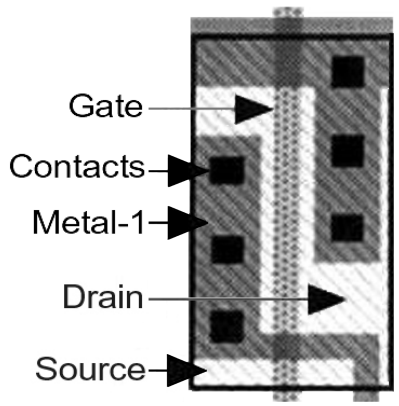

Fig. 5. Redundant contacts are used for wide MOSFETs to achieve better yield.

contacted pitch of narrow and wide MOSFETs, which differ in the space between the contact and the gate. For the MOSFETs with the gate narrower than the active region around the contact, the minimum space between the contacts and the gate is larger than that of other MOSFETs (Fig. 8), which leads to the different contacted pitches of MOSFETs.

For a realistic grid design these design rules need to be modified to allow the two peaks to coalesce into one. One approach is to increase the width of some MOSFETs such that the peak corresponding to narrow MOSFETs is eliminated. The contacted pitch of wide MOSFETs—reduced from 980 to 950 nm after considering the 10% contact size shrink—can then be used to define the horizontal grid pitch.

In addition to active contacts, there are also gate contacts which connect gates to metal-1 lines. These are often placed in the middle of the source and drain contacts in the horizontal direction (Fig. 8). If the pitch between source and drain contacts is used as the grid pitch, the gate contacts must be moved to align with the source or drain contacts. Cell area then increases significantly when more than two MOSFETs are connected in series. Fig. 9 shows two scenarios of snapping contacts of series MOSFETs connection in Fig. 7 to the grid. The grid pitch is assumed to be the pitch of source and drain contacts. Because of the gate extension of the previous MOSFET, the gate contact of the following MOSFET has to be moved apart to satisfy the minimum spacing requirement of poly-silicon layer. Regardless of displacement in the height direction [Fig. 9(a)] or in the width direction [Fig. 9(b)], extra space is needed to snap the gate contacts on grid. Therefore, it is desirable to use the pitch between

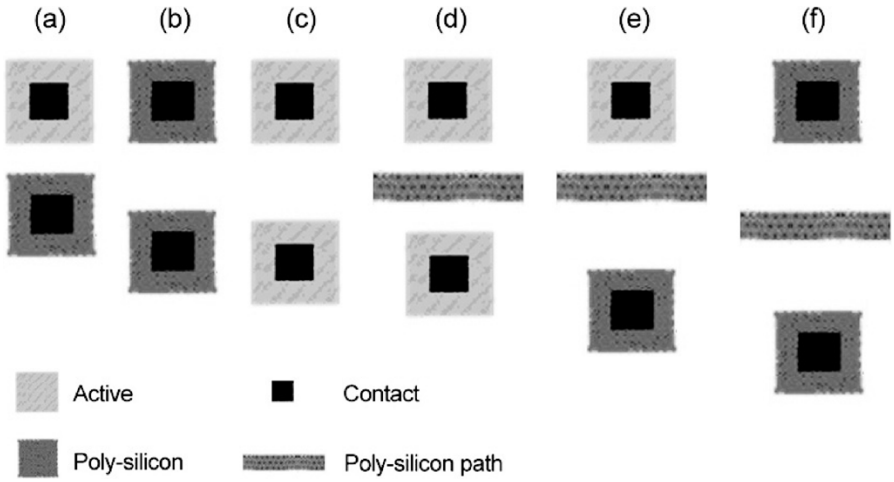

Fig. 6. Six main scenarios of the placement of two neighboring contacts in the vertical direction. The space between two contacts in each scenario is proportional to the minimum space between two contacts in the real layout.

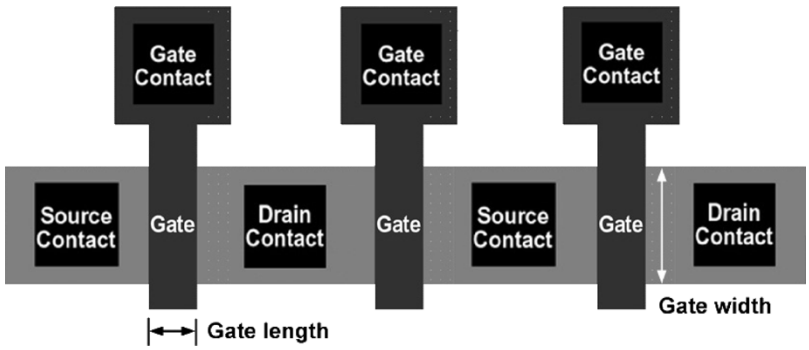

Fig. 7. MOSFETs are mostly placed in series in the horizontal direction with contacts placed in both the source and drain regions.

the gate and source contacts (475 nm)—half of that between the source and drain contacts but still <540 nm—as the horizontal grid pitch. We note that again this is smaller than the improved pitch resolution at 540 nm.

B. Offset

From a lithography point of view, snapping all contacts on grid is not an absolute requirement. A slight offset of contacts from grid point can be allowed for illumination optimization. The extra flexibility offered by the offset results in a reduction on the final cell area. It is also useful to note that the contact pitch distribution is much more regular in the horizontal direction than in the vertical direction. The space between the neighboring source and drain contacts in the horizontal direction is fixed at 950 nm or 1425 nm. Therefore, offset is more useful in the vertical direction.

As an example, after snapping the contacts on the grid, the spacing between two neighboring contacts in the vertical direction should be at a multiple of 320 nm. However, after reducing the contact size to 90%, the pitch between the neighboring contacts in the fifth scenario of Fig. 6 [Fig. 6(e)] is 1290 nm, just 10 nm larger than 1280 nm (four times of 320 nm). Without an offset, the space need to be enlarged by 24% to 1600 nm (five times of 320 nm) when we snap the contacts on the grid. Because the height of standard cell is kept unchanged, there may not be enough room to place the contacts in one column, although they were in the same column originally. An extra column of grid points is needed to place these contacts. However, as shown in Fig. 10, if a 10 nm offset of contact from grid point is allowed, it can be avoid to increase the space between the two contacts in Fig. 6(e) to five grid points (1600 nm) and reduce the possibility of adding an extra column of grid points.

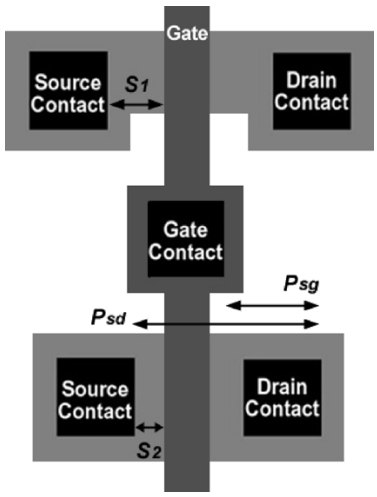

Fig. 8. For the MOSFETs with the gate narrower than the active region (upper), the minimum space between the active contacts and the gate, S_1, is larger than that of other MOSFETs (lower), S_2. Since gate contacts are mostly placed in the middle of active contacts, the pitch, P_{sg}, is half P_{sd}.

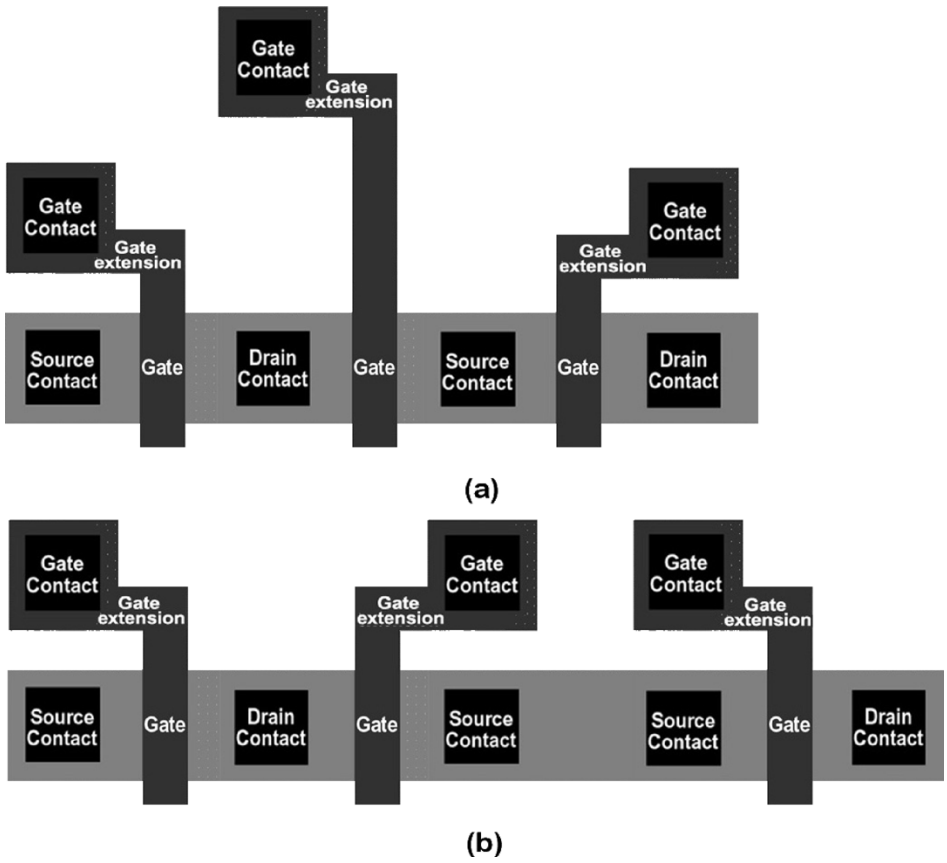

Fig. 9. Two scenarios of snapping contacts of series MOSFETs connection to the grid. Grid pitch is assumed to be the pitch of source and drain contacts.

Offset approach is mainly helpful for sequential cells but not for combinational cells. This is because the layout of combinational cells is regular in both the horizontal and the vertical directions [Fig. 4(a) and Fig. 4(b)]. Offset is also negligible use for the cells with mainly wide MOSFETs, such as cells for a large load capacitor. In this case, most of contacts are redundant and are used to achieve better yield (Fig. 5), being placed regularly in the vertical direction.

As a comparison, four sequential cells are modified using the contact offset to test its effect on the final cell area. Designs not using the contact offset are also listed as a reference. The grid pitches is 475 nm (horizontal) $\times$ 320 nm (vertical). The results are shown in Table I. The areas of two of the cells are decreased by 2% and 3%, respectively, after allowing an offset of contacts.

Finally, we need to note that the effect of contact offset depends on the design rule of the technology used and the grid pitches. Offset is useful only if the spaces between neighboring contacts are just slightly larger than a multiple of grid pitch. Meanwhile, the tolerance for the offset depends on the imaging procedures. We assume 5% as the maximum offset of contacts from grid points comparing with the grid pitches in this study.

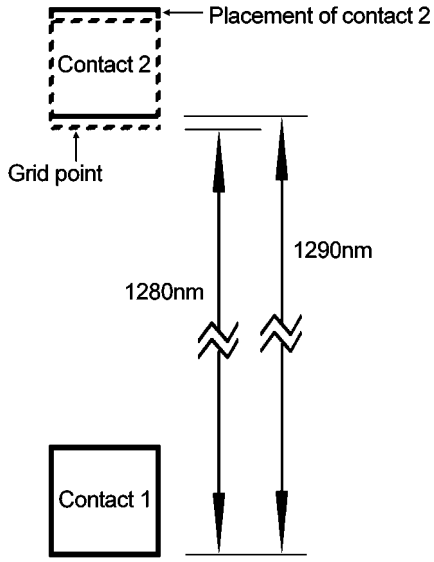

Fig. 10. By allowing a 10-nm offset of the contact from the grid point, it can be avoided to increase the space of contacts in Fig. 6(e) to 1600 nm (5 times of 320 nm).

IV. Double Exposure

Two main conclusions can be drawn from the discussion above: First, vertical and horizontal pitches should be chosen separately according to layout configurations in these directions. Second, the desired grid pitches (320 nm in the height direction and 475 nm in the width direction) are smaller than the improved pitch resolution limit of single-exposure (540 nm).

Although the desired grid pitches are beyond the resolution limit, this kind of grid is still manufacturable because printed contacts never occupy neighboring points on the 475 nm $\times$ 320 nm grid. The actual spacing of contacts will still satisfy the design rules. That means, for example, that the dense grid can be

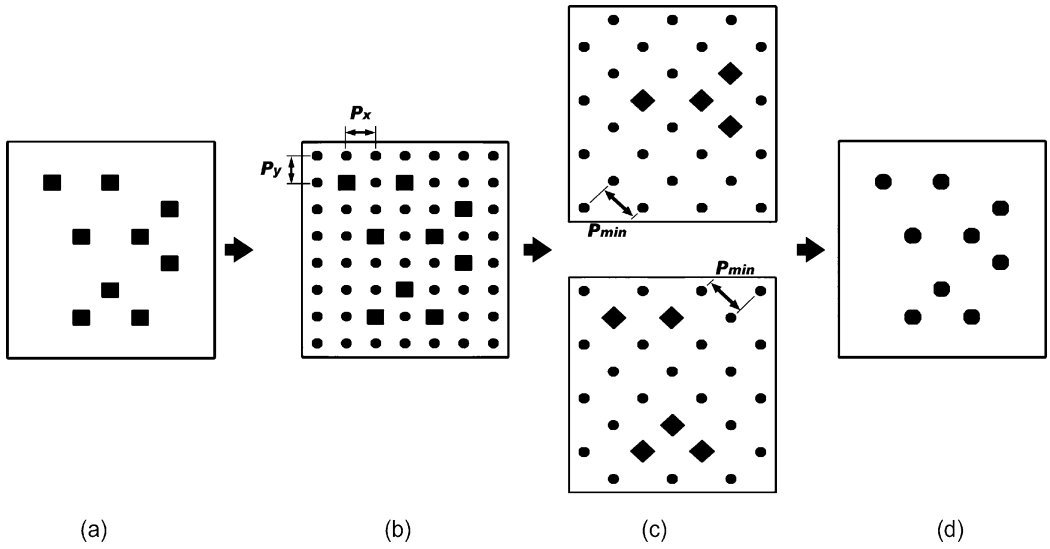

Fig. 11. Exposure of the dense virtual grid by combining two exposures of sparser grids. (a) Layout of contact level; (b) layout with assist contacts; (c) mask patterns for double exposure; (d) printed image.

TABLE I
COMPARING OF THE RELATIVE AREA ($Area_{\text{new}}/Area_{\text{original}} \times 100\%$) AFTER MODIFICATION WITH OR WITHOUT CONTACT OFFSET

Cell name	Area without offset	Area with offset
DFFRHQx1	98%	98%
SDFFTRx2	101%	99%
EDFFx1	105%	102%
D-Latchx1	97%	97%

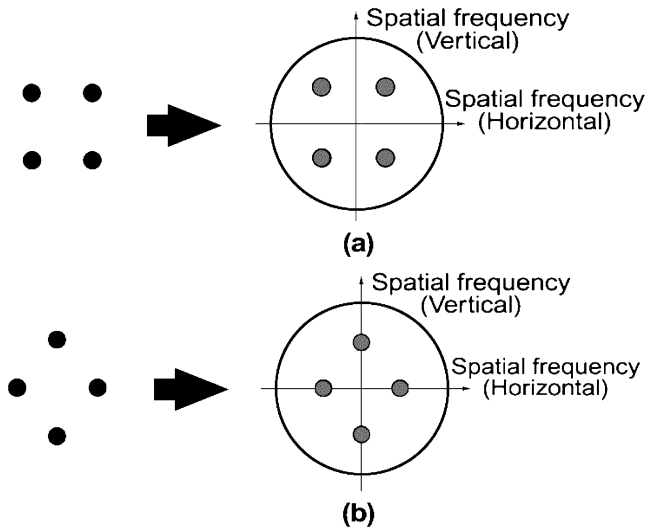

Fig. 12. Poles of quadrupole illumination source should be placed at the axes for double exposure. (a) Illumination source configuration for single exposure; (b) illumination source configuration for double exposures.

decomposed into several sparser grids, each of which is within the resolution limit. The contacts on these sparser grids are fabricated on different masks which are sequentially exposed to form the contact level image. Since the original dense grid is decomposed into several sparser ones, it is called the virtual grid.

Fig. 11 illustrates our proposed double exposure approach [16]. Suppose to fabricate the contact layout of Fig. 11(a), we need to image a dense grid consisting of contacts and assist contacts with horizontal grid pitch P_x and vertical grid pitch P_y, both beyond the resolution limit [Fig. 11(a)]. We can decompose the dense grid into two sparser grids with their axes rotated, as shown in Fig. 11(b) and Fig. 11(c). The rotated grid pitch of sparse grids, P_{min}, is determined by:

$$P_{min} = \sqrt{P_x^2 + P_y^2}. \tag{3}$$

In the case here, $P_x = 475$ nm and $P_y = 320$ nm, implying $P_{\min}$ of 570 nm, which is above the 540 nm improved pitch resolution limit. Sequential exposures of these two masks print all contacts on the virtual grid on the die. Of course, an overlay error on either contact mask would reduce yield, and two masks will cost more than one. However, since mask write times depend on the number of features written, which remains constant comparing with that of a single exposure process, and faster tools can be used for larger pitches, extra costs for reticle can be decreased. It should be reiterated that this double exposure method works because there are no nearest-neighboring contacts on the virtual grid. The particular example in Fig. 11 places assist features or actual contacts at all virtual grid points. Without that RET-based restriction, a single contact mask might suffice.

In addition, the resolution enhancement method should be optimized to expose the actual grids on the masks of the double exposures. For example quadrupole illumination with poles at 45° [Fig. 12(a)] may be optimal to image the grid in Fig. 11(a). However, for imaging of the grids shown in Fig. 11(c), the poles should be placed on the x and y axes [Fig. 12(b)] with distances to zero point determined by P_x and P_y. The sparser grid and regular contacts placement has the additional advantage of preventing unexpected overlap of side-lobes when attenuating-

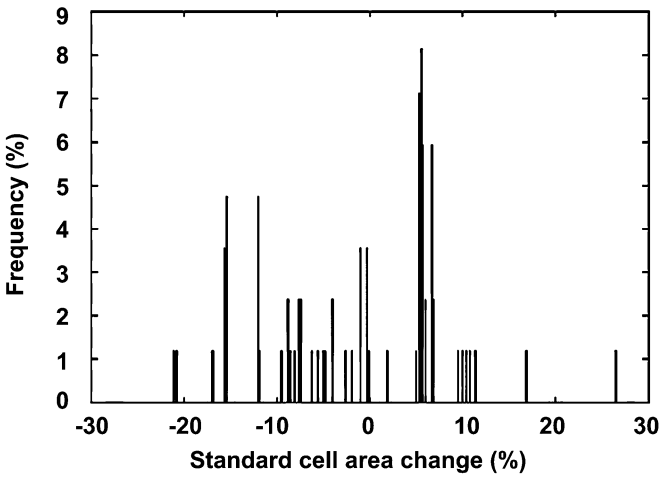

Fig. 13. Histogram of percentage area change of 84 standard cells after snapping contacts on grid. (minimum contact pitch is shrunk by 10%).

PSMs or assist features are used [18]. Phase errors can also be avoided more easily when using alternating-PSMs [19]. Many advanced RET schemes are more easily implemented with grid-based design [20].

V. Cell Placement in Physical Design

During cell placement in the physical design, cells are placed in rows with the power supply paths overlapped. It is expected that the virtual grid of all cells can match to keep a global contact grid across the circuit area. This leads to additional restrictions during standard cell placement. However, as noted in Section II, cells that are father apart than the optical interaction range do not need to be on the same virtual grid. That means the cells can be placed in several blocks, and only in each cell block is a unique virtual grid needed.

VI. Results

To study the effect of regularly placed contacts on standard cell area, 84 cells in a 250-nm library were modified by shrinking the minimum contact pitch and size by 10% and snapping all contacts to the grid with an offset tolerance of 5% comparing with the grid pitches. The virtual grid has a vertical pitch of 320 nm and a horizontal pitch of 475 nm. The height of the standard cell is kept unchanged. Adjustments in cell area are represented by the change of cell widths. Cell area changes are plotted in Fig. 13, which shows the histogram of percentage area change for these 84 standard cells. The percentage area change ranges from -21% to $+27\%$ with an average decrease of 5%. Combinational cells are generally more amenable to regular contacts placement than sequential cells as expected. That is because contact pitches of combinational cells in Fig. 4(a) and Fig. 4(b) naturally have well-defined peaks, whereas sequential cells must be engineered for such behavior.

Although the average cell area change is -5%, It is not convict to conclusion that areas of circuits decrease by 5%. Since different circuits use different combination of standard cells, changes in circuit area will vary from circuit to circuit. Two circuits, a finite impulse response (FIR) filter and an add-compare-select (ACS) unit in Viterbi decoder, were designed using the modified standard cells to study the effect on circuit area. The area of the FIR circuit decreased by 4% while that of the ACS unit shrank by 2%. These initial results are encouraging to the application of the grid-based contact lithography in chip fabrications.

VII. Further Reductions

The area reductions of 2% and 4% may not seem significant enough for an immediate adoption, especially taking into account the additional cost for the lithography process. Further area reduction or other circuit performance improvements are needed to attract a wider application of the grid-layout-based RETs. However, regular contact placement can synergize with other technology development toward such goals. For example, area reductions can be improved by further reductions of the horizontal contacted pitch of MOSFETs ($P_{c\rightarrow c}$ in (2)). The W_c in (2) has been reduced to 90% by the regular contact placement. It is expected that L_g can also be reduced by the grating-placed gates. Nevertheless, the reduction of L_g may have electrical ramifications such as leakage current increase that need to be modeled. The $S_{c\rightarrow g}$ is determined by the alignment error of different masks and cannot be decreased by the fabrication-friendly layout. The increase of the minimum gate width discussed in Section III-A2 can help to reduce the MOSFETs horizontal contacted pitch further. At the same time, to maximize the area decrease by the fabrication-friendly layout, design rules should also be optimized according to the new layout styles and lithographic approaches. In this study, we only use the same design rules except for the rules for the minimum contact size, the minimum contact pitch, and the minimum gate width.

VIII. Conclusion

In this paper, the practicability and methodology of applying regularly placed contacts on layout design are studied. We show that such fabrication-friendly layout does not necessarily mean circuit area increase. Introduction of the virtual grid concept and the use of double exposure, or other advanced RET scheme, makes it possible to place contacts onto a dense virtual grid with pitches beyond the conventional pitch resolution limit. This allows more freedom for fabrication-friendly layout designs and lithography optimization, leads to a smaller average circuit area.

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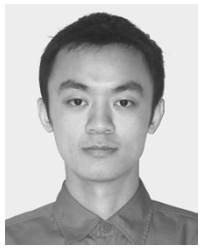

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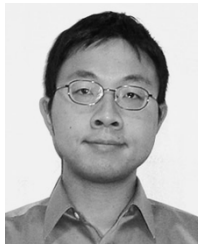

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