Mobility Improvement of n-MOSFET's with Nitrided Gate Oxide by Backsurface Ar^+ Bombardment

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***Abstract*— Low-energy (550 eV) argon-ion beam was used to bombard directly, the backsurface of nitrided n-MOSFET's after the completion of all conventional nMOS processing steps. The interface characteristics and inversion layer mobility of the MOS devices were investigated. The results show that, as bombardment time increases, interface state density and fixed charge density decrease first, and then the change slows down or even turns around. Correspondingly, the carrier mobility and drain conductance of the MOS devices are found to enhance first, and then saturate or turn around. Therefore, this simple technique, which is readily compatible with existing IC processing, is effective for restoring some of the lost device performance associated with gate-oxide nitridation.**

I. Introduction

A VARIETY of nitridation techniques on thin gate dielectrics have been studied intensively in the past decade for their improved dielectric reliability and interface hardness against hot-carrier stress [1]–[3]. However, the electrical performance of resulting MOSFET's generally suffers from this nitrogen incorporation, which roughens the crystal lattice at the interface. On the other hand, ion implantation and ion-beam etching techniques can generate a lattice-damaged layer which can effectively getter lattice defects, in addition to metallic impurities in silicon wafer [4]–[7]. Nevertheless, these gettering processes are, in general, carried out before the completion of the whole devices, and high energy (60 $\sim$ 160 keV), high annealing temperature (800 $\sim$ 1100°C), and long annealing time (1 $\sim$ 3 hrs) are often needed. Obviously, these methods are highly undesirable in VLSI processing technology. In this letter, low-energy (550 eV) Ar^+-beam bombardment on the backsurface and low-temperature (450°C) short-time annealing were used instead, after fabricating n-MOSFET's with NH_3-nitrided oxides as gate dielectrics. The interface characteristics, channel electron mobility (μ_{eff}), and linear drain conductance (G_d) of the devices were then evaluated. Improvements in both μ_{eff} and G_d are found, and possible mechanisms involved are discussed.

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II. Experimental

The n-MOSFET's used in this work were fabricated on p-type (100)-oriented Si wafers (6 $\sim$ 8 Ω cm) using conventional n^+-polysilicon-gate self-aligned MOS technology. The gate oxides were thermally grown at 1000°C in dry oxygen, and then nitrided in pure NH_3, either by rapid thermal annealing at 1200°C for 1 min or by furnace annealing at 1000°C for 60 min (denoted as RTN and NO samples, respectively). The oxide thickness is 240 Å as measured by C-V techniques. Devices with L/W = 3 μm/10 μm were studied. MOS capacitors (100 $\times$ 100 μm^2) were fabricated on the same wafer adjacent to the MOSFET's. After completing all device processing steps, the wafers were put into plating equipment and a low-energy (550 eV) Ar^+ beam with 0.5 mA/cm^2 intensity was applied to directly bombard the backsurface of the wafers at room temperature under a vacuum of 3.2 mPa. Four different bombardment durations, 0, 10, 20, and 40 min, were performed. The corresponding samples are denoted as RTN (0, 10, 20, and 40). The same notations are applied to the NO samples. Subsequently, a layer of aluminum was evaporated on the back of the wafer and then annealed in nitrogen at 450°C for 20 min. Interface characteristics are determined by C-V techniques on the MOS capacitors. Effective electron mobility is calculated using the formula given in [8].

III. Results and Discussion

Fig. 1(a) and (b) show the linear drain conductance (G_d) of the MOSFET's versus gate voltage for RTN and NO samples, respectively. For RTN devices, all three devices receiving Ar^+ bombardment exhibit enhanced G_d, while for NO devices, a turn-around behavior is observed. Specifically, the NO10 device exhibits higher G_d than NO0, with NO20 showing comparable values with NO0; NO40 is worse than NO0. Presented in Fig. 2(a) and (b) are the effective electron mobility of the RTN and NO samples, respectively. Improved μ_{eff} for the three bombarded RTN devices is observed, with RTN10 showing the best improvement ($\sim +10\%$). Like the case of G_d, NO devices show the turn-around behavior again: NO10 is the best ($\sim +5\%$) and NO40 is the worst ($\sim -4\%$). According to the Auger Electron Spectroscopy (AES) analysis (not shown here), higher nitrogen concentration is present at the Si/Oxynitride interface of the NO samples than that of the RTN ones. As a result, electron mobility of the NO

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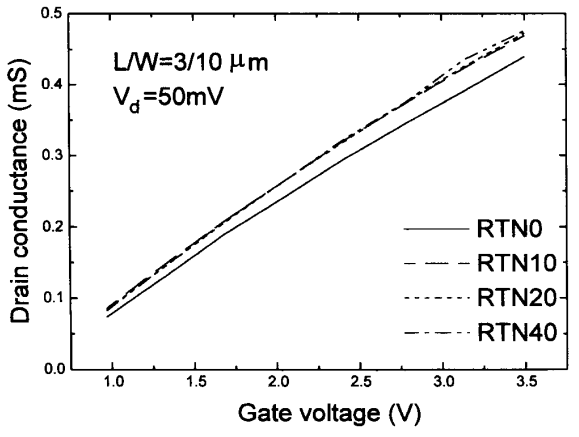
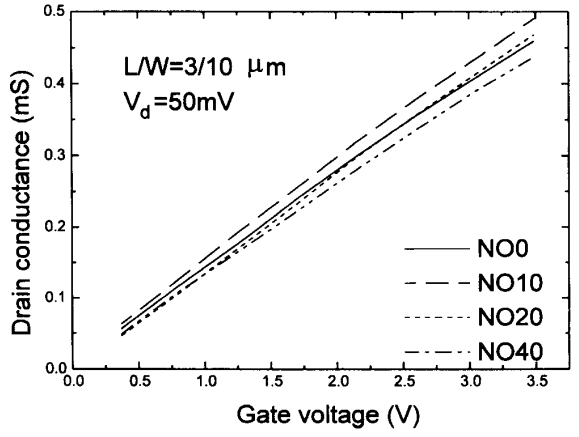
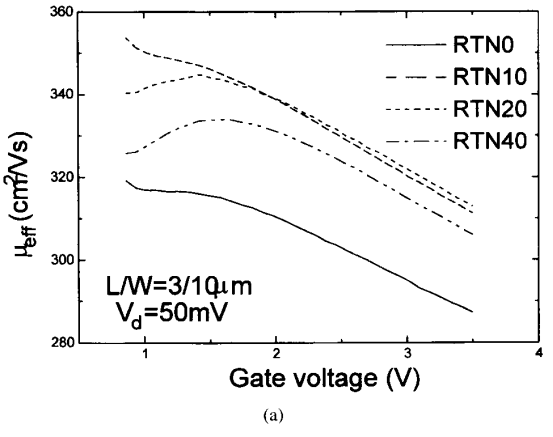


(a)

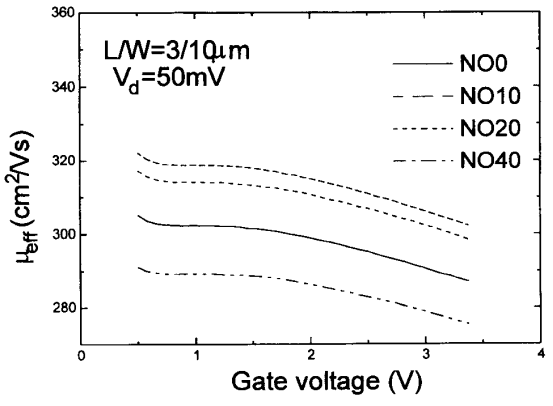


(b)

Fig. 1. Linear drain conductance versus gate voltage with bombardment time as parameters for (a) RTN, and (b) NO devices.



(a)



(b)

Fig. 2. Effective mobility versus gate voltage with bombardment time as parameters for (a) RTN, and (b) NO devices.

samples is improved at high normal field and degraded at low field, exhibiting less μ_{eff} dependence on V_g than that of the RTN ones [9], as shown in Fig. 2. To investigate the causes of the above observations, we measured the interface state and fixed charge densities on the MOS capacitors adjacent to the MOS transistors. The results are given in Fig. 3. It can be clearly seen that both the interface state (D_{itm}) and fixed charge (Q_f) densities of the RTN samples decrease first and then saturate as bombardment time increases. On the other hand, turn-around behavior is found in both D_{itm} and Q_f for the NO samples. This similarity indicates the close relationship between the interface and electrical characteristics of the devices. The bombardment effects on G_d and μ_{eff} can well be attributed to the changes of interface properties. One possible explanation is that the backsurface Ar^+-beam bombardment could create a lattice-damaged layer in the bulk of the wafer which gives rise to some stress at the surface of the wafer, partially compensating the original interface stress created by the processing steps, with gate-oxide nitridation, in particular. This lower stress can reduce both D_{itm} and Q_f, and therefore increase G_d and μ_{eff}. However, excessive stress compensation can appear if bombardment time is too long under a given ion energy and density, resulting in the turn-around behavior observed in NO samples. Moreover, the RTN devices show a much larger reduction in D_{itm} than the NO ones, indicating that the former have a much higher original stress level at the interface. This is expected because the RTN devices have undergone rapid temperature change during gate-oxide nitridation. Furthernore, this bombardment-induced stress relief at the interface can result in higher hot-carrier resistance—our preliminary results have confirmed such an expectation. Another feasible mechanism could be the release of some diffusing species by the Ar^+ bombardment into the back of the wafer, which diffuses to the wafer surface and reacts with the interface. Therefore, further work is required to reveal the actual mechanism of the improvement. Lastly, it is hoped that, by further optimizing the conditions for the backsurface bombardment, even better device characteristics can be achieved.

IV. Conclusion

It is well known that nitrogen incorporation in the gate oxide enhances the interface hardness at the sacrifice of device electrical performance. In this work, we demonstrate that, by using

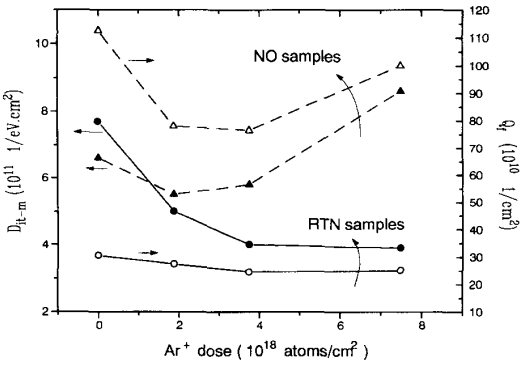


Fig. 3. Interface state and fixed charge densities of MOS capacitors after different bombardment doses.

a simple technique compatible with existing IC processing, the interface characteristics, and hence the electrical characteristics of nitrided MOSFET's, can be improved to some extent. Two possible mechanisms are proposed to explain such change at the nitrided SiO_2-Si interface induced by backsurface Ar^+ bombardment.

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