A Novel Technique of N_2O-Treatment on NH_3-Nitrided Oxide as Gate Dielectric for nMOS Transistors

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***Abstract*—A novel technique of N_2O treatment on NH_3-nitrided oxide is used to prepare thin gate oxide. Experiments on MOS capacitors and nMOSFET's with this kind of gate dielectric show that N_2O treatment is superior to conventional reoxidation step in suppressing both electron and hole trappings and interface trap creation under high-field stress. Interface hardness against hot-carrier bombardment and neutral electron trap generation are also improved. Thus, N_2O treatment on NH_3-nitrided oxide shows excellent electrical and reliability properties, while maintaining sufficiently high nitrogen concentration in gate oxide which offers good resistance to dopant penetration.**

I. Introduction

MOS VLSI circuits require devices with high quality thin gate and tunnelling oxides. The problems associated with charge flow under Fowler–Nordheim (F-N) and/or hot carrier injection through such oxides adversely affect device reliability, and are therefore of primary concern. In addition, good diffusion-barrier property is a key requirement for gate oxide, especially in dual-gate CMOS technology, where p^+ doped poly-Si gate pMOSFET's are used [1]. Therefore, various oxynitride dielectrics fabricated by different techniques have been extensively investigated in the past as an alternative to conventional SiO_2 in submicrometer MOS devices [2]–[15]. For example, NH_3 nitridation can introduce sufficiently high nitrogen concentration [N] at the Si/SiO_2 interface which improves the interface hardness against hot-carrier bombardment. However, hydrogen-related species are also incorporated in the resulting oxides (NO), which introduce a large amount of electron traps and consequently increase electron trapping significantly [2]. Reoxidation of NH_3-nitrided oxides (RONO) can only partially eliminate the nitridation-induced electron traps [2], [3]. Recently developed N_2O-nitrided (N_2ON) [4], [5] and N_2O-grown (N_2OG) [6] oxides eliminate hydrogen-related species from processing environment, but these kinds of oxides may not contain sufficient nitrogen to prevent boron penetration from p^+ doped poly-Si gate [7]. In this paper, a new technique, namely N_2O treatment of NH_3-nitrided oxides (N_2ONO), is proposed. On the basis of preliminary study [8], [9], the charge-trapping properties and device degradation under both F-N high-field stress and channel hot-carrier stress on MOS capacitors and nMOSFET's with this kind of oxide are studied comparatively in more detail with four other kinds of oxides, with emphasis on the comparison between the reoxidation step and N_2O treatment.

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II. Experimental

MOS capacitors and nMOSFET's were fabricated on 6–8 Ω·cm (100) p-type Si substrate using conventional n^+ polysilicon-gate MOS technology. The channel doping of nMOSFET's ($\sim 2 \times 10^{17}$ cm^{-3}) was controlled by boron implant through a sacrificial oxide which was stripped after the implant. Then, five kinds of gate dielectrics were prepared according to the conditions listed in Table I. Note that the oxidation durations for the five gate dielectrics are slightly different in order to achieve similar thickness of resulting oxides. All gate oxides were finally annealed in N_2 at 950 °C for 25 min. Polysilicon-gate, 450 nm-thick, was then deposited by LPCVD at 625 °C, followed by phosphorous diffusion at 950 °C and annealed in nitrogen at 960 °C for 20 min. Gates were defined by RIE etching. Al metallization and sintering in forming gas at 430 °C for 30 min completed the process. The equivalent thickness of gate dielectrics is listed in Table I as measured by *CV* techniques. No passivation film was used.

The experimental set-up used to test and stress the devices consisted of an HP 4145B semiconductor parameter analyzer for constant current injections, stresses, and measurements, an HP 4140B pA meter and an HP 4284A precision LCR meter for quasistatic and high-frequency (1 MHz) *CV* measurements respectively. All instruments used were controlled by a desktop computer. F-N injections on capacitors were performed at a constant current level of -1 mA/cm^2 (negative gate bias), which corresponded to an average electric field in the oxide of 9~10 MV/cm. This current density was comparable to those encountered in E^{2}PROM's. *CV* measurements on the capacitors were alternated with F-N injections to determine the flatband voltage (V_{FB}) and interface state density (D_{it-m}). Measurements showed that the interruptions of injection necessary to record the *CV* curves only negligibly affected the charges generated in the oxide, since difference of gate voltages required to maintain constant current injection before and after *CV* measurements was negligibly small (<5 mV). A low-density constant current (-0.01 mA/cm^2) stress on MOS capacitors was also conducted to investigate the hole trapping

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TABLE I
GATE OXIDE FABRICATION CONDITIONS AND THE INITIAL PROPERTIES MEASURED ON MOS CAPACITORS

samples	oxidation	nitridation (35 min)	the third step (30 min)	N_f (10^{11} cm^{-2})	$D_{it\text{-}m}$ (10^{11} eV^{-1}cm^{-2})	thickness (Å)
OX	O_2, 850 °C, 70 min	-------	-------	0.1	0.6	138
N2ON	O_2, 850 °C, 60 min	N_2O, 950 °C	------	0.3	1.7	142
NO	O_2, 850 °C, 70 min	NH_3, 950 °C	-------	10	3.0	136
N2ONO	O_2, 850 °C, 65 min	NH_3, 950 °C	N_2O, 950 °C	5	1.8	128
RONO	O_2, 850 °C, 70 min	NH_3, 950 °C	O_2, 950 °C	6	1.6	126

rate of these oxides [10]. The area of the capacitors was 100×200 μm^2. To stress the nMOSFET's, a constant injection current density of 0.5 mA/cm^2 with the gate positively biased was applied to the gate while the source and drain shorted to the substrate and grounded. The shifts in the threshold voltage (V_T) and subthreshold gate-voltage swing (S) of the devices were taken as measures of device degradation. V_T was defined as the linearly extrapolated value of gate voltage at $I_D = 0$ with $V_D = 50$ mV. S was calculated as the gate-voltage swing needed to reduce subthreshold current by one decade. To minimize small-size effects and to ensure uniform F-N injection, nMOSFET's with large device dimensions ($L/W = 100$ μm/100 μm) were selected in this stress. Moreover, hot carrier reliability under various stress conditions was studied on the nMOS transistors with smaller device size ($W_{\rm drawn}/L_{\rm drawn} = 12/1.2$ μm). The effective channel length $L_{\rm eff}$ was 1.0 μm ($\Delta L = 0.2$ μm), as was extracted by measuring *IV* characteristics on a group of nMOSFET's with different channel lengths but same width based on BSIMPro program [11]. All measurements in this work were conducted at room temperature.

III. RESULTS AND DISCUSSIONS

A. Initial Characteristics

Initial fixed charge (N_f) and midgap interface state density ($D_{\rm it-m}$) extracted from *CV* data on MOS capacitors with various gate dielectrics are presented in Table I. Like the reoxidation step for RONO samples, the N_2O treatment on NO samples (N_2ONO) reduces the N_f to the similar level as RONO samples, and the $D_{\rm it\text{-}m}$ values are comparable among the N_2ON, RONO, and N_2ONO samples. The dependence of initial transconductance (G_m) on gate voltage (V_G) of nMOSFET's with different gate dielectrics is shown in Fig. 1. Lower peak G_m is found in the NO, RONO and N_2ONO gate oxide devices, as compared to OX and N_2ON devices due to the relatively heavy nitridation of gate oxides [2]. However, N_2ONO device exhibits less peak G_m degradation than NO and RONO device. And improved G_m in the high-V_G regime is observed in RONO and N_2ONO gate oxide devices when compared with OX devices, which is typical as a result of nitridation-induced residual mechanical stress [12]. Since this phenomenon is not observed in the N_2ON device, it can be deduced that the nitridation level in the N_2ON device is quite low and might not be sufficient to prevent boron penetration in p$^+$ poly-gate pMOSFET's.

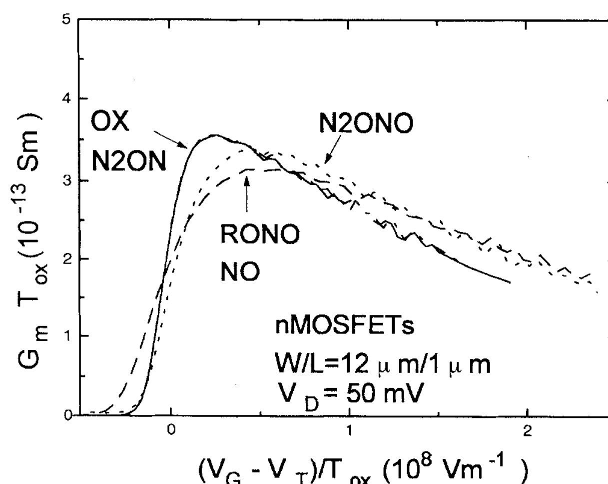

Fig. 1. Dependence of initial transconductance on gate bias for the nMOS devices with OX, RONO, NO, N_2ON, and N_2ONO gate dielectrics.

B. Oxide Characteristics of MOS Capacitors under High-Field Stress

Electron trapping properties of oxides were studied by monitoring the change in gate voltage (ΔV_G) to maintain a constant current density (-1 mA/cm^2) in MOS capacitors. As shown in Fig. 2, in general, NO oxides show the largest ΔV_G, indicating significant electron trapping by NH_3-nitridation-induced electron traps [13]. On the other hand, N_2ONO oxides show only a small ΔV_G, suggesting greatly suppressed electron trapping, which is comparable to N_2O-nitrided oxides (N_2ON) and superior to RONO and conventional thermal oxides (OX). In detail, in the lower injection fluence region where ΔV_G does not go up linearly, electron trapping mainly takes place in pre-existing traps. In NO oxides, hydrogen-related species such as -H and -OH bonds produced by the decomposition of NH_3 in the oxide bulk are mainly responsible for these traps [14]. Therefore, results in Fig. 2 indicate that N_2O treatment (N_2ONO oxide) is more effective in reducing these electron traps than reoxidation process (RONO oxide) by annealing out the hydrogen. The amount of pre-existing electron traps in N_2ONO oxides is similar to that in N_2ON oxides. In the higher injection fluence region where ΔV_G goes up linearly, electron trapping is dominated by newly generated electron traps. The generation rate is constant and proportional to dV_G/dF, where F is tunnelling fluence [15]. Consequently, the lowest electron trap generation rate is observed in Fig. 2 for N_2ONO oxides. Fig. 3 gives some typical quasistatic

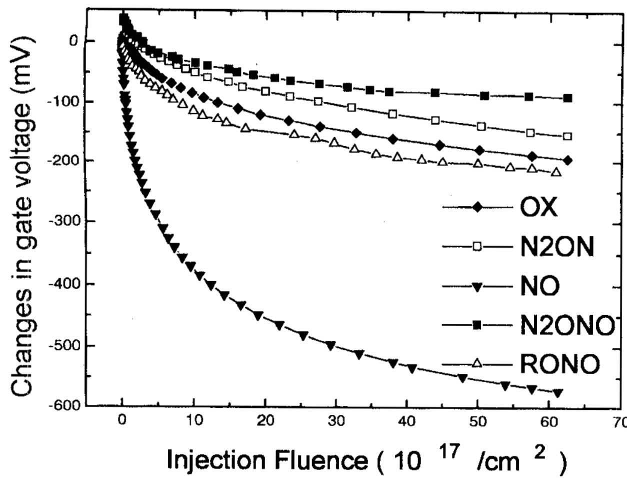

Fig. 2. Change in gate voltage required to maintain a constant current density ($J_G = -1$ mA/cm^2) versus injected electron fluence for OX, N_2ON, NO, N_2ONO, and RONO oxides.

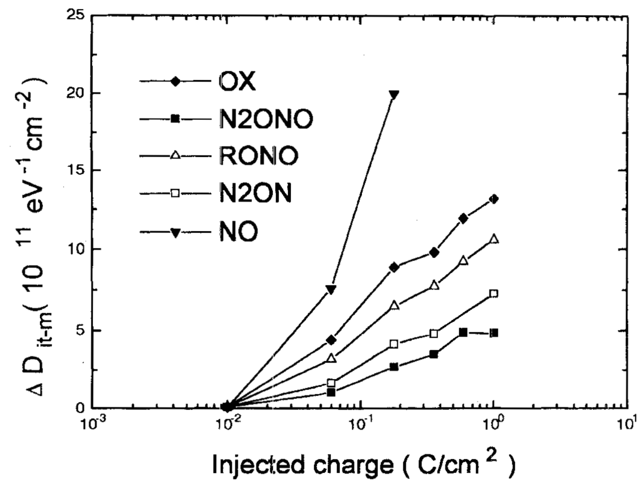

Fig. 4. Increase in midgap interface state density ($\Delta D_{\mathrm{it-m}}$ of MOS capacitors with different gate dielectrics under F-N injection stress (-1 mA/cm^2).

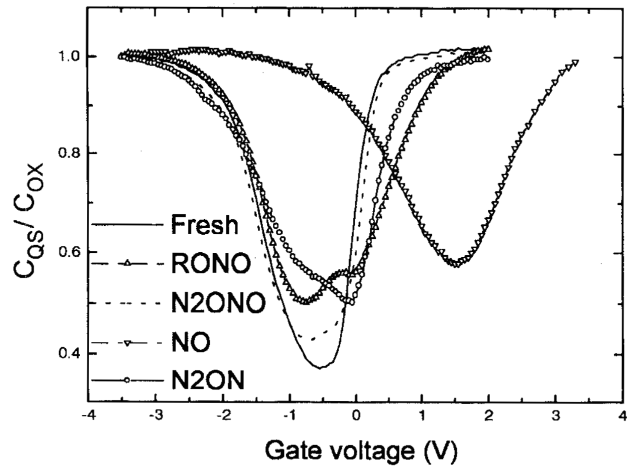

Fig. 3. Typical normalized quasistatic capacitance-voltage characteristics after 6 min of injection ($J_G = -1$ mA/cm^2) for several kinds of capacitors.

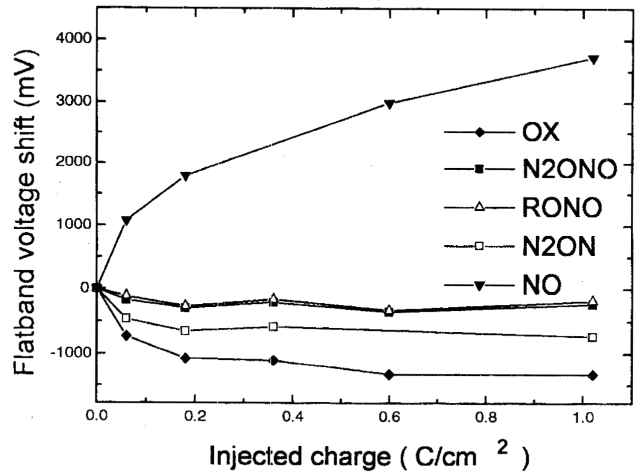

Fig. 5. Flatband voltage shift versus injected charge density on MOS capacitors for different gate dielectrics under the same stress condition as that used in Fig. 4.

capacitance characteristics after 6 min of high-field injection (-1 mA/cm^2). The extracted midgap interface-state creation ($\Delta D_{\mathrm{it-m}}$) due to the stress is presented in Fig. 4. Increased interface state generation (ΔD_{it}) is observed in NO oxides as compared to OX oxides [13], [17]. However, ΔD_{it} in N_2ONO oxides is comparable to the N_2ON oxides and superior to RONO and OX oxides. Large ΔD_{it} in NO oxides is attributed to a distorted interfacial region due to the formation of mismatched Si-N bonds in the Si-O network. N_2O treatment on NO oxides significantly suppresses this undesirable effect, as seen from Fig. 4.

Depicted in Fig. 5 is the corresponding flatband voltage shift (ΔV_{FB}) under the same stress condition as that used in Fig. 4. Unlike ΔV_g, which is most sensitive to charges located near the cathode, ΔV_{FB} is the combined effect of charge trapping at the interface states and in the bulk oxide, and mainly reflects the charges near the Si/gate-oxide interface [18]. A large positive ΔV_{FB} in NO oxide, shown in Fig. 5, indicates severe negative charge trapping, and in this case, bulk trapping plays a major role in determining ΔV_{FB}. For the other four dielectrics, a negative-going shift in V_{FB} is observed, implying the trapping of positive charges. In this case, trapping near the interface dominates since bulk electron trapping is greatly suppressed in these four gate oxides, as is evident in Fig. 2. The positive charges are due to generated donor-like interface states [19], which are positively charged when they are unoccupied under *CV* measurement conditions, and/or the generation of positively charged "slow states," or "anomalous positive charge" (APC) [20]. From Fig. 5, we can see N_2ONO and RONO oxides exhibit least donor-type D_{it} or APC generation.

C. Hole Trapping Properties of MOS Capacitors

Hole trapping in the gate dielectric is a key phenomenon for the reliability of nMOS transistors [21] and oxide breakdown

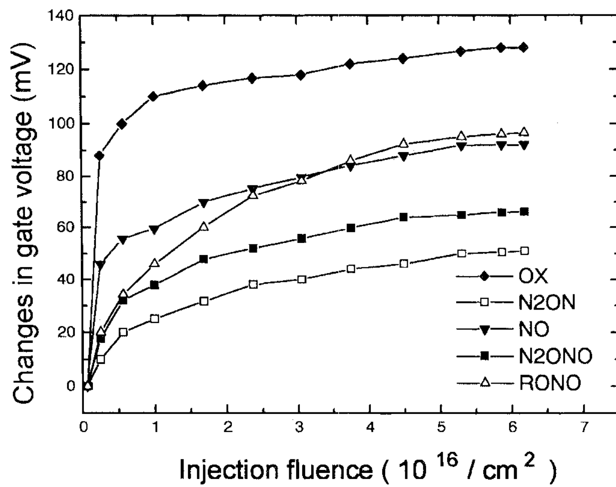

Fig. 6. Gate voltage shift versus injected electron fluence during low-density constant current injection ($J_G = -10\ \mu A/cm^2$) on MOS capacitors for various kinds of oxides.

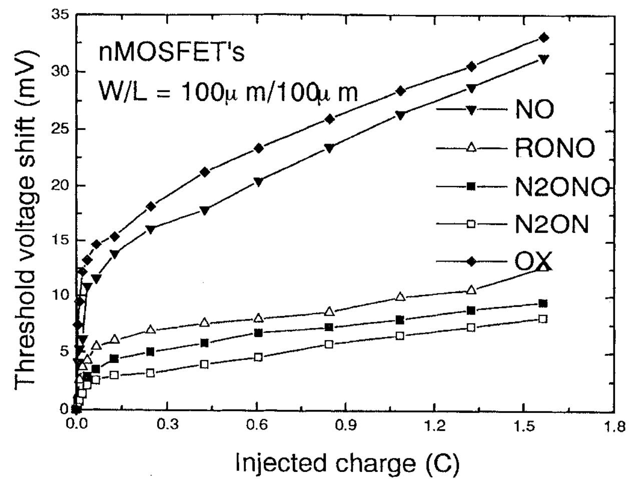

Fig. 7. The shift of threshold voltage vs injected charge for the five kinds of nMOSFET's under positive gate voltage F-N constant current stress ($J_G = +0.5$ mA/cm^2).

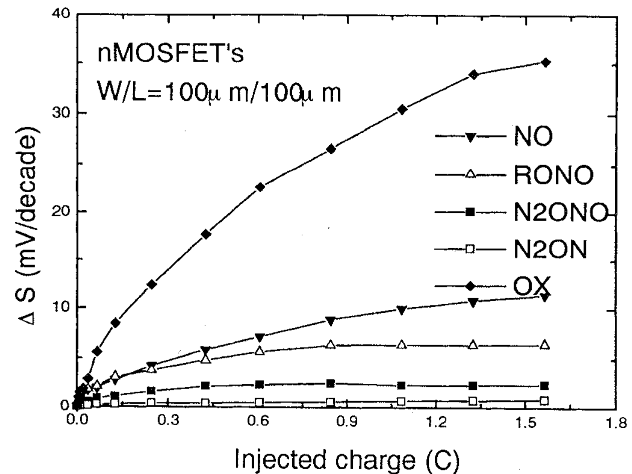

Fig. 8. The shift in subthreshold gate-voltage swing versus injected charge for the five kinds of nMOSFET's under the same stress condition as that used in Fig. 7.

under high-field current injection stress [22]. Hole trapping rate of the oxides studied was investigated by applying a low-density constant current (-0.01 mA/cm^2) stress on MOS capacitors. The data are presented in Fig. 6. The trapping of positive charge is characterized by the gate voltage reduction during the initial period of current stressing in a low electron fluence region ($<10^{17}$/cm^2). According to this figure, N_2O treatment after NH_3-nitridation (N_2ONO) is superior to the reoxidation process (RONO) in suppressing hole trapping. Our results also show that NH_3-nitridation reduces the hole trapping as compared to the control oxide, in agreement with the previous reports in [23], [24] on the basis of measurements using both the hole avalanche injection and high-field stress techniques. Moreover, reoxidation process does not definitely further decrease the hole trapping, as the case in our sample shown in Fig. 6. It has been pointed out that a relatively heavy reoxidation is required to bring about a further reduction of the hole trap density, which is correlated to the formation of an oxygen-rich layer near the silicon interface [23]. Further, it appears that the hole trapping takes place mainly in the pre-existing traps, since low applied voltage required for low current density injection is less likely to produce traps. This argument is further supported by the voltage saturation trend at the higher-fluence regime in the Fig. 6. The appearance of positive charges is believed to be due to the holes generated at the anode interface as a result of impact ionization by tunnelling electrons and subsequently trapped near the anode valence band edge [25].

D. NMOSFET Degradation under F-N Stress

Figs. 7 and 8 describe the degradations of V_T and S in nMOSFET's ($L/W = 100\ \mu m/100\ \mu m$) with increasing injected charge under F-N constant current stress (+0.5 mA/cm^2). N_2ONO oxide is superior to OX, NO, and RONO oxides in terms of V_T and S shifts, and is slightly worse than N_2ON oxide. It is worth noting that, although ΔV_T of OX and NO oxides are comparable as shown in Fig. 7, the corresponding ΔS of OX oxide is much larger than that of NO oxide, as can be seen in Fig. 8, indicating the ΔV_T of OX devices mainly arises from the interface state generation, while the ΔV_T of NO devices is dominated by bulk charge trapping due to a high density of electron traps. Both mechanisms are greatly suppressed especially in the N_2ONO and N_2ON oxides. The results in Figs. 7 and 8 also suggest that N_2O treatment on the NH_3-nitrided oxide (N_2ONO) gives better gate oxide quality than reoxidation treatment (RONO).

E. NMOSFET's Degradation under Channel Hot Carrier Stress

Three hot-carrier stress conditions were employed to investigate the reliability of nMOS transistors with the different gate dielectrics studied. The first one is called channel hot electron (CHE) stress with $V_G = V_D = 6.5$ V, which induces mainly electron traps in the gate oxide and fills them with the

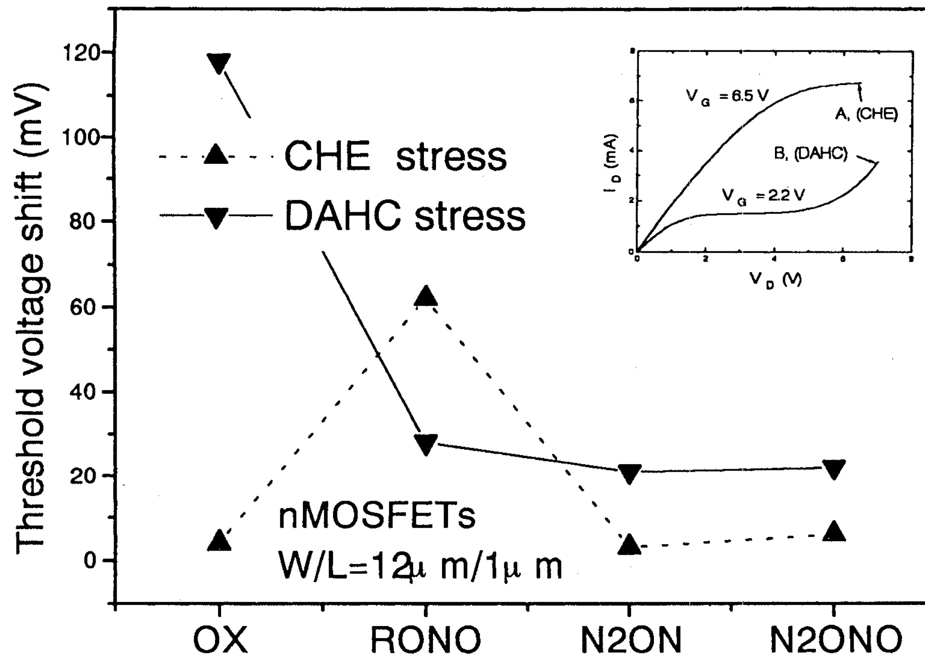

Fig. 9. Threshold voltage shifts of nMOS transistors with four kinds of gate dielectrics under CHE stress ($V_G = V_D = 6.5$ V) and DAHC stress ($I_{b,max}$ and $V_D = 7$ V). Stress time is 2400 s. Stress biases illustrated by the point of A and B in the inset.

injected channel hot electrons [26]. The second one is drain avalanche hot carrier (DAHC) stress. During this stressing, the gate voltage is adjusted to achieve maximum substrate current ($I_{b,max}$), while the drain voltage is increased to the drain avalanche regime ($V_D = 7$ V), which is characterized by a sharp increase in drain current as a result of electron-hole pair generation through impact ionization in drain junction. The bias conditions for the CHE and DAHC stressings are illustrated by the A and B points, respectively, in the inset of Fig. 9. Low gate voltage hot-carrier stressing ($V_G \approx V_D/5$, $V_D = 7$ V) was employed as the third one. During this type of stressing, both hole and electron traps are created in gate dielectrics, as well as a small quantity of interface states [27], [28], as a result of the injection of hot holes generated by impact ionization [29]. However, since the generated electron traps are initially neutrally charged, a short electron injection phase (at $V_G = V_D = 6.5$ V for 20 s) was used to fills the neutral electron traps so that their influence on the I_D-V_G curves can be fully characterized [27]. Such damage is especially important in dynamic operating environment where neutral traps can be generated and filled, resulting in enhanced degradation [30]. Source and substrate were tied to ground in all the above stress measurements.

Threshold voltage shifts (ΔV_T) of nMOS devices with OX, N_2ON, N_2ONO, and RONO gate dielectrics under CHE and DAHC stressings for 2400 s are shown in Fig. 9. Largest ΔV_T is observed for RONO device in channel electron injection stress ($V_G = V_D = 6.5$ V). While N_2ONO device exhibits much smaller ΔV_T, which is comparable with OX and N_2O devices. This result indicates that N_2O treatment after NH_3-nitridation is much more effective than reoxidation process in reducing electron traps induced by NH_3-nitridation. Under DAHC stress ($I_{b,max}$ and $V_D = 7$ V), both RONO and N_2ONO devices show much suppressed V_T degradation than OX device, since interface state generation now is the dominant damage [26]. Devices with nitrided gate dielectrics therefore exhibit enhanced interface resistance against stress degradation than conventional thermal oxide as a result of interfacial nitrogen incorporation, which introduces stronger Si-N bonds ($E_{Si-N} \sim 4.6$ eV) [16], [31] and relaxes interfacial strained Si-O bonds [32]. Higher [N] may exist in the N_2ONO oxide than RONO oxide, since reoxidation step reduces not only hydrogen concentration, but also [N] both at surface and in the bulk [16]. Thus, improved immunity of interface state generation under hot-carrier bombardment in the N_2ONO oxide as compared to RONO oxide is expected.

Changes in threshold voltage (V_T) and peak linear transconductance (G_m) of the nMOS devices with the gate dielectrics studied under low V_G stress for 2400 s and subsequent 20 s of electron injection are given in Fig. 10(a) and (b), respectively. A negative V_T shift and an increase in G_m are observed in the first low V_G stress phase due to the channel shortening effect caused by hole trapping in gate dielectrics localized near the drain junction [27], [28]. This property could be used as an estimate of hole injection into the gate dielectric. The results shown in curve A of Fig. 10(a) and (b) indicate that N_2ON oxide has minimum hole trapping and OX oxide has the maximum. N_2ONO oxide, once again, exhibits slightly improved hole trapping property, in agreement with the results in Fig. 6 obtained from low-density constant current stress. Subsequent short electron injection shifts the curve A to B as shown in Fig. 10. Large positive V_T shift and G_m degradation are obtained due to compensation of trapped holes and filling of neutral electron traps by injected electrons. It should be

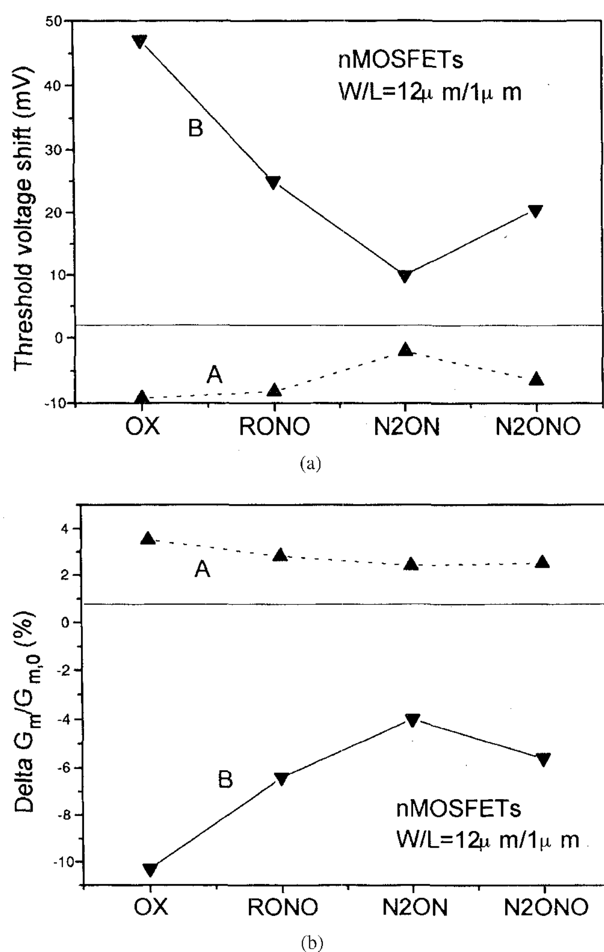

Fig. 10. Threshold voltage change (a) and percentage degradation of peak linear transconductance (b) of nMOS transistors with various kinds of gate dielectrics. Curve A: immediately after low gate voltage stress at $V_G = 1$ V, $V_D = 7$ V for 2000 s. Curve B: following a short electron injection phase at $V_G = V_D = 6.5$ V for 20 s.

noted that the electron injection itself introduced negligible damage because of its short stress time, as is verified by measuring fresh devices. As expected, N_2ONO oxide shows suppressed neutral electron trap generation under low V_G stress in comparison with RONO oxide, as indicated by curve B in Fig. 10, since the neutral electron traps are believed to be created through the recombination of injected electrons and trapped holes [33] and hole trap density in N_2ONO oxide has been verified to be lower than that in RONO oxide. Furthermore, the neutral traps are likely to lie in the vicinity of interface because the injected holes are unable to penetrate deep in the dielectric bulk [34]. Therefore, their influence on device characteristics is significant. Thus, suppression of this kind of damage is critical in improving device reliability, especially under AC dynamic stress [30].

IV. Conclusion

In conclusion, a new technique of N_2O treatment on NH_3-nitrided oxide is used to prepare thin gate dielectric for nMOS transistors. The charge-trapping properties of the gate dielectrics on MOS capacitors and degradation of nMOSFET's under F-N constant current stresses and channel hot-carrier stresses were comparatively investigated among several dielectrics fabricated by different techniques. We have found that this new kind of oxide (N_2ONO) has significantly lower pre-existing bulk electron and hole traps, and greatly suppressed bulk electron trap and interface state generation under F-N stress as compared to reoxidized NH_3-nitrided (RONO) oxide. Moreover, various channel hot-carrier stress experiments demonstrate that electron trapping, interface damage, and neutral electron trap generation under channel hot-carrier stress of nMOSFET's with N_2ONO gate oxide are less than the ones of devices with RONO gate oxide, which can be attributed to the N_2O treatment giving a higher nitrogen concentration [N] in N_2ONO oxide. As for the comparison between N_2ONO and N_2O-nitrided (N_2ON) oxides, the former one shows slightly worse reliability properties. However, it has higher [N] through the use of NH_3 nitridation. This higher [N] in N_2ONO oxide gives rise to a better resistance to boron diffusion in p^+ poly-gate p-MOSFET's, which could be a serious problem if N_2ON oxide is used as gate oxide.

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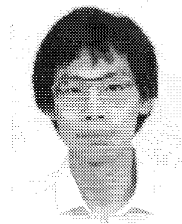

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