

A New Lateral Trench-Gate Conductivity Modulated Power Transistor

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Abstract—In this paper, a new conductivity modulated power transistor called the Lateral Trench-Gate Bipolar Transistor (LTGBT) is presented. This structure incorporates a trench-gate in which the locations of the channel and source in conventional LIGBT have been interchanged. This channel and source arrangement results in significant improvement in latch-up current density. Experimental results indicate that the static and dynamic latch-up current densities are improved by 2.3 and 4.2 times, respectively, compared to those of the LIGBT at a n^+ cathode length of $5\ \mu\text{m}$. Dependence of the latch-up current density of the LTGBT on the design of the n^+ and p^+ cathode regions is examined both numerically and experimentally. The maximum controllable current density is found to be increased when the space between the trench-gate and the p^+ cathode is reduced. Specifically, as the space is decreased to $2\ \mu\text{m}$, no latch-up phenomenon was observed. This nonlatch-up characteristic is obtained at the expense of a slight increase (0.8 V) in threshold voltage.

Index Terms—Conductivity modulation, latch-up, power integrated circuits, power transistors, trench-gate.

I. INTRODUCTION

POWER transistors to be used in Power Integrated Circuits (PIC's) are generally required to have low on-resistance, fast switching speed, and high breakdown voltage. The lateral IGBT's (LIGBT's) [1] are commonly used power devices for PIC applications because of their superior device characteristics. In these devices, the high current handling capability relies on conductivity modulation of the high resistivity drift region. However, device latch-up, which leads to loss of gate control, may occur at high current due to the existence of the parasitic thyristor. Since device failure due to latch-up prevents the device to be used in practical applications, it is very important to improve the latch-up characteristics of the LIGBT. Modification of the structure to improve the latch-up

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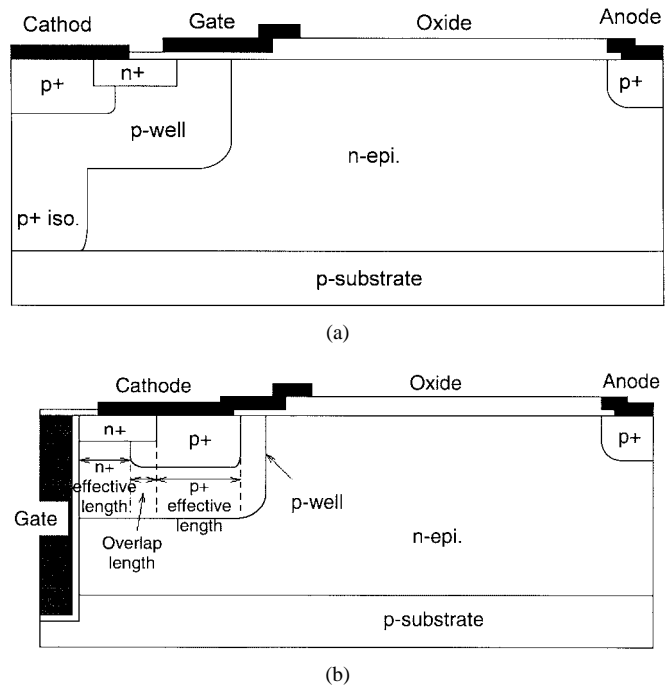


Fig. 1. Schematic cross section of (a) the LIGBT and (b) the LTGBT.

characteristics of the LIGBT has been carried out extensively [2]–[4].

In this paper, a new Lateral Trench-Gate Bipolar Transistor (LTGBT) structure [5] for improved latch-up characteristics is presented. The same structure has been implemented on SOI substrate for the same purpose [6]. Since SOI is an entirely different technology (better isolation and much more expensive) compared with bulk silicon technology (less perfect isolation and very economical), it is important to find out the device characteristics of the LTGBT on bulk silicon. Numerical simulations on the static and dynamic latch-up current densities are shown in comparison with those of the conventional LIGBT. Dependence of the latch-up current density on the design of the n^+ and p^+ cathode regions of the LTGBT structure will also be discussed. The conductivity modulation effect of the LTGBT has been characterized, and the results are compared with those of the trench gate LDMOS fabricated on the same wafer.

II. DEVICE STRUCTURE AND OPERATION

Fig. 1 illustrates both the LIGBT and the LTGBT structures. The main difference between the two structures is the place-

ment of the MOS gate region and the n^+/p^+ cathode regions. In the LTGBT, the MOS gate is formed using a vertical trench with the contact of the p-well region located in front of the n^+ cathode. The p-well is connected with the n^+ cathode through the p^+ cathode. Existing of the p-well between the channel and the anode regions facilitates the collection of holes by the p^+ cathode contact so that holes will have less tendency to flow through the area underneath the n^+ cathode to cause device latch-up. At the on-state, the vertical channel depletion region can also divert holes to flow away from that region and reduce the number of holes to flow underneath the n^+ cathode. All of these allow the holes to be collected effectively by the p^+ cathode through the p-well before reaching the n^+ cathode, and latch-up of the structure can be prevented.

Operation of the LTGBT is identical to that of the LIGBT. In the forward active mode of operation, a positive voltage is applied to the anode relative to the cathode. Anode current starts to flow at gate voltages higher than the threshold voltage and an anode voltage higher than one diode drop. At a higher anode voltage, the anode pn junction starts to turn on and injects holes into the n-epi of the transistor. Some of these holes will recombine with the electrons flowing in from the vertical channel, and some of them will flow from the n-epi to the p-well and be collected by the p^+ cathode without flowing through the area underneath the n^+ cathode. So they do not cause latch-up.

To further improve the latch-up characteristics of the structure, it is required to make the n^+ cathode region short. However, minimum length of the n^+ region is limited by the photolithography capability. One way to avoid the need of expensive photolithography is to overlap the n^+ and p^+ cathode regions, and with a differential junction depth between the n^+ and p^+ cathode regions. With the p^+ junction depth deeper than that of the n^+ junction depth and the p^+ concentration lower than that of the n^+ concentration, the long n^+ cathode region needed will be provided at the surface, and its effect on latch-up can be minimized by the portion of the p^+ cathode which is situated underneath the n^+ cathode. In this way, the device will have effectively a very short n^+ cathode, depending on the amount of overlap. The reduced cathode length and the location of the p^+ in front of the n^+ cathode in the LTGBT ensures better protection against latch-up.

III. TWO-DIMENSIONAL SIMULATIONS

To analyze the on-state and latch-up performance of the LTGBT, numerical simulations were performed using the two-dimensional device simulator MEDICI [7]. MEDICI allows the on-state and off-state performance of such a complex structure to be simulated. The LTGBT used in the simulation is shown in Fig. 1(b) which is designed to have a drift region length of $40\ \mu\text{m}$. The thickness of the n-epi is $3\ \mu\text{m}$. The p-well has a surface concentration of $10^{17}/\text{cm}^3$ and a depth of $2\ \mu\text{m}$. The channel length is approximately $1.5\ \mu\text{m}$.

The electron and hole current vectors of the LTGBT at the on-state with an n^+ cathode length of $8\ \mu\text{m}$ are shown in Fig. 2(a) and (b), respectively. It is observed that electrons are flowing from the vertical channel to the n-drift region and

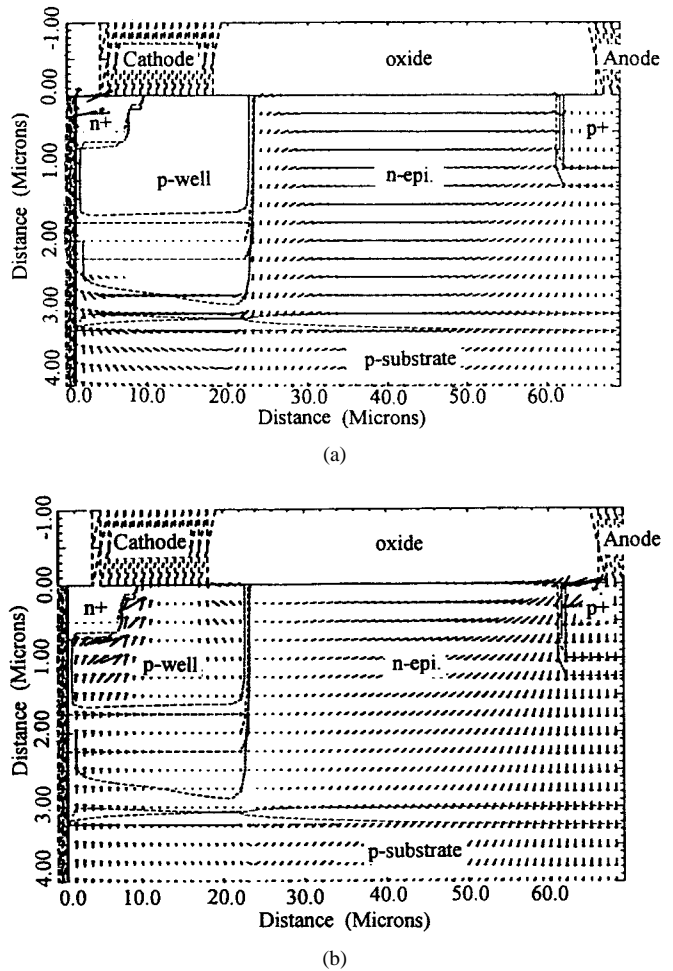


Fig. 2. Current vectors of (a) electron and (b) hole of the LTGBT for an n^+ cathode length of $8\ \mu\text{m}$ and at a forward voltage of $1.6\ \text{V}$.

the p-substrate, and holes are injected from the p^+ anode into the n-epi. Part of the holes flow from the n-epi into the p-well. And part of them recombine with electrons flowing in from the channel. These holes that flow into the p-well will be collected by the p^+ cathode without causing latch-up. For holes that flow underneath the p-well to recombine with electrons there, part of them will travel back to the p-well via the path underneath the n^+ cathode. Thus, the area underneath the n^+ cathode is found to have some holes. It is noted that the n-epi/p-substrate junction has been turned-on due to the fact that the entire region is flooded with electron-hole plasma. Depending on the length of the n^+ cathode, latch-up might occur if the n^+ cathode is sufficiently long. At a longer n^+ cathode (e.g., $12\ \mu\text{m}$), more holes are shown to flow in the area underneath the n^+ cathode [Fig. 3(a)] with the same forward voltage of $1.6\ \text{V}$. At a higher forward voltage ($3.0\ \text{V}$), the hole current eventually turns on the n^+ cathode/p-well junction, and holes start to flow into the n^+ cathode as shown in Fig. 3(b). In this situation, latch-up of the structure occurs.

Conductivity modulation in the LTGBT has been designed to occur not only in the n-epi drift region, but also deeper into the epi and the p-substrate. This is because electrons flowing through the vertical channel travel deeper into the bulk. The holes recombining with the electrons there will

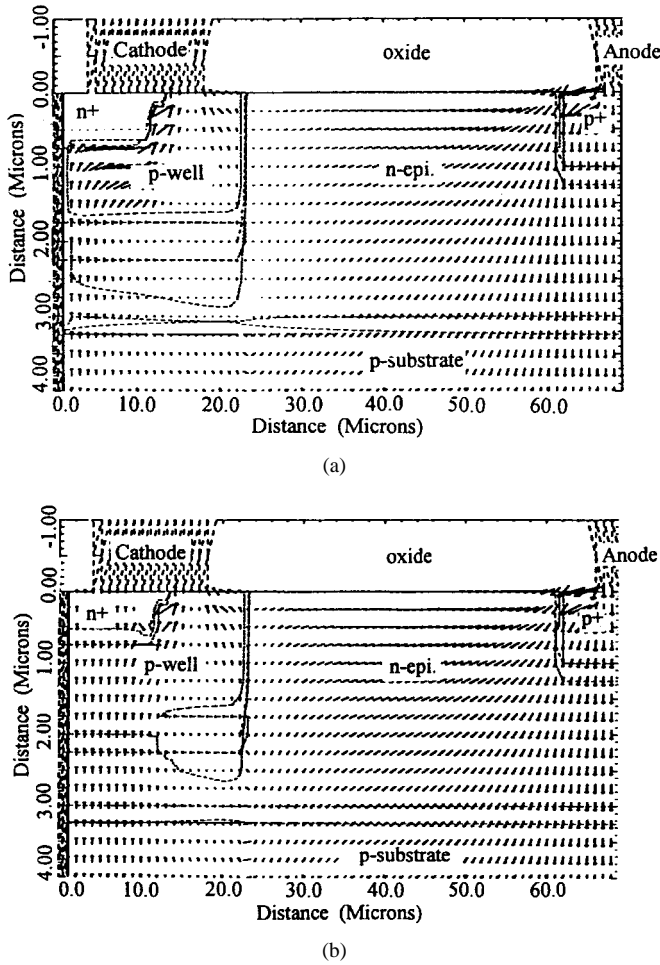


Fig. 3. Hole current vectors at forward voltage of (a) 1.8 V and (b) 3.6 V (after latch-up) for the LTGBT with an n^+ cathode length of 12 μm .

also take a vertical path. These electrons recombine with the large population of holes injected from the anode. This makes conductivity modulation more effective in the epi and in the bulk, resulting in a lower on-state resistance. However, this will not occur until the bias at the anode is high enough so that excess amount of holes can be injected into the bulk. Before this happens, on-resistance of the device is indeed larger due to the longer distance that the electrons have to travel deeper into the bulk through the vertical channel.

For comparison, the simulated current-voltage ($I-V$) characteristics of the LIGBT and LTGBT are shown in Fig. 4. At a on-state current density of 155 A/cm^2 and at a gate bias of 20 V, the forward voltages of the LIGBT and LTGBT are the same (2.6 V). As the anode voltage is less than 2.6 V, the LTGBT has a lower current handling capability compared to the LIGBT. This is due to the fact that the electrons flowing in through the vertical channel travel a longer distance deep into the bulk before recombination as mentioned earlier. When the anode voltage is larger than 2.6 V, the forward conduction characteristics of the LTGBT is better than that of the LIGBT. In this situation, electron injection from the channel will be significant and conductivity modulation in the n-epi and the bulk will be much stronger than that in the LIGBT structure, resulting in higher current handling capability. As shown

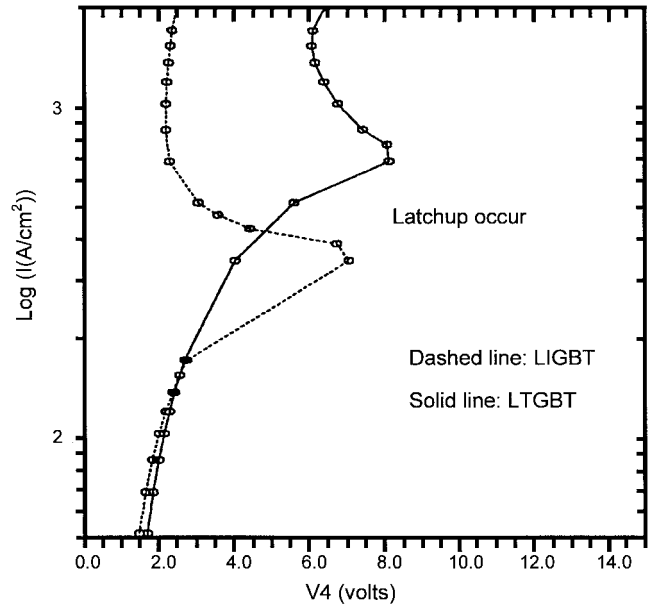


Fig. 4. Simulated forward conduction characteristics of the LTGBT and LIGBT.

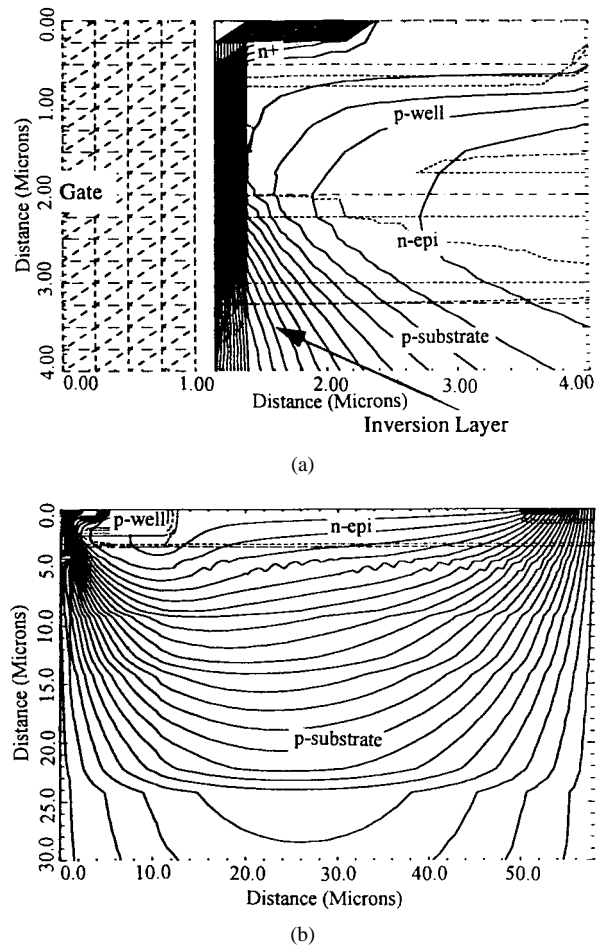


Fig. 5. Simulated current flow-lines in the LTGBT structure. (a) View closer to the trench-gate. (b) View including substrate.

by the current flow-lines of the LTGBT structure in Fig. 5, injection of electrons from the vertical channel is obvious [Fig. 5(a)] and more current flows to the bottom of the n-epi [Fig. 5(b)].

It is noted that, from Fig. 4, the static latch-up current densities of the LIGBT and LTGBT at the same n^+ cathode length of $5 \mu\text{m}$ are approximately 300 A/cm^2 and over 700 A/cm^2 , respectively. In the simulation, the LTGBT and LIGBT have the same p-well length ($10 \mu\text{m}$) and p^+ to n^+ cathode overlap length ($2 \mu\text{m}$). This static latch-up current density comparison exhibits a 2.3 times improvement in the LTGBT. The simulation results on the dynamic latch-up current density during the turn-off transient, with an inductive load of $200 \mu\text{H}$ connected at the anode, are 152 A/cm^2 for the LIGBT and over 640 A/cm^2 for the LTGBT. The dynamic latch-up current density is defined as the maximum current level that the device can be switched off in the way described above without the lose of gate control. The simulated dynamic latch-up current density of the LTGBT exhibits a 4.2 times improvement over the LIGBT. The simulated breakdown voltage of the device is approximately 280 V without the use of an n-buffer surrounding the p^+ anode and 540 V with the n-buffer.

IV. FABRICATION PROCESS

The LTGBT's were fabricated on p-type substrate with a $3\text{-}\mu\text{m}$ thick n-type epi layer. Resistivities of the epi and substrate are $20 \Omega\text{-cm}$ and $45 \Omega\text{-cm}$, respectively. A drift implant of approximately $1 \times 10^{12} \text{ cm}^{-2}$ of phosphorus was used to achieve the RESURF (reduced surface field) condition. After the p-well implantation and drive-in, the anode and cathode regions were formed by boron and arsenic diffusions, respectively. LTO and photoresist were used as mask for trench etching. The trench was produced using the RIE, and the trench depth is $5 \mu\text{m}$. The trench gate oxide was formed using the double oxide process, and the first gate oxide was treated as sacrificial oxide. After a gate oxide growth of 800 \AA , polysilicon *in situ* doped with phosphorus is used to refill the trench. The LTGBT's has a drift length of $40 \mu\text{m}$, a channel length of about $1.5 \mu\text{m}$, and a p-well length of $21 \mu\text{m}$. Threshold voltage and breakdown voltage of the LTGBT's were approximately 1.5 V and 270 V , respectively. The breakdown voltage of 270 V is due to the fact that the n-buffer surrounding the p^+ anode was not incorporated in the device. This breakdown voltage agrees with the simulation result. The thin epi layer used for the LTGBT fabrication is for process compatible to low voltage CMOS process.

V. EXPERIMENTAL RESULTS

Fig. 6 shows the measured $I-V$ characteristics of the LTGBT with an n^+ cathode length of $10 \mu\text{m}$ and a p^+ to n^+ cathode overlap length of $7 \mu\text{m}$. Onset voltage of the device is at approximately 1.2 V . The onset voltage is defined here as threshold at which the drain diode is turned on.

To characterize the latch-up sensitivity to the overlap lengths, LTGBT with different p^+ and n^+ cathode overlap lengths have been designed. The measured static latch-up current densities for different overlap lengths with a gate bias of 20 V and a constant n^+ cathode length of $10 \mu\text{m}$ are shown in Fig. 7. It is shown that the latch-up current density increases as the amount of overlap increases. This is expected since the effective n^+ cathode length reduces at larger overlap,

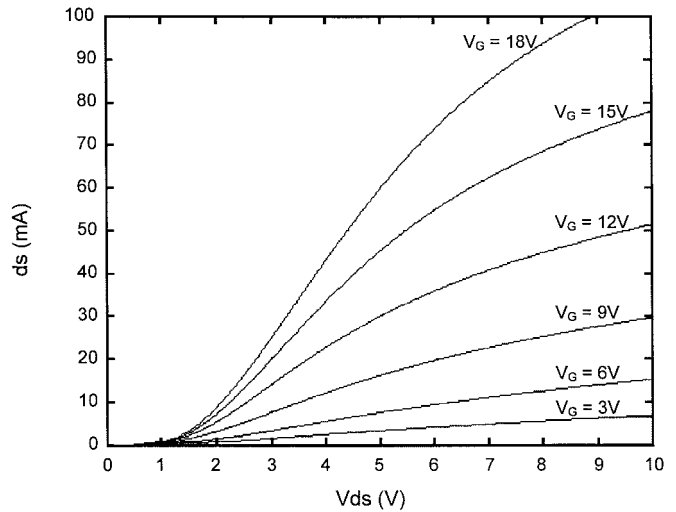


Fig. 6. Experimental $I-V$ characteristics of the LTGBT.

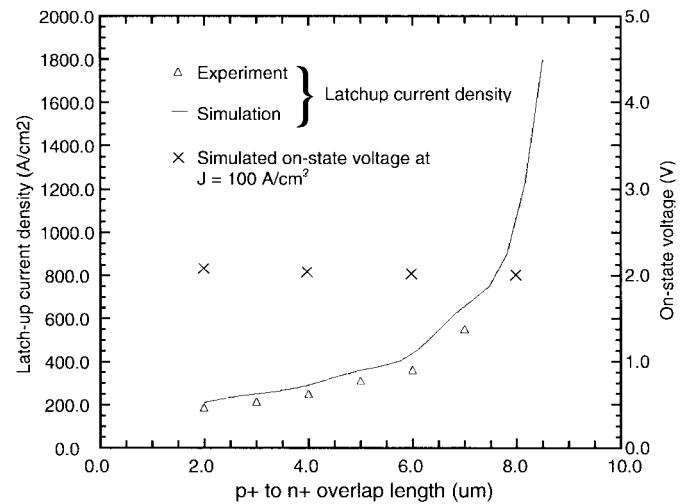


Fig. 7. Experimental and simulated latch-up current density as a function of overlap lengths of the n^+ and p^+ cathodes.

resulting in a smaller biasing resistance underneath for causing latch-up. Specifically, when the n^+ effective cathode length is reduced to $2 \mu\text{m}$, result show that no latch-up occurs, and the current in the structure tends to saturate with increasing anode voltage, even at an anode voltage of 100 V . Along with the experimental results, the simulation results are also shown. The experimental results agree well with the simulations. Furthermore, threshold voltage of the experimental LTGBT is increased from 1.5 V to 2.3 V . The remarkable improvement on the latch-up performance is obtained at the expense of an 0.8 V increase in the threshold voltage. From the simulation results shown in Fig. 7, the latch-up current density is at approximately 1100 A/cm^2 for the overlap length of $8 \mu\text{m}$. The corresponding anode voltage is 225 V . In addition, it is noted that the latch-up current density increases rapidly when the overlap length increases to more than $8 \mu\text{m}$. It is believed that the rapid increase in latch-up current density is due to the electric field shielding formed between the trench-gate depletion region and the p^+ cathode, which prevents holes to flow into the area underneath the n^+ cathode to cause latch-

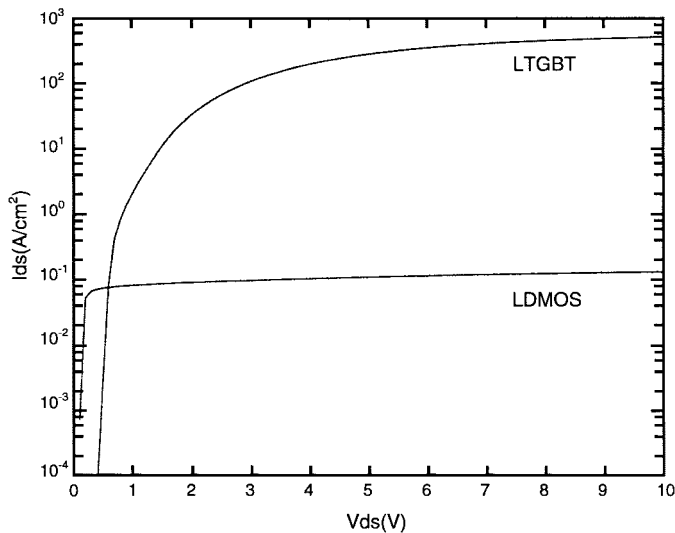


Fig. 8. Experimental I - V characteristics of the LTGBT and trench-gate LDMOS.

up. The simulated on-state voltage as a function of p^+ to n^+ overlap at a constant on-state current density of 100 A/cm^2 is also shown in Fig. 7. The on-state voltage is essentially constant at different p^+ to n^+ overlap lengths.

The measured forward conduction characteristics of the LTGBT along with those of the trench gate LDMOS transistor are shown in Fig. 8. It is observed that the LTGBT has over three orders of magnitude higher forward current density than that of the LDMOS transistor. This comparison is just used to demonstrate that the LTGBT does provide significant conductivity modulation. The absolute value of the comparison is not important since the trench gate LDMOS transistor implemented here is not a favorable structure. Since the LIGBT fabrication process is not compatible to the LTGBT process, no experimental LIGBT device was obtained.

VI. CONCLUSION

A new conductivity modulated power transistor, called the LTGBT, was proposed. Its performance has been characterized. With the trench gate situated behind the cathode and the effective length of the n^+ cathode minimized, holes can be collected by the cathode effectively without causing latch-up even at high current level. The static and dynamic latch-up current densities for the LTGBT exhibit 2.3 times and 4.2 times improvement over those of the LIGBT at the same n^+ cathode length of $5 \mu\text{m}$. Furthermore, the dependence of the latch-up characteristics on the effective n^+ cathode length has been elucidated. It is demonstrated that a smaller effective n^+ cathode length offers a higher latch-up current density. The maximum controllable latch-up current is not limited by the n^+ cathode length but by the effective n^+ cathode length, which can be made very small by increasing the overlap between the n^+ and p^+ cathode diffusions. As the effective n^+ cathode length decreases to $2 \mu\text{m}$, no latch-up was observed in the experimental device. This remarkable improvement in the latch-up performance is accomplished at the expense of a 0.8 V increase in the threshold voltage. Finally, the electron

injection from the vertical channel enhances the conductivity modulation effect in the n -epi and p -substrate regions which in turn improves the forward conduction characteristics of the LTGBT over the LIGBT.

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Jun Cai, photograph and biography not available at the time of publication.

Johnny K. O. Sin (S'79-M'88-SM'96), for a photograph and biography, see this issue, p. 1787.



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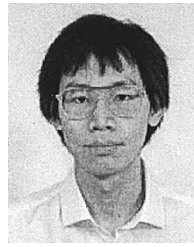
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