Dynamic-Stress-Induced Enhanced Degradation of $1/f$ Noise in n-MOSFET's

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***Abstract*—AC-stress-induced degradation of $1/f$ noise is investigated for n-MOSFET's with thermal oxide or nitrided oxide as gate dielectric, and the physical mechanisms involved are analyzed. It is found that the degradation of $1/f$ noise under ac stress is far more serious than that under dc stress. For an ac stress of $V_G = 0 \sim 0.5V_D$, generations of both interface states (ΔD_{it}) and neutral electron traps (ΔN_{et}) are responsible for the increase of $1/f$ noise, with the former being dominant. For another ac stress of $V_G = 0 \sim V_D$, a large increase of $1/f$ noise is observed for the thermal-oxide device, and is attributed to enhanced ΔN_{et} and generation of another specie of electron traps, plus a small amount of ΔD_{it}. Moreover, under the two types of ac stress conditions, much smaller degradation of $1/f$ noise is observed for the nitrided device due to considerably improved oxide/Si interface and near-interface oxide qualities associated with interfacial nitrogen incorporation.**

***Index Terms*—$1/f$ noise, AC hot-carrier stress, dynamic stress, MOSFET's, nitridation.**

I. Introduction

THE $1/f$ noise characteristics of MOSFET's are very important because the capability of integrating low-noise analog circuits and high-speed digital circuits on the same chip is crucial to the production of a wide range of high-performance MOS integrated circuits. Therefore, extensive study on degradation of $1/f$ noise under various kinds of hot-carrier stresses has been made [1]–[3] and different degradations of $1/f$ noise for different hot-carrier stresses were found [4], [5]. However, to our knowledge, these experimental studies concerned only dc hot-carrier stresses, while MOSFET's in real circuits are exposed to transient gate-and drain-voltage conditions. It is therefore more meaningful to investigate ac hot-carrier-induced degradation of $1/f$ noise. In this work, two typical ac stress conditions with V_G pulsed between 0 and 0.5 V_D or 0 and V_D are used to investigate the degradation behaviors of $1/f$ noise for n-MOSFET's with thermal oxide or nitrided oxide as gate dielectric. Frequency-and duty-cycle-dependent degradations of $1/f$ noise are also examined and the physical mechanisms involved are discussed. It is observed that, although the ac hot-carrier stresses induce a larger noise degradation than dc hot-carrier stresses for thermal-oxide device, significantly improved $1/f$ noise properties are obtained for nitrided devices.

Manuscript received October 5, 1998; revised May 3, 1999. This work was supported by The University of Hong Kong under the RGC and CRCG Research Grants. The review of this paper was arranged by Editor D. P. Verret.

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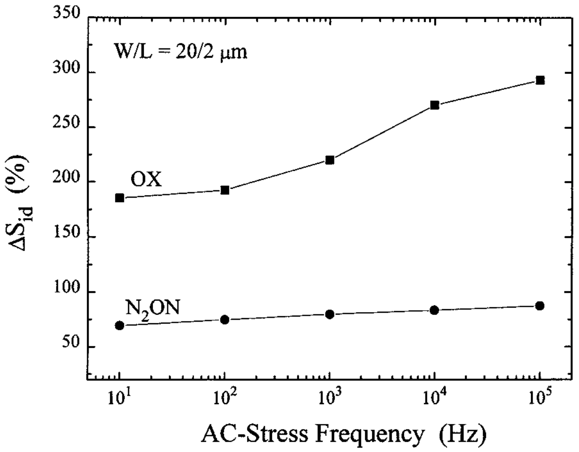
Publisher Item Identifier S 0018-9383(00)00155-6.

II. Experiments

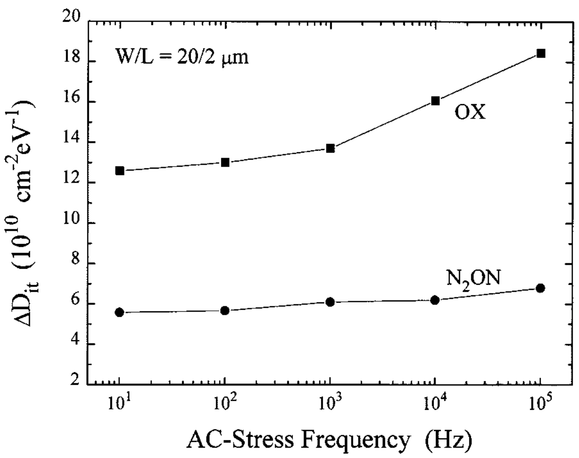
The n-channel MOSFET's used in this study were fabricated on p-type (100) silicon wafers with a resistivity of 6–8 Ω-cm by a self-aligned n^+ polysilicon gate process. After the channel region was implanted by B^+ through a sacrificial oxide which was then stripped, thermal gate oxide (OX) was grown at 850 °C for 70 min in dry O_2. N_2O-nitrided oxide (N_2ON) was obtained by annealing a thinner thermal oxide (grown at 850 °C for 60 min in dry O_2) at 950 °C for 20 min in pure N_2O ambient so as to achieve the same thickness. The two gate oxides were finally annealed in N_2 at 950 °C for 25 min. Final thickness measured by capacitance–voltage technique was about 160 Å for both oxides. Aluminum was thermally evaporated, and then patterned, followed by a forming gas anneal at 410 °C for 30 min. Two ac hot-carrier stresses (gate voltage V_G pulsed between $V_{Gi} = 0$ V and $V_{Gh} = 4$ or 8 V, a fixed drain voltage $V_D = 8$ V, source and substrate grounded) were, respectively, applied on n-MOSFET's with channel width W/length L of 20 μm/2 μm and 10 μm/3 μm to investigate the degradation behaviors of $1/f$ noise. Since experimental data of the latter were similar to that of the former, only the results of the former were reported below. A unipolar square waveform was supplied by HP41501A pulse generator expander with built-in filter function, which suppressed possible voltage overshoot (the maximum value was 230 mV when $V_{Gh} = 8$ V and $f = 100$ kHz). The $1/f$ noise was measured at 50 Hz using HP 35665A dynamic signal analyzer, BTA 9603 FET noise analyzer, and HP 4145B semiconductor parameter analyzer in the linear region of device operation ($V_D = 0.2$ V) for a gate overdrive voltage $V_G^* = V_G – V_T = 0.5$ V (V_T is the threshold voltage). Moreover, a charge-pumping (CP) technique, which varied pulse base level to drive the silicon surface from accumulation to inversion while keeping the amplitude of the pulse constant ($\Delta V_G = 5$ V) with reverse-biased source and drain (0.1 V), was also used to obtain information on interface-state density.

III. Results and Discussion

The $1/f$ noise is characterized by the noise power (S_{id}) of drain current which is derived from a unified $1/f$ noise model incorporating both number fluctuation and surface mobility fluctuation [6]. Fig. 1(a) shows the percentage S_{id} degradation (ΔS_{id}) for n-MOSFET's after a 3000-s ac stress at $V_D =$ 8 V, V_G pulsed between $V_{Gi} = 0$ V and $V_{Gh} = 4$ V with



(a)



(b)

Fig. 1. Frequency dependence of (a) $1/f$ noise degradation and (b) interface-state generation after a 3000-s ac stress with $V_D = 8$ V and V_G pulsed between $V_{Gl} = 0$ V and $V_{Gh} = 4$ V. Rise/fall times of the gate pulse are 200 ns with 50% duty cycle. Noise measurement conditions are $f = 50$ Hz, $V_D = 0.2$ V and $V_G^* = 0.5$ V. The corresponding dc stress-induced S_{id}/D_{it} degradations at $V_D = 2\ V_G = 8$ V are 181%/11.4 × 10^{10} cm^{-2} eV^{-1} for OX sample and 65%/5.4 × 10^{10} cm^{-2} eV^{-1} for N_2ON sample.

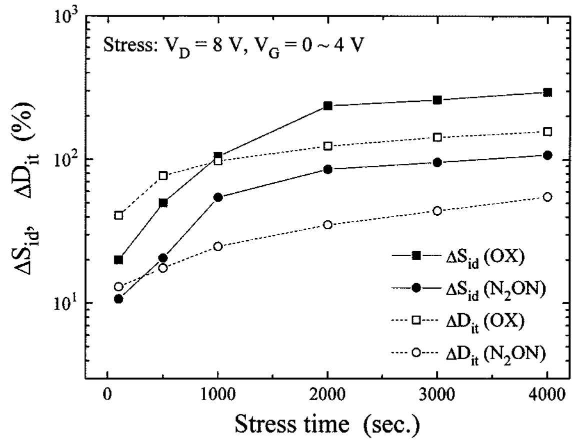


Fig. 2. Degradation of $1/f$ noise as a function of stress time under the same ac stress voltage conditions as that in Fig. 1 at a frequency of 10^4 Hz with 50% duty cycle. Noise measurement conditions are same as that in Fig. 1.

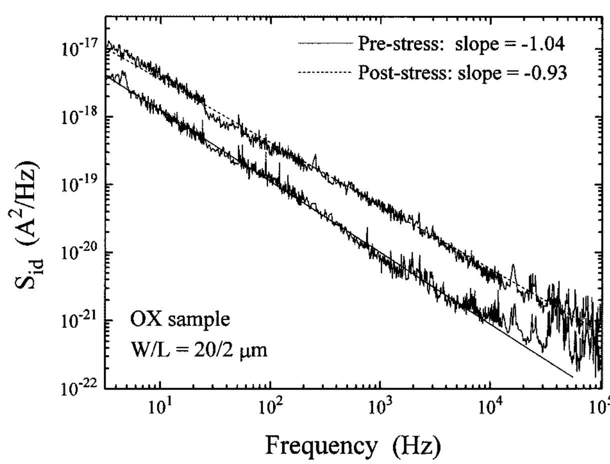


Fig. 3. Drain-current noise power spectrum of OX sample before and after a 3000-s ac stress at $f = 10^4$ Hz under the same conditions as Fig. 1. The error of extracted slope values is ±0.003.

rise/fall times of 200 ns and 50% duty cycle. The corresponding dc-stress-induced degradations at $V_D = 2V_G = 8$ V, which is mainly associated with interface-state generation under maximum substrate current [7], are 181% for OX sample and 65% for N_2ON sample. It can be seen that ac stress-induced ΔS_{id} increases with frequency and is larger than dc stress-induced ΔS_{id}, especially for $f > 10^3$ Hz. Similar frequency dependence of increased interface-state density measured by CP technique is also observed, as shown in Fig. 1(b). This is consistent with the results in [8]. As a result, ΔD_{it} should be mainly responsible for ΔS_{id}, while other factors should be hole trapping and generation of neutral electron traps near the interface due to the presence of the low-V_G half cycle during the ac stress with V_D fixed at high voltage [9], [10]This is supported by the larger value of ΔS_{id} than that of ΔD_{it} measured at $f = 10^4$ Hz, as shown in Fig. 2. Furthermore, the drain-current noise power spectrum of OX sample is measured before and after a 3000-s ac stress at $f = 10^4$ Hz under the same conditions as in Fig. 1. As can be seen from Fig. 3, the measured low-frequency noise is indeed a $1/f$ noise with a slope of −1.04 (prestress) or −0.93 (post-stress). A reduction of the slope after the stress implies a nonuniform generation of interface and near-interface traps, i.e., generation of high-frequency traps (traps close to the interface) is more than that of low-frequency traps (traps away from the interface). Therefore, a larger degradation of $1/f$ noise occurs at the high-frequency end than at the low-frequency end. In addition, it is worth pointing out that in the initial stage of the ac stress in Fig. 2, ΔS_{id} is even smaller than ΔD_{it}. This is probably because most initially created interface states lies at the interface (fast interface states) so that fluctuation in the number of channel carriers due to tunneling between the interface states and the inversion layer is too quick to be detected in the typical frequency range of noise measurements [11]. Moreover, ΔN_{et} is also small in the initial stage. For longer stress time, besides a large ΔD_{it} including both fast interface states and near-interface oxide traps (the two are indistinguishable in CP measurement, but the latter can be detected by noise measurement [11]), hole trapping and generation of neutral electron traps become also serious, thus resulting in ΔS_{id} larger than ΔD_{it}. Compared to OX sample, N_2ON sample exhibits greatly suppressed ΔS_{id} due to hardened oxide/Si interface and near-interface oxide

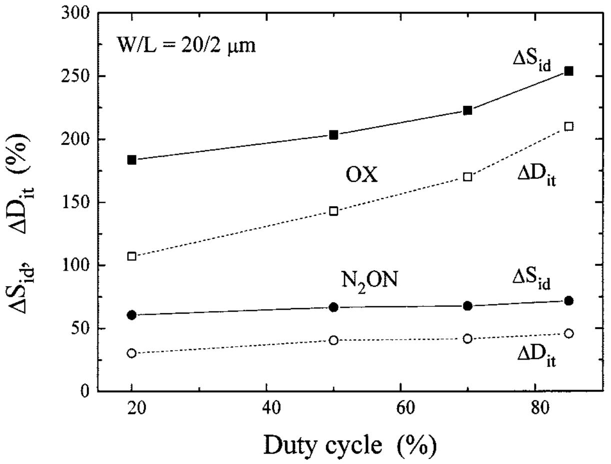


Fig. 4. Duty-cycle dependence of $1/f$ noise degradation under an ac stress with $V_D = 8$ V and V_G pulsed between $V_{Gl} = 0$ V and $V_{Gh} = 4$ V at a frequency of 10^4 Hz. Rise/fall times of the gate pulse are 200 ns. Noise measurement conditions are same as that in Fig. 1.

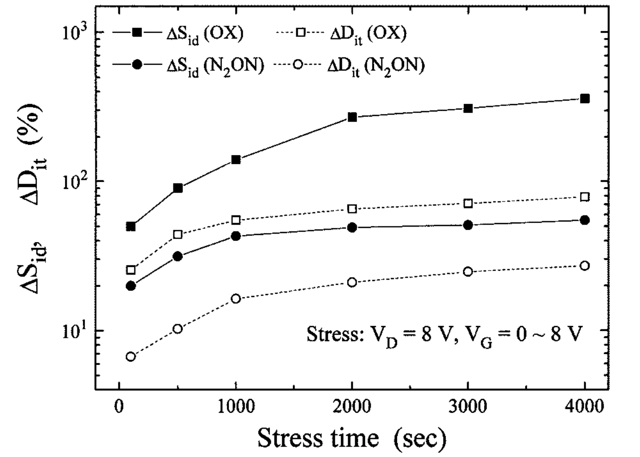


Fig. 5. Degradation of $1/f$ noise as a function of stress time under an ac stress with $V_D = 8$ V and V_G pulsed between $V_{Gl} = 0$ V and $V_{Gh} = 8$ V at a frequency of 10^4 Hz. Rise/fall times of the gate pulse are 200 ns with 50% duty cycle. Noise measurement conditions are same as that in Fig. 1.

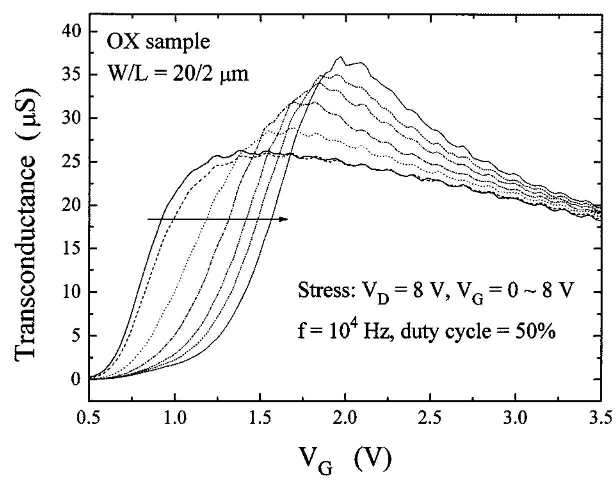


Fig. 6. Transconductance characteristics of OX device under the ac stress conditions in Fig. 4. Along the arrow direction, stress time is 0, 100, 500, 1000, 2000, 3000, and 4000 s.

resulting from N_2O nitridation and thus smaller ΔD_{it} and ΔN_{et}. Based on the above discussion, it can be concluded that ΔS_{id} induced by ac stress at $V_G = 0$–4 V and $V_D = 8$ V is a combined effect of ΔD_{it} and ΔN_{et}.

To further clarify the impacts of ΔD_{it} and ΔN_{et} on ΔS_{id}, duty-cycle dependence of $1/f$ noise degradation is examined under an ac stress for 2000 s at $V_D = 8$ V and $V_G = 0$ 4 V with $f = 10^4$ Hz and rise/fall times of 200 ns, and the results are depicted in Fig. 4. For OX sample, ΔS_{id} increases significantly with duty cycle, while a weak dependence of ΔS_{id} on duty cycle is found for N_2ON sample. As mentioned above, there is neutral electron-trap generation in the low-V_G portion of a cycle and interface-state generation in the high-V_G portion of a cycle. So, for larger duty cycle, the stress condition of $V_D = 2V_G = 8$ V occurs for a larger fraction of the total ac stress duration, yielding larger ΔD_{it}, while ΔN_{et} dominates for small duty cycles. This fact is well illustrated by the gradual closeness of ΔD_{it} to ΔS_{id} at larger duty cycles. However, ΔD_{it} of N_2ON sample is hardly sensitive to duty cycle due to considerably enhanced interface hardness against hot-carrier bombardment, and thus a weak duty-cycle dependence of ΔS_{id} results. In view of the above analysis and further comparing the ΔS_{id} values at the two ends of duty cycle, it can be believed that ΔS_{id} is influenced to a larger extent by ΔD_{it} than ΔN_{et}, at least for duty cycles ≥ 50%.

Presented in Fig. 5 is another ac stress-induced degradation of S_{id} when V_G is pulsed between a wider range (0–8 V) with other conditions same as those in Fig. 2. Surprisingly, in the whole stress duration, a larger ΔS_{id} of OX sample is induced by the ac stress as compared to the stress in Fig. 2, while the opposite holds for N_2ON sample, with both devices displaying smaller ΔD_{it}. This can be explained as followings. Like the previous ac stress, in the low-V_G half cycle, there are hole trapping and ΔN_{et}. Since N_{et} is believed to be created through the recombination of injected electrons and trapped holes [12], an enhanced ΔN_{et} should result due to $V_{Gh} = V_D = 8$ V in this ac stress, which can lead to a large amount of electron injection [7]. Moreover, under this ac stress, another specie of electron traps can also be created by the injected hot electrons, with its physical or microscopic nature different from the one created by hot holes at low gate voltage [13]. All these happen in the gate oxide close to the oxide/Si interface near the drain. So, a damaged region near the drain is easily formed when all these electron trap generation/trapping are serious. This is true for OX sample as demonstrated by its transconductance behaviors in Fig. 6, because its peak linear transconductance G_m increases and the curve shifts to higher V_G (implying higher V_T) as the ac stress progresses. This is just an indication of gradual formation of a damaged region near the drain [14]. Therefore, it can be deduced that a large amount of generated electron traps along with ΔD_{it} cause a large carrier-number fluctuation and thus a large ΔS_{id} under the ac stress of $V_D = 8$ V and $V_G = 0$–8 V. However, for N_2ON sample, owing to nitrogen incorporation near its oxide/Si interface which introduces stronger Si–N bonds ($E_{Si\text{–}N}$~ 4.6 eV) [15], [16] and relaxes interfacial strained Si–O bonds [17], the two kinds of electron-trap generations and ΔD_{it} are considerably suppressed and no damaged region is formed near the drain, thus resulting in a much smaller ΔS_{id} as observed in Fig. 5.

IV. Summary

Degradation behaviors of $1/f$ noise under dynamic stress are investigated for n-MOSFET's with nitrided oxide or thermal oxide as gate dielectric. Compared to static stress, dynamic stress results in a larger increase of $1/f$ noise. This is because not only interface states but also electron traps are created during dynamic stress. However, nitrided devices show significantly improved immunity to dynamic stress-induced degradation in $1/f$ noise due to nitrogen incorporation near the oxide/Si interface which hardens the interface and near-interface oxide, and thus suppresses generations of interface states and electron traps.

References

[1] Z. H. Fang, S. Christoloveanu, and A. Chovet, "Analysis of hot-carrier-induced aging from $1/f$ noise in short-channel MOSFET's," *IEEE Electron Device Lett.*, vol. EDL-7, pp. 371–373, June 1986.

[2] C. H. Cheng and C. Surya, "The effect of hot-electron injection on the properties of flicker noise in n-channel MOSFET's," *Solid State Electron.*, vol. 36, p. 475, 1993.

[3] P. K. Hurley, E. Sheehan, S. Moran, and A. Mathewson, "The impact of oxide degradation on the low-frequency $(1/f)$ noise behavior of p-channel MOSFET," *Microelectron. Reliab.*, vol. 36, no. 11/12, pp. 1679–1682, 1996.

[4] J. M. Pimbley and G. Gildenblat, "Effect of hot-carrier stress on low frequency MOSFET noise," *IEEE Electron Device Lett.*, vol. EDL-5, p. 345, 1984.

[5] M. Aoki and M. Kato, "Hole-induced $1/f$ noise increase in MOS transistors," *IEEE Electron Device Lett.*, vol. 17, p. 118, 1996.

[6] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors," *IEEE Trans. Electron Devices*, vol. 37, p. 654, 1990.

[7] B. Doyle, M. Bourcerie, J. C. Marchetaux, and A. Boudou, "Interface state creation and charge trapping in the medium-to-high gate voltage range during hot-carrier stressing of n-MOS transistors," *IEEE Trans. Electron Devices*, vol. 37, pp. 744–754, Mar. 1990.

[8] C. Hu, "AC effects in IC reliability," *Microelectron. Reliab.*, vol. 36, no. 11/12, pp. 1611–1617, 1996.

[9] K. R. Doyle and B. S. Doyle, "AC verse DC hot-carrier degradation in n-channel MOSFET's," *IEEE Trans. Electron Devices*, vol. 40, p. 96, 1993.

[10] E. Takeda, R. Izawa, K. Umeda, and R. Nagai, "AC hot-carrier effects in scaled MOS devices," in *Proc. IEEE Int. Rel. Phys. Symp.*, 1991, p. 118.

[11] R. Jayaraman and C. Sodini, "$1/f$ noise interpretation of the effect of gate oxide nitridation and reoxidation on dielectric trap," *IEEE Trans. Electron Devices*, vol. 37, p. 305, 1990.

[12] I. Chen, S. Holland, and C. Hu, "Electron trap generation by recombination of electrons and holes in SiO_2," *J. Appl. Phys.*, vol. 61, p. 4544, 1987.

[13] W. Weber, M. Brox, R. Thewes, and N. S. Saks, "Hot-hole-induced negative oxide charges in n-MOSFET's," *IEEE Trans. Electron Devices*, vol. 42, p. 1473, 1995.

[14] C. Nguyen-Duc, S. Cristoloveanu, and G. Reimbold, "Effects of localized interface defects caused by hot-carrier stress in n-channel MOSFET's at low-temperature," *IEEE Electron Device Lett.*, vol. 9, pp. 479–481, Sept. 1988.

[15] T. Hori, H. Iwasaki, and K. Tsuji, "Electrical and physical characteristics of ultrathin reoxidized nitrided oxides prepared by rapid thermal processing," *IEEE Trans. Electron Devices*, vol. 36, p. 340, 1989.

[16] T. Y. Chu, W. Ting, J. H. Ahn, S. Lin, and D. L. Kwong, "Study of the composition of thin dielectrics grown on Si in a pure N_2O ambient," *Appl. Phys. Lett.*, vol. 59, p. 1412, 1991.

[17] R. P. Vasquez and A. Madhukar, "Strain-dependent defect formation kinetics and a correlation between flatband voltage and nitrogen distribution in thermally nitrided SiO_xN_y/Si structures," *Appl. Phys. Lett.*, vol. 47, p. 998, 1985.

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