Effects of Wet N_2O Oxidation on Interface Properties of 6H-SiC MOS Capacitors

P. T. Lai, *Member, IEEE*, J. P. Xu, and C. L. Chan

***Abstract*—Oxynitrides were grown on n- and p-type 6H-SiC by wet N_2O oxidation (bubbling N_2O gas through deionized water at 95°C) or dry N_2O oxidation followed by wet N_2O oxidation. Their oxide/SiC interfaces were investigated for fresh and stressed devices. It was found that both processes improve p-SiC/oxide but deteriorate n-SiC/oxide interface properties when compared to dry N_2O oxidation alone. The involved mechanism could be enhanced removal of unwanted carbon compounds near the interface due to the wet ambient, and hence a reduction of donor-like interface states for the p-type devices. As for the n-type devices, incorporation of hydrogen-related species near the interface under the wet ambient increases acceptor-like interface states. In summary, the wet N_2O oxidation can be used for providing comparable reliability for n- and p-SiC MOS devices, and especially obtaining high-quality oxide-SiC interface in p-type MOS devices.**

***Index Terms*—Interface-state density, MOS capacitors, silicon carbide, wet N_2O oxidation.**

I. Introduction

THERE has been considerable progress in improving qualities of oxide on SiC and oxide/SiC interface, mainly based on nitridation processes. Although N_2O-annealed oxides showed an increase in interface-state density [1], [2], NO-annealed oxides exhibited improved electrical properties: reduced interface-state density [1]–[4], enhanced reliability [5], and increased channel-carrier mobility [6]. Recently, oxynitrides directly grown in N_2O [7] and NO [8] showed better oxide/SiC interface and bulk properties than their respective counterparts annealed in the same gas. However, an obvious problem is that nitridation-induced improvements of n-SiC and p-SiC interface characteristics are different, usually with the former larger than the latter. In this work, the effects of N_2O oxidation in a wet ambient on the interface properties and reliability of n- and p-SiC MOS devices are investigated. When compared with the dry N_2O oxidation, an opposite phenomenon is observed. Wet N_2O oxidation improves p-SiC/oxide but deteriorates n-SiC/oxide interface properties. Moreover, experimental results show that a dry-wet N_2O oxidation can be used to obtain comparable reliability for n-channel and p-channel SiC MOS devices. In this letter, relevant results are reported and physical mechanisms involved are analyzed.

II. Experiments

N- and p-type (0001) Si-face 6H-SiC wafers, manufactured by CREE Research, were used in this study. The SiC wafers had a 5-μm epitaxial layer grown on heavily doped substrates (i.e., n/n^+ and p/p^+). The doping level of the epitaxial layer was 4×10^{15} cm^{-3} for both types. The wafers were cleaned using the conventional RCA method followed by a 1-min dip in 5% HF, and then loaded into a quartz furnace at 800°C. After raising the temperature to 1150°C, a 4-h oxidation was carried out in a dry pure N_2O (denoted as DN2OG sample) or a wet N_2O ambient by bubbling pure N_2O gas through de-ionized water at 95°C (denoted as WN2OG sample), both at a flow rate of 500 ml/min. The third sample was oxidized first in dry pure N_2O for 2.5 h and then in wet N_2O for 1.5 h at the same temperature and flow rate (denoted as DWN2OG). After cooling down in N_2 with a ramping rate of $-1^\circ C/\min$ to 950°C, all samples were subjected to postoxidation annealing in N_2 at a flow of 1.0 l/min for 0.5 h. Finally, aluminum was thermally evaporated, and then patterned to form gate electrodes, each with an area of 1.14×10^{-3} cm^2. This step was followed by a forming gas anneal at 410°C for 30 min. High-frequency (HF, 1 MHz) capacitance–voltage (C–V) characteristics were measured using HP4284A LCR meter at room temperature with a bias sweep rate of 0.1 V/s and a small signal amplitude of 20 mV. Accumulation capacitance, flat-band voltage, equivalent oxide charge and average interface-state density were extracted from the HF capacitance–voltage (C–V) curves. High-field stress (±7 MV/cm) applied by HP4156B precision semiconductor parameter analyzer, with the capacitors biased in accumulation, was used to examine device reliability in terms of the flat-band voltage shift ($\Delta V_{\rm fb}$). Stress times were 10, 100, 500, 1000, 2000, 3000, and 5000 s. All measurements were carried out under a light-tight and electrically-shielded condition.

III. Results and Discussion

Fig. 1(a) and (b) show typical HF C–V curves under the dark condition for n- and p-type 6H-SiC MOS capacitors fabricated using different processing conditions. Some parameters extracted from these HF C–V curves are listed in Table I, where equivalent oxide thickness $t_{\rm ox}$ is calculated from accumulation capacitance (i.e., oxide capacitance $C_{\rm ox}$) using the dielectric constant of SiO_2 (3.9), and flat-band voltage $V_{\rm fb}$ is determined

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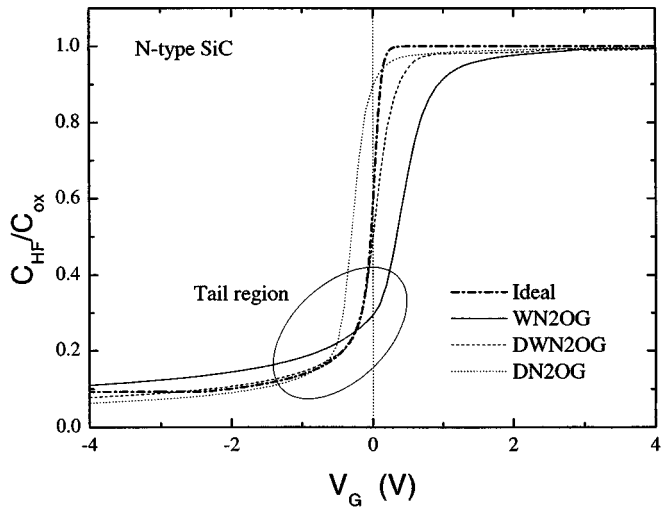
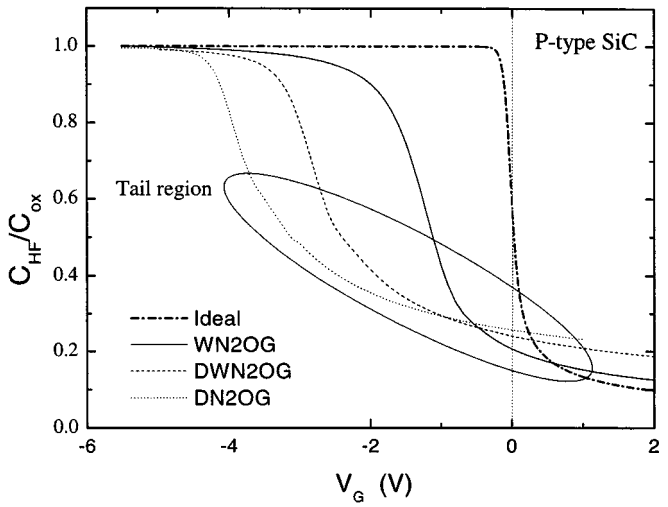


(a)



(b)

Fig. 1. Typical high-frequency C–V curves of the three kinds of capacitors under the dark condition at room temperature. (a) n-type SiC MOS and (b) p-type SiC MOS. Area of capacitor is 1.14×10^{-3} cm^2. For clarity, the ideal curves are shown only for the WN2OG devices.

from the flat-band capacitance $(C_{\rm fb})$ formula [9] modified by replacing the dielectric constant of Si with that of SiC:

$$\frac{C_{\rm fb}}{C_{\rm ox}} = \left(1 + \frac{150\sqrt{\frac{T}{300}}}{t_{\rm ox}\sqrt{N}}\right)^{-1}$$

with T the temperature in Kelvin and the carrier concentration N equal to the acceptor or donor doping as an approximation. Equivalent oxide-charge density is calculated as $Q_{\rm ox} = -C_{\rm ox}(V_{\rm fb} - \phi_{\rm ms})/q$, where the work-function difference $\phi_{\rm ms}$ between aluminum and 6H-SiC is calculated to be 0.031 V for n-type SiC and -2.53 V for p-type SiC. The interface-state density $(D_{\rm it})$ is taken as the average value between 0.5 and 0.6 eV away from the edge of conduction band (n-type SiC) or valence band (p-type SiC), estimated from the HF C–V curve using the Terman method [10]. From Table I and Fig. 1, three points can be summarized: 1) the growth rate of wet N_2O oxidation is higher than that of dry N_2O oxidation, probably due to higher oxidation rate in steam atmosphere than in dry ambient and enhanced out-diffusion of CO (one of the factors limiting the growth rate in wet oxidation [11]); 2) both wet and dry-wet N_2O oxidations shift the C–V curves of the p-type SiC samples in the positive $-V_G$ direction and hence reduce their $|V_{\rm fb}|$; and 3) from the slope of the C–V curve in the depletion region and the size of the tail in the deep-depletion region, it can be deduced that compared with dry N_2O oxidation, wet and dry-wet N_2O oxidations improve the oxide/SiC interface quality for p-type device, but deteriorate the n-type oxide/SiC interface, similar to the results of wet O_2 oxidation on SiC [12], [13]. This is supported by the estimated $D_{\rm it}$'s in Table I.

TABLE I
ELECTRICAL AND PHYSICAL PARAMETERS EXTRACTED FROM HF C–V CURVES. $D_{\rm it}$ IS AN AVERAGE VALUE BETWEEN 0.5 AND 0.6 EV FROM THE EDGE OF THE CONDUCTION BAND (N-TYPE SIC) OR VALENCE BAND (P-TYPE SIC)

	N-type SiC			P-type SiC		
Sample	WN2OG	DWN2OG	DN2OG	WN2OG	DWN2OG	DN2OG
t_{ox} (A)	328	280	246	317	272	240
C_{fb}/C_{ox}	0.58	0.54	0.51	0.57	0.54	0.50
V_{fb} (V)	0.42	0.04	-0.29	-1.23	-2.55	-3.13
$Q_{ox} \times 10^{11}$ cm^{-2}	-2.56	-0.07	2.81	-8.84	0.16	5.39
$D_{it} \times 10^{11}$ cm^{-2}eV^{-1}	4.5	3.1	2.2	3.0	4.2	5.7

It is believed that the interface states in the upper half and lower half of the band gap are quite different (acceptor-like and donor-like, respectively), and originate from dangling bonds and carbon compounds at the interface, respectively [13]. (For acceptor-like interface states, there could be other possible origins, e.g., Si-Si bonds at the interface which induce symmetric defect states at the two band edges [4].) Therefore, as compared with the dry N_2O-grown sample, the improved interface properties of p-type MOS capacitors prepared using wet or dry-wet N_2O oxidation may be associated with the effective removal of unwanted carbon compounds (donor-like interface states) due to two possible effects of the wet ambient: 1) enhanced out-diffusion of CO as mentioned previously and 2) enhanced removal of interstitial carbon as well as carbon clusters by nitridation [14]. On the other hand, the inferior interface quality of n-type MOS capacitors could be attributed to the creation of more acceptor-like interface states in the wet oxidation ambient which is speculated to result from hydrogen-related species such as -OH bonds in the steam [12], [13], [15]. These could be considered as the main reason for the positive flat-band shift of the wet N_2O-oxidized samples, because the increase in the negative fixed oxide charge is negligible compared with the change in the interface states during wet oxidation [12]. Therefore, the more negative $Q_{\rm ox}$ in the WN2OG sample in Table I does not indicate a real increase in the negative fixed oxide charge, but instead indicates a reduction in the donor-like interface states for p-type devices or an increase in the acceptor-like interface states for n-type devices.

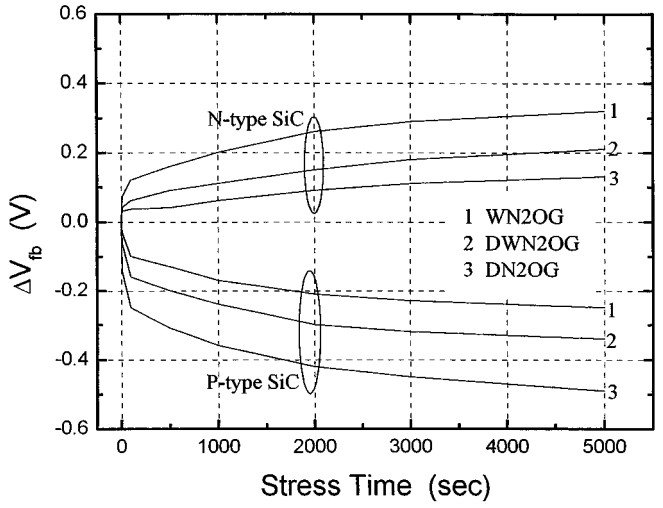


Fig. 2. Flat-band voltage shifts of all samples under high-field stressing (± 7 MV/cm) at room temperature, with capacitors biased in accumulation. Area of capacitor is 1.14×10^{-3} cm^2.

Fig. 2 is the flat-band voltage shift of all samples during high-field stressing (± 7 MV/cm) with their gates biased in accumulation at room temperature. The stress field is determined as $(V_G - V_{\rm fb})/t_{\rm ox}$ to account for the difference in the flat-band voltages of the samples under comparison. It should be noted that the $|\Delta V_{\rm fb}|$'s of all these nitrided samples are approximately $10\times$ smaller than that of a conventional O_2-grown sample [7]. In agreement with the improvement of the interface quality in Fig. 1, the WN2OG sample exhibits the best and worst reliability for p-type and n-type substrates, respectively, with the DWN2OG sample lying in between. Also, there is an opposite change in $V_{\rm fb}$ for p-type and n-type devices, indicating that donor (acceptor)-like interface states and positive (negative) oxide charges are generated in p (n)-type device under the high-field stressing condition. A smaller $|\Delta V_{\rm fb}|$ for p-type WN2OG and DWN2OG samples than the p-type DN2OG sample implies stronger oxide/SiC interface in the former two samples, and thus less generation of donor-like interface states and positive oxide charges. This indicates that a wet ambient is beneficial for the effective removal of carbon-related species as well as the creation of more strong Si $\equiv$ N and N $\equiv$ O bonds. In addition, from Fig. 2, it can be observed that $\Delta V_{\rm fb}$ of both DWN2OG samples always lie between those of WN2OG and DN2OG samples. Therefore, it is possible for the dry-wet N_2O oxidation to produce high-quality p- and n-channel SiC MOS devices with equal reliability, when the times for dry and wet oxidations are properly adjusted.

IV. Summary

Improved p-SiC/oxide interface quality was demonstrated in MOS devices with wet or dry-wet N_2O-grown oxynitride as the gate dielectric. Enhanced reliability of the two p-type SiC MOS devices was also observed under high-field stress. These facts indicate that wet N_2O oxidation is a promising process for the fabrication of high-performance p-SiC MOS devices. Moreover, when the wet N_2O oxidation is combined with dry N_2O oxidation, p-type SiC MOS devices still show improved interface properties, with acceptable degradation in its n-type counterpart. As a result, this can be an efficient approach for improving the interface properties of p- and n-channel SiC MOS devices, and even for achieving identical reliability for both devices.

References

[1] S. Dimitrijev, H.-F. Li, H. B. Harrison, and D. Sweatman, "Nitridation of silicon-dioxide films grown on 6H silicon carbide," *IEEE Electron Device Lett.*, vol. 18, pp. 175–177, May 1997.

[2] S. Dimitrijev, P. Tanner, and H. B. Harrison, "Slow-trap profiling of NO and N_2O nitrided oxides grown on Si and SiC substrates," *Microelectron. Reliab.*, vol. 39, no. 4, pp. 441–449, 1999.

[3] H.-F. Li, S. Dimitrijev, H. B. Harrison, and D. Sweatman, "Interfacial characteristics of N_2O and NO nitrided SiO_2 grown on SiC by rapid thermal processing," *Appl. Phys. Lett.*, vol. 70, no. 15, pp. 2028–2030, 1997.

[4] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, M. Di Ventra, S. T. Pantelides, L. C. Feldman, and R. A. Weller, "Effects of nitric oxide annealing on the interface trap densities near the band edges in the 4H polytype of silicon carbide," *Appl. Phys. Lett.*, vol. 76, no. 13, pp. 1713–1715, 2000.

[5] H.-F. Li, S. Dimitrijev, and H. B. Harrison, "Improved reliability of NO-nitrided SiO_2 grown on p-type 4H-SiC," *IEEE Electron Device Lett.*, vol. 19, pp. 279–281, Aug. 1998.

[6] J. Palmour, *Abs. 3rd Eur. Conf. Silicon Carbide and Related Materials*, 2000, p. 112.

[7] J. P. Xu, P. T. Lai, C. L. Chan, B. Li, and Y. C. Cheng, "Improved performance and reliability of N_2O-grown oxynitride on 6H-SiC," *IEEE Electron Device Lett.*, vol. 21, pp. 298–300, June 2000.

[8] S. Chakraborty and P. T. Lai, "MOS characteristics of NO-grown oxynitrides on n-type 6H-SiC," Microelectron. Reliab., to be published.

[9] D. K. Schroder, *Semiconductor Material and Device Characterization*, 2nd ed. New York: Wiley, 1998.

[10] L. M. Terman, "An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes," *Solid-State Electron.*, vol. 5, pp. 285–299, 1962.

[11] C. Raynaud, "Silica films on silicon carbide: A review of electrical properties and device applications," *J. Non-Cryst. Solids*, vol. 280, pp. 1–31, 2001.

[12] H. Yano, F. Katafuchi, T. Kimoto, and H. Matsunami, "Effects of wet oxidation/anneal on interface properties of thermally oxidized SiO_2/SiC MOS system and MOSFETs," *IEEE Trans. Electron Devices*, vol. 46, pp. 504–510, Mar. 1999.

[13] S. Suzuki, W. J. Cho, R. Kosugi, J. Senzaki, S. Harada, and K. Fukuda, "Influence of the post-oxidation process on the MOS interface and MOSFETs properties," *Mater. Sci. Forum*, vol. 353–356, pp. 643–646, 2001.

[14] P. Tanner, S. Dimitrijev, H. F. Li, D. Sweatman, K. E. Prince, and H. B. Harrison, "SIMS analysis of nitrided oxides grown on 4H-SiC," *J. Electron. Mater.*, vol. 28, no. 2, pp. 109–111, 1999.

[15] H. Yano, T. Kimoto, H. Matsunami, M. Bassler, and G. Pensl, "MOSFET performance of 4H-, 6H-, and 15R-SiC processed by dry and wet oxidation," *Mater. Sci. Forum*, vol. 338–342, pp. 1109–1112, 2000.