A Constant-Power Battery Charger With Inherent Soft Switching and Power Factor Correction

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***Abstract*—A battery charging circuit, which operates as a constant power source, is proposed in this paper. By maintaining a constant output power throughout the charging process, the circuit reduces the size of thermal installation which would normally be required in the cases of constant-voltage or constant-current charging. The proposed circuit takes the form of a half-bridge converter with an additional small inductor and two extra diodes connected in parallel to two dividing capacitors. Constant power delivery is achieved by the discontinuous-voltage-mode operation of the two dividing capacitors, each of which is connected in parallel with a diode. The circuit enjoys low voltage and current stresses, and achieves soft switching with no extra components. When used off-line, the converter maintains a high input power factor and a low level of input current harmonic distortion that meets international regulations. All the above characteristics are determined only by the values of the circuit parameters, the control mechanism being noncritical. A 12 V 65 W prototype was built to demonstrate the merits of this circuit.**

***Index Terms*—Battery charger, power factor correction, switching converters, zero-voltage-switching.**

I. Introduction

BATTERY chargers are designed typically around two modes of operation, namely, *constant-voltage charging* and *constant-current charging*. The former utilizes a constant voltage source and an equivalent series resistance to control the amount of current that flows into the battery. As soon as the battery voltage is raised to the voltage sources, the converter must limit its current to prevent excessive dissipation. The latter, moreover, keeps the charging current constant until the battery voltage reaches a designated value [1]–[5]. For both modes of charging, mandatory thermal design for the power converter is required. Specifically, in constant-voltage charging, the converter dissipates a large amount of thermal power in the equivalent series resistance, mainly during the initial charging phase. Since this highly dissipative charging phase lasts only for a short duration of the entire charging process, the heavy thermal design, though mandatory, is very sparingly utilized. Moreover, in constant-current charging, the converter delivers very high power when the charging process is near completion. Again the high-power charging period only lasts for a short duration of time, the thermal design has a low utilization. In other words, the thermal management for the cases of constant-voltage and constant-current charging must inevitably be over-designed for much of the charging time.

In this paper a circuit topology, which is based on a half-bridge converter topology with an additional small inductor and two diodes connected in parallel with two dividing capacitors, is proposed for battery charging applications. The basic circuit, as studied previously in Pong *et al.* [6] and Poon *et al.* [7], [8], has an inherent power limiting characteristic. Moreover, inherent power factor correction (PFC) or harmonic current reduction can be achieved by operation in discontinuous-voltage mode, as demonstrated in Tse [9]. In the proposed circuit, we combine the merits of the above-mentioned topology and the discontinuous-voltage-mode operation, to achieve a very simple design solution that requires minimal thermal installation for battery charging applications. In addition to PFC, soft switching and low voltage stress can be easily achieved with this circuit topology.

II. Overview of Power Limiting and Resistive Input Characteristics

Fig. 1 shows the schematic of the constant power converter and some waveforms illustrating the circuit operation. The basic configuration is a half-bridge converter with an additional small inductor L_r and two additional diodes connected in parallel to the dividing capacitors C_1 and C_2. The duty cycle is fixed and kept at slightly less than 50% to avoid simultaneous conduction of the two switches. A battery with voltage V_T and equivalent series resistance $R_{\rm os}$ is connected at the output terminals.

The basic operational requirements of the proposed constant power converter are that capacitors C_1 and C_2 work in the discontinuous-voltage mode for a given load current, and that the peak voltage across the secondary winding of T_1 is higher than the battery voltage V_T to allow power flow to the battery. Diodes D_1 and D_2 limit the voltages of capacitors C_1 and C_2 to 0 V (actually -0.7 V), ensuring that the voltage swing of each capacitor is clamped between the positive supply voltage V_i and 0 V.

A main feature of the circuit operation is the discontinuous-voltage-mode operation of the dividing capacitors. When MOSFET M_1 is on (M_2 is off), capacitor C_2 is charged up and capacitor C_1 is discharged. The transformer secondary delivers current to the load during this time. As the voltage swing of C_1 and C_2 is clamped by diodes D_1 and D_2, the voltage at node B will finally reach V_i and be clamped at this value. Similarly,

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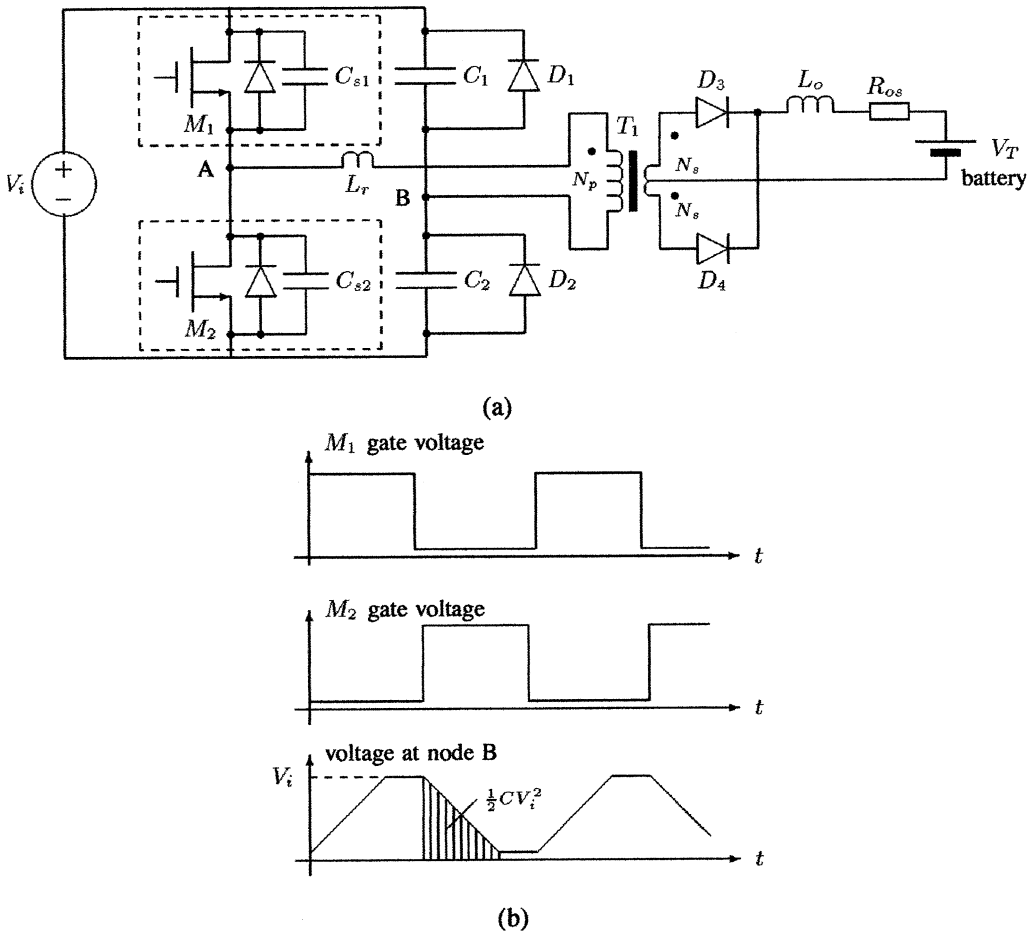

Fig. 1. Constant power converter for battery charging: (a) schematic and (b) waveforms showing basic operation.

the discharging of C_2 and charging of C_1 begin when M_2 is turned on. In this case, the voltage at node B will fall to 0 V and be clamped at this level. Likewise, current is delivered to the output load during the discharging of C_2 and charging of C_1. While the detailed operation is left to Section IV, we can immediately appreciate that the output power is limited by the size of capacitors C_1 and C_2. Provided that the on-period of M_1 or M_2 is sufficiently long, capacitors C_1 and C_2 can be charged and discharged fully within a cycle. Thus, the capacitors will transfer their energy entirely to the output side, achieving constant power delivery. Furthermore, the loss associated with discharging and charging the dividing capacitors is partially recovered and delivered to the load due to the presence of an reactive elements L_r which is placed in series with the equivalent loading at the primary side of transformer T_1.

For a preliminary analysis of the circuit operation, we may assume that

a) the primary magnetizing inductance of transformer T_1 is large enough to make the magnetizing current negligible;
b) the output inductance L_o is large enough to maintain a continuous-mode operation of its current.

Suppose that in each switching cycle, the dividing capacitors are completely discharged of the energy stored during the charging interval. Since the stored energy in L_r is not delivered directly to the load (rather recovered to the input), the power delivered to the primary side of the transformer, denoted by P_{T1}, is given by

$$P_{T1} = (C_1 + C_2)V_i^2 f_s - L_r I_p^2 f_s \tag{1}$$

where I_p is the output current reflected at the primary winding of transformer T_1, and f_s is the switching frequency. Neglecting the voltage drop across the equivalent series resistance of the battery, the maximum output power $P_{o,\max}$ can be written as

$$P_{o,\max} = V_T I_p \frac{N_p}{N_s}. \tag{2}$$

Equating $P_{o,\max}$ and P_{T1} gives

$$P_{o,\max} = C_{12}V_i^2 f_s - \frac{\left[\frac{N_p}{N_s}\left(\sqrt{V_T^2 + 4L_r C_{12}\left(f_s V_i \frac{N_s}{N_p}\right)^2} - V_T\right)\right]^2}{4L_r f_s} \tag{3}$$

where $C_{12} = C_1 + C_2$. If $L_r \ll (1/4C_{12})(V_T N_p / V_i f_s N_s)^2$, the maximum output power can be approximated as

$$P_{o,\max} \approx C_{12}V_i^2 f_s. \tag{4}$$

The validity of the above approximate formula is well justified because L_r is usually small. This is because the purpose of L_r is to assist soft switching of the MOSFET switches, and its value

needs only be large enough to buffer the energy from the equivalent drain-source stray capacitors.

To see the inherent power-factor-correction characteristic, we simply note from (4) that the input impedance of the converter is resistive and is given by $R_i = 1/C_{12}f_s$. Hence, when used with an AC mains input, the circuit naturally attains high input power factor.

It should be noted that in order to ensure constant power operation, the output current should be maintained at a level such that the output power falls within the power limit. This puts a limit on the ohmic drop across the connecting wire and the battery internal resistance, i.e.,

$$R_{\rm os} \le \frac{\frac{V_i N_s}{2N_p} - V_T}{2C_{12}f_s V_i \frac{N_p}{N_s}} \tag{5}$$

where $R_{\rm os}$ is the equivalent resistance consisting of the battery internal resistance and the connecting wire, and $V_i > 2V_T(N_p/N_s)$. In practice, since $R_{\rm os}$ is very small, the criterion stated in (5) should be easily satisfied. Thus, this topology is very suitable for the implementation of a constant power charger.

III. Averaged Circuit Operation in a Mains Cycle

In the foregoing section, we have demonstrated the inherent resistive input characteristic that can be exploited for power factor correction. Here, we will consider the operation when the input is connected to an AC mains. Referring to Fig. 2, the operation can be described in terms of five stages, corresponding to five sub-intervals of time during a mains half-cycle. For brevity, we let $v_i(t)$ be the input voltage, and C_i be the equivalent input capacitor which holds a minimum voltage V_r during a finite interval of time near the mains zero cross-over. Note that $C_i = C_{12}/4$ if no extra input filter or bulk capacitor is added.

- **Stage 1:** $0 < t < \tau_0$—The input voltage $v_i(t)$ is lower than V_r, resulting in zero input current. Fig. 2(b) shows the equivalent circuit during this stage.
- **Stage 2:** $\tau_0 < t < \tau_1$—The input voltage is higher than V_r, but the voltage reflected at the transformer secondary is below V_T. Fig. 2(c) shows the equivalent circuit. In this stage, the input current starts to energize the series dividing capacitors.
- **Stage 3:** $\tau_1 < t < \tau_2$—This stage occurs for a short transient duration. Fig. 2(d) shows the corresponding equivalent circuit. The input voltage produces a peak transformer secondary voltage higher than the battery voltage V_T. Power begins to flow to the output. However, the output voltage is still too low to permit a discontinuous-voltage-mode operation of the dividing capacitors.
- **Stage 4:** $\tau_2 < t < \tau_3$—This stage accounts for the largest part of the mains half-cycle. The equivalent circuit is shown in Fig. 2(e). In this stage, the converter runs into constant power mode, and the input AC impedance becomes virtually resistive. The transformer primary voltage swings between 0 V and $v_i(t)$, and capacitors C_1 and C_2 operate in discontinuous-voltage mode.
- **Stage 5:** $\tau_3 < t < \tau_4$—In this brief transition stage, as illustrated in Fig. 2(f), the input voltage falls too low to maintain the constant power mode, and the input current drops to zero at τ_4. The voltage across C_i will stay at V_r.

Having gone through the various stages in a mains half-cycle, we now derive the formulas for $\tau_0, \tau_1, \tau_2, \tau_3, \tau_4$, and relevant input and output currents. First of all, τ_0 can be found by equating $v_i(t)$ and V_r, i.e.,

$$\tau_0 = \frac{\sin^{-1}(V_r/\hat{V}_i)}{\omega_m} \tag{6}$$

where $\hat{V}_i$ is the peak input voltage, $\omega_m = 2\pi f_m$, and f_m is the mains frequency. Next, we can find τ_1 by noting that during stage 2, the voltage at the transformer secondary is equal to the battery voltage V_T, i.e.,

$$\tau_1 = \frac{\sin^{-1}(2V_T N_p/\hat{V}_i N_s)}{\omega_m}. \tag{7}$$

The input current during stage 2, denoted by $i_{[\tau_0-\tau_1]}(t)$, is given by

$$i_{[\tau_0-\tau_1]}(t) = \omega_m C_i \hat{V}_i \cos\omega_m t. \tag{8}$$

We now consider stage 3. The output current, denoted by $i_{o[\tau_1-\tau_2]}(t)$, is given by (9) shown at the bottom of the page. Since constant power operation starts to come to effect at the end of stage 3, we can write

$$i_{o[\tau_1-\tau_2]}(\tau_2) = \frac{2N_p C_{12} f_s \hat{V}_i}{N_s} \sin\omega_m \tau_2. \tag{10}$$

Furthermore, for $\tau_1 < t < \tau_2$, we have

$$i_{[\tau_1-\tau_2]}(t) = \omega_m C_i \hat{V}_i \cos\omega_m t + i_{o[\tau_1-\tau_2]}(t)\frac{N_s}{2N_p}. \tag{11}$$

We can therefore find τ_2 numerically by putting (9) in (10).

To find τ_3, we consider the value of the input voltage at the boundary of constant power mode as given in (5). Since the voltage across the series capacitors C_1 and C_2 follow the input voltage, we have

$$\tau_3 = \frac{1}{\omega_m}\sin^{-1}\left(\frac{2V_T}{\frac{\hat{V}_i N_s}{N_p} - 4\hat{V}_i R_{\rm os} C_{12} f_s \frac{N_p}{N_s}}\right) \tag{12}$$

$$i_{o[\tau_1-\tau_2]}(t) = \frac{\hat{V}_i N_s}{2N_p}\left(\frac{R_{\rm os}\sin\omega_m t - \omega_m L_o \cos\omega_m t - (R_{\rm os}\sin\omega_m\tau_1 - \omega_m L_o\cos\omega_m\tau_1)e^{-R_{\rm os}(t-\tau_1)/L_o}}{\omega_m^2 L_o^2 + R_{\rm os}^2}\right) + \frac{V_T}{R_{\rm os}}\left(e^{-R_{\rm os}(t-\tau_1)/L_o} - 1\right). \tag{9}$$

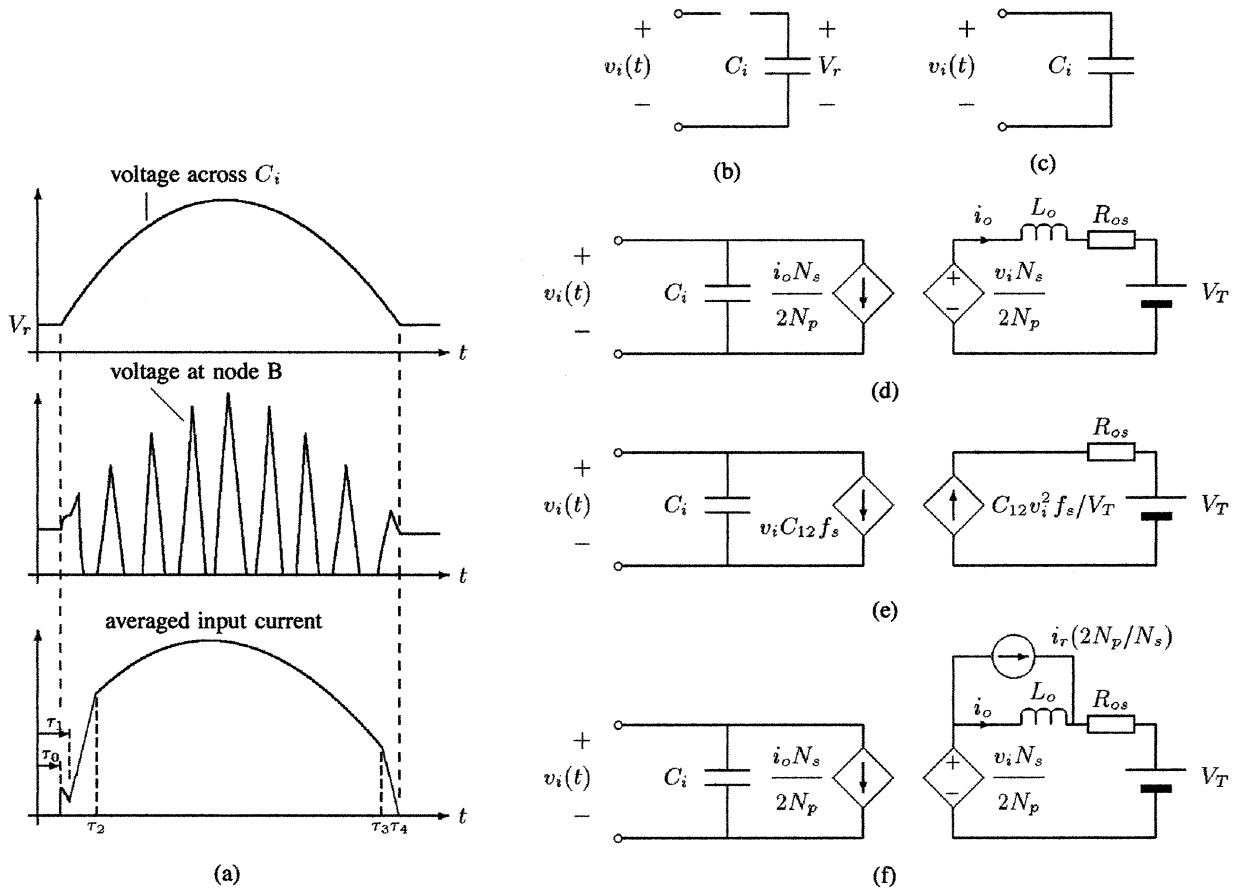

Fig. 2. (a) Waveforms showing different stages in a mains half-cycle, (b) equivalent averaged circuit for $0 < t < \tau_0$, (c) equivalent averaged circuit for $\tau_0 < t < \tau_1$, (d) equivalent averaged circuit for $\tau_1 < t < \tau_2$, (e) equivalent averaged circuit for $\tau_2 < t < \tau_3$, and (f) equivalent averaged circuit for $\tau_3 < t < \tau_4$.

for $(1/4f_m) < t < (1/2f_m)$, and the corresponding input current waveform during stage 4 is

$$i_{[\tau_2-\tau_3]}(t) = \omega_m C_i \hat{V}_i \cos\omega_m t - C_{12} f_s \hat{V}_i \sin\omega_m t. \quad (13)$$

Also, capacitor C_i will hold up the input voltage and prevent the voltage across the capacitor from following the input voltage waveform. From (13), the input current can drop to zero before τ_3 is reached, provided that

$$C_i > \left| \frac{C_{12} f_s \sin\omega_m\tau_3}{\omega_m \cos\omega_m\tau_3} \right|. \quad (14)$$

Suppose the input current falls to zero at $t = \tau_3' < \tau_3$. It is readily found that

$$\tau_3' = \frac{-1}{\omega_m} \tan^{-1}\left(\frac{\omega_m C_i}{C_{12} f_s}\right). \quad (15)$$

However, in practice, $\omega_m \ll 2\pi f_s$ and there is no large input bulk capacitor, (15) therefore has no acceptable solution, meaning that the input current cannot fall to zero before $t = \tau_3$.

We can thus assume that at $t = \tau_3$ the input current takes a nonzero value of i_r. The input current waveform during stage 5 is then given by (16) shown at the bottom of the page, and i_r can be simply written as

$$i_r = C_{12} f_s \hat{V}_i \sin\omega_m\tau_3. \quad (17)$$

Thus, τ_4 can be numerically obtained from

$$i_{[\tau_3-\tau_4]}(\tau_4) = 0. \quad (18)$$

Furthermore, the residue voltage V_r can be approximated as

$$V_r = \hat{V}_i \sin\omega_m\tau_4. \quad (19)$$

Finally, since $R_{\rm os}$ and L_r are small, only stage 4 is significant. The averaged (maximum) input power, denoted by $P_{\rm in,max}$, can be approximated by averaging the input power over the period from τ_2 to τ_3, giving

$$P_{\rm in,max} \approx 2C_{12} f_s f_m \int_{\tau_2}^{\tau_3} \hat{V}_i^2 \sin^2\omega_m t\, dt. \quad (20)$$

$$i_{[\tau_3-\tau_4]}(t) = \frac{\hat{V}_i N_s^2}{4N_p^2}\left(\frac{R_{\rm os}\sin\omega_m t - \omega_m L_o\cos\omega_m t - (R_{\rm os}\sin\omega_m\tau_3 - \omega_m L_o\cos\omega_m\tau_3)e^{-R_{\rm os}(t-\tau_3)/L_o}}{\omega_m^2 L_o^2 + R_{\rm os}^2}\right)$$
$$+ \frac{V_T N_s}{2R_{\rm os}N_p}\left(e^{-R_{\rm os}(t-\tau_3)/L_o} - 1\right) + i_r e^{-R_{\rm os}(t-\tau_3)/L_o} + \omega_m C_i \hat{V}_i \cos\omega_m t \quad (16)$$

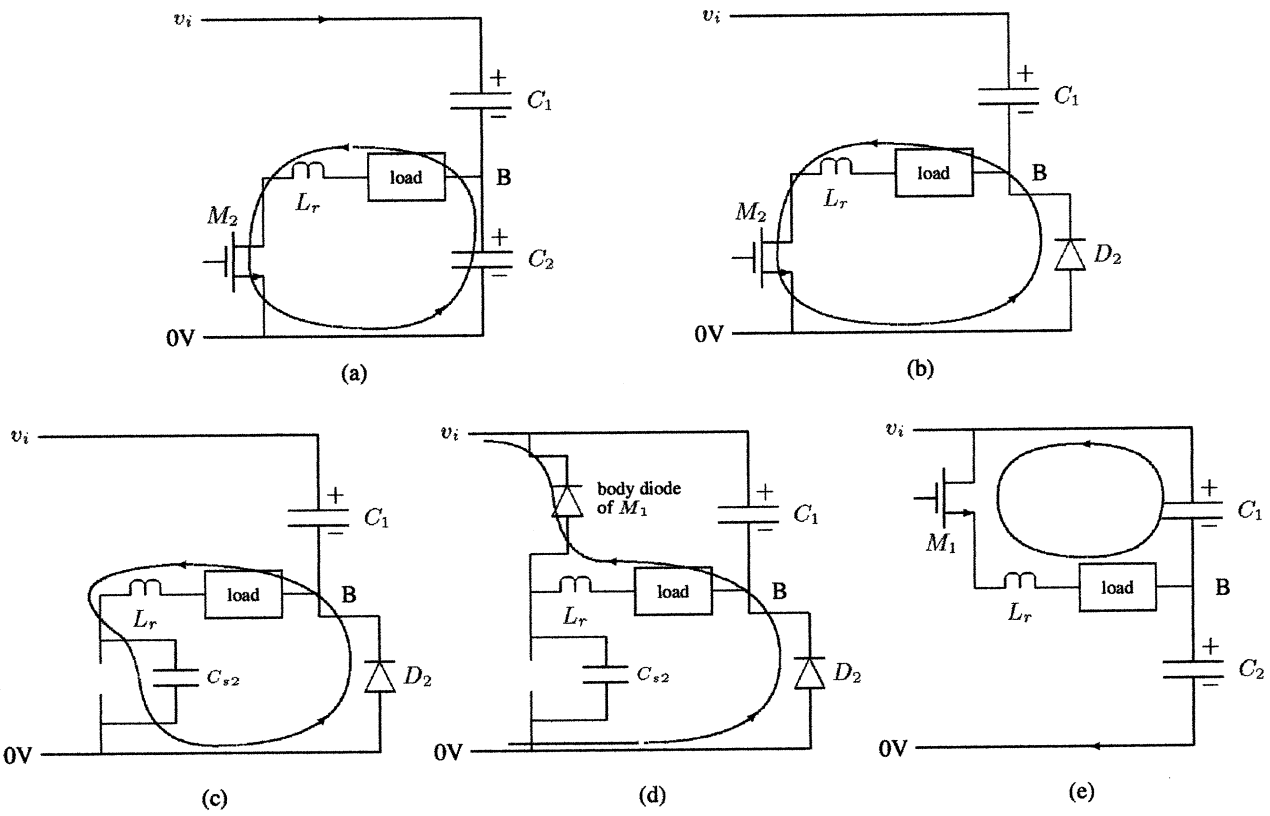

Fig. 3. Topological sequence in a switching half-cycle for constant power mode ($\tau_2 < t < \tau_3$): (a) M_2 on and power being delivered to load, (b) current circulating through parallel diode, (c) stray capacitance of M_2 being charged, (d) zero voltage state created for M_1, and (e) M_1 turned on and power being delivered to load.

Expanding gives

$$P_{\text{in,max}} \approx \frac{C_{12}\hat{V}_i^2 f_s}{2\pi}(\cos\omega_m\tau_2 \sin\omega_m\tau_2 - \cos\omega_m\tau_3 \sin\omega_m\tau_3 + \omega_m\tau_3 - \omega_m\tau_2). \quad (21)$$

The foregoing describes the averaged circuit operation in various stages during a mains half-cycle and provides approximate formulae for the time durations of these stages and the input current waveform which can be used to predict the harmonic contents of the input current. Calculations based on the above formulas and experimental measurements will be compared in a later section.

IV. Circuit Operation in a Switching Cycle

In this section, we study the detailed circuit operation in a switching cycle, and attempt to highlight the salient characteristics of the proposed converter. Taking advantage of the symmetry of the converter, we need only to consider the half switching cycle [10], [11], and in particular we focus on the duration in which the circuit operates in constant power mode, i.e., $\tau_2 < t < \tau_3$.

Fig. 3 shows the topological sequence in a switching half-cycle. We begin with M_2 being turned on (M_1 off), as illustrated in Fig. 3(a). During this stage, capacitor C_2 discharges itself and delivers current to the load. The voltage between the two dividing capacitors falls gradually. This stage is the only power delivering stage in the switching half-cycle. Since L_r is small and R_{os} is negligible, the effective duty cycle D_{eff} can be written as

$$D_{\text{eff}}(t) = \frac{2V_T N_p}{\hat{V}_i N_s \sin\omega_m t} \quad (22)$$

which is valid as long as the circuit operates in constant power mode, i.e., $\tau_2 < t < \tau_3$ in the mains half-cycle. As capacitor C_2 discharges, its voltage falls to 0 V. By action of the small inductor, current forces its way through diode D_2, as illustrated in Fig. 3(b). The next step is to turn off M_2. This causes the drain-source capacitance of M_2 to be charged by the circulating current, as shown in Fig. 3(c) (at the same time discharging that of M_1), and soon the body diode of M_1 conducts, as shown in Fig. 3(d). This creates a zero-voltage condition for M_1 to turn on softly [12], [13]. The second half-cycle repeats with the roles of M_1 and M_2 interchanged.

It is of interest to know the constraints, if any, on the choice of component values and parameters in order for the circuit to operate as described. Firstly, assuming that the zero-voltage turn-on transient duration corresponding to the stages shown in Fig. 3(c) and (d) is small, the averaged current flowing through diode D_2, denoted by $i_{D_2}(t)$, is

$$i_{D_2}(t) = [1 - D_{\text{eff}}(t)]i_p(t) \quad (23)$$

where

$$i_p(t) = \frac{C_{12} f_s N_s \hat{V}_i^2 \sin^2\omega_m t}{V_T N_p} \quad (24)$$

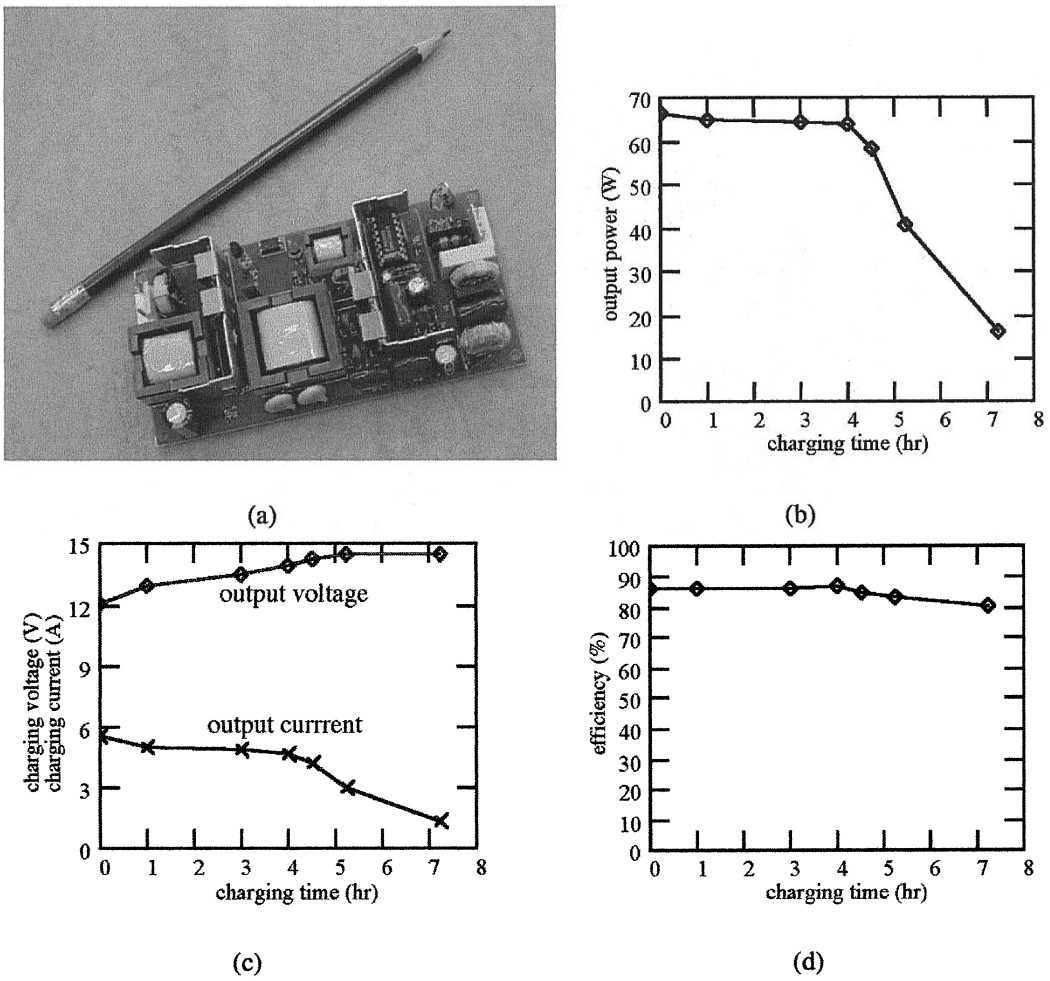

Fig. 4. (a) Photo of the charger showing minimal thermal requirement, (b) output power, (c) output voltage and current versus charging time, and (d) efficiency versus charging time.

for $\tau_2 < t < \tau_3$ in the mains half-cycle. In fact, $i_p(t)$ is the current value at the instant when M_2 is turned off. Starting with this value, the diode current resonates until a zero-voltage condition is created for M_1. Let the drain-source capacitance be C_{s1} and C_{s2}, for M_1 and M_2, respectively. Also, define C_s by

$$C_s = C_{s1} + C_{s2} \tag{25}$$

which is the equivalent stray capacitance seen at node A (see Fig. 1). Then, the duration of the resonating period, denoted by $\tau_{\rm res}(t)$, can be written as

$$\tau_{\rm res}(t) = \sqrt{L_r C_s}\sin^{-1}\left(\frac{V_T N_p}{C_{12} f_s \hat{V}_i N_s \sin\omega_m t}\sqrt{\frac{C_s}{L_r}}\right) \tag{26}$$

which is valid for $\tau_2 < t < \tau_3$ in the mains half-cycle. Furthermore, in order for C_{s2} to be charged up to $v_i(t)$ (and C_{s1} to be discharged to zero), the series inductor should satisfy

$$L_r > C_s\left(\frac{V_T N_p}{C_{12} f_s \hat{V}_i N_s \sin\omega_m t}\right)^2. \tag{27}$$

Moreover, we recall from Section II that L_r should satisfy

$$L_r \ll \frac{(V_T N_p/\hat{V}_i f_s N_s)^2}{4C_{12}} \tag{28}$$

TABLE I
CALCULATED AND MEASURED PARAMETER VALUES

PARAMETER	CALCULATED	MEASURED	ERROR
C_{12}	13.58 nF	13.6 nF	+0.1 %
$P_{\rm in,max}$	72 W	75.7 W	+5.1 %
τ_0	2.00 ms	1.65 ms	−17.5 %
τ_1	2.21 ms	1.83 ms	−17.2 %
τ_2	2.47 ms	2.00 ms	−19.0 %
τ_3	7.75 ms	8.00 ms	+3.2 %
τ_4	7.96 ms	8.20 ms	+3.0 %
L_r	21 μH	20 μH	−4.8 %

in order for (4), hence (21), to be valid. Thus, combining (27) and (28), we require that

$$C_s \ll \frac{C_{12}}{4} \tag{29}$$

which is easily satisfied in most practical cases.

Finally we consider the zero-voltage turn-on condition for the MOSFETs. Basically, M_1, and M_2 should be programmed to turn on during a short duration of time in which the drain-source

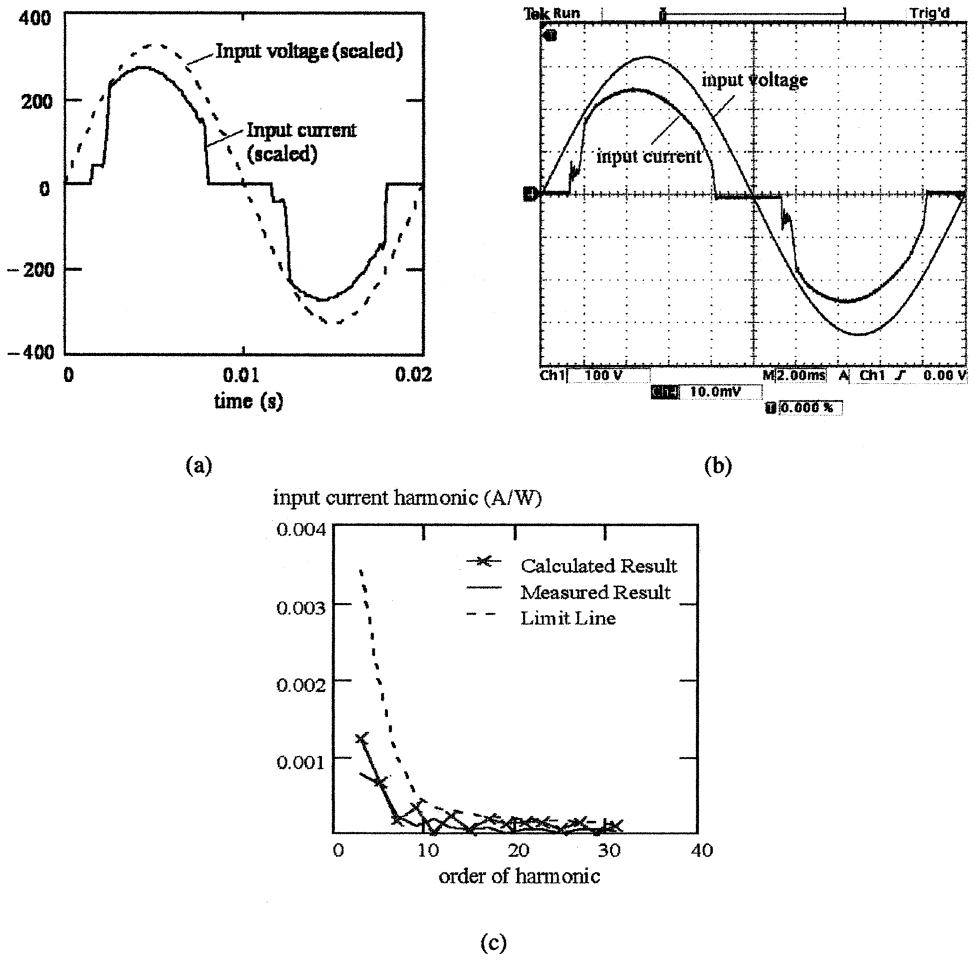

Fig. 5. (a) Theoretical input current and voltage waveforms, (b) measured input current and voltage waveforms, and (c) calculated and measured input harmonic current contents.

voltage is near zero. Denoted by $\tau_{\rm ZVS}$, the length of this brief duration can be found as

$$\tau_{\rm ZVS} = \left(\frac{C_{12} f_s \hat{V}_i L_r N_s \sin \omega_m t}{V_T N_p}\right) \cos\left(\frac{\tau_{\rm res}(t)}{\sqrt{L_r C_s}}\right) \qquad (30)$$

which is valid as long as the constant power mode is maintained, i.e., $\tau_2 < t < \tau_3$ in the mains half-cycle.

V. Experimental Verification

A 65 W constant power charger for a 12 V 35 Ah lead-acid battery was built to verify the proposed design. Assuming a 90% efficiency, the input power needed is 72 W. The basic circuit parameters are chosen as follows: $f_s = 120$ kHz, $N_s/N_p = 3/26$, and $C_{\rm in} = 1$ μF (extra input filtering capacitor). From (21), C_{12} is found as 13.58 nF, from which we have $C_1 = C_2 = 6800$ pF. The minimum series ZVS inductance, L_r, is found from (27) as 21 μH. In the experiment, a 20 μH is used. Other crucial components are chosen as follows: diodes D_3 and D_4 are MBR20100, MOSFETs M_1, and M_2 are STPS6NB50, and transformer core T_1 is EET30 NC2H. Furthermore, since constant power charging is employed, the charging control is as simple as lowering the power level through the pulse-width modulator once the output voltage has reached the required level.

Table I compares the calculated and measured values of some critical parameters, and Fig. 4 shows a photo of the prototype and some measured results. As shown in Fig. 4(b), the output power remains almost constant for virtually the whole charging period. The power starts to drop at the fifth hour when the battery is fully charged and has reached the clamped voltage of the converter. The converter then further reduces the power by a pulse-width-modulation mechanism. The measured battery voltage V_T is 12 V, and the series equivalent resistance $R_{\rm os}$ is 0.03 Ω. The measured efficiency of the charger reaches 87%, taking into account the loss of an input EMI filter which is needed to suppress the conductive noise to below the class B level.

As shown in Fig. 5(a) and (b), the theoretical and measured waveforms of input voltage and current match quite well. In fact, we have observed that the measured waveform of the input in Fig. 5(b) is even more desirable compared to what has been predicted in Fig. 5(a). The difference is due to the deviation of τ_1 and τ_2, as a result of the presence of magnetizing inductance of the transformer which causes voltage swing at the center point of the dividing capacitors, giving a higher peak voltage at the secondary of the transformer and an enlarged duration of power

transfer to the battery. Finally, the input harmonic current contents have been found to meet regulatory requirements, as shown in Fig. 5(c).

VI. Conclusion

A constant power charger with inherent soft switching and power factor correction has been presented. By virtue of the constant charging power, there is no need to install substantial thermal management to address the dissipation problem which may occur only for a short portion of the whole charging process as in the cases of constant voltage and constant current chargers. This advantage will become significant for high-power charging applications. As zero-voltage-switching and power factor correction are achieved inherently with no extra control circuits, the proposed circuit is very suitable for implementation of low-cost high-performance battery chargers.

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