Enhanced Mobility for Pentacene TFT Built on NH_3-Annealed Thermally Grown SiO_2

M. C. Kwan, Kenneth K. H. Cheng, P. T. Lai and C. M. Che

Abstract – **We have enhanced the mobility of pentacene OTFTs using NH_3-annealed SiO_2 as gate dielectric and this annealing method is often applied in the semiconductor industry for inorganic transistors. The device has field-effect mobility higher than 0.5 cm^2/Vs, with on/off current ratio larger than 10^6, and subthreshold slope less than 2.5 V per decade. When compared with the control sample, which uses N_2-annealed SiO_2, the mobility of the proposed pentacene OTFT increases by over 50%.**

I. Introduction

In the past decade, organic thin-film transistor (OTFT) has been studied extensively [1] due to its potentially low-cost applications such as radio-frequency identification (RFID) and flexible, light-weight large-screen displays. Among all organic materials used to fabricate OTFT, pentacene is the most commonly used organic material to act as the active layer because of its high carrier mobility in OTFTs [2] and high stability in air. The performance of OTFT is determined by its mobility, which in turn is greatly influenced by the interface properties between the active layer and the dielectric layer. Octadecyltrichlorosilane (OTS) [3]-[5] and other materials [6]-[7] were used to modify the surface of the dielectric layer to enhance the OTFT mobility. In this work, we perform an ammonia (NH_3) annealing after the growth of thermal SiO_2 in order to modify the surface of the SiO_2. Our results show that the NH_3 annealing can increase the mobility of the pentacene OTFT by up to 58%.

II. Experimental

In our process, n-type silicon wafers were first cleaned using the standard RCA process. The wafers were then oxidized in dry oxygen at 1100°C for 200 minutes. This step was followed by either NH_3 or N_2 annealing at 1100°C for 60 minutes. The device fabricated on N_2-annealed SiO_2 was for comparison purpose. The thickness of SiO_2 measured by F20 Thin-Film Measurement System (Filmetrics, Inc) was 274 nm for the NH_3-annealed SiO_2 and 238 nm for the N_2-annealed SiO_2. Before pentacene deposition, the SiO_2 at the back of both wafers was removed using 20% HF solution. The back of the silicon wafers then acted as the gate of the OTFT. Pentacene was deposited using Edward Auto 306 thermal evaporator. During the pentacene deposition, the chamber pressure was kept at 10^{-6} torr. and the deposition rate was about 1.3 nm per minute. The thickness of the pentacene thin film was 30 nm which was measured by a quartz-crystal thin-film thickness monitor. After pentacene deposition, gold source and drain contacts were evaporated onto the pentacene thin film through a shadow mask. The channel length (L) and channel width (W) were around 30 μm and 300 μm respectively. The electrical characteristics of OTFTs were measured by Hewlett Packard 4145B semiconductor parameter analyzer. The I-V characteristics of all OTFTs were measured at room temperature in dark environment. Fig. 1 shows the structure of the pentacene OTFT.

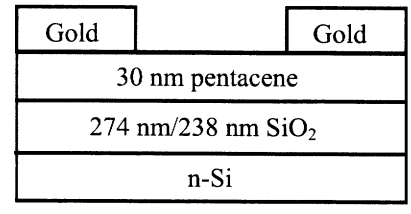

Fig. 1 Pentacene thin-film transistor structure. Top gold contacts for source and drain, while n-Si substrate for gate.

III. Results and Discussion

OTFT operates due to the field effect, which is similar to that in MOSFET. However, OTFT operates in the accumulation regime, not in the inversion regime as in MOSFET. In a p-type OTFT, when a negative voltage is applied to the gate terminal, positive charges or holes will accumulate at the interface between the dielectric layer and the organic active layer. If the applied negative voltage is large enough to accumulate a large amount of holes, then a conductive channel is formed and the OTFT is said to be in the "on state". The voltage required to turn on the OTFT is called the threshold voltage V_T.

Once the OTFT is on, applying a negative voltage to the drain terminal will lead to a current flow from the source terminal to the drain terminal due to the movement

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of holes. The drain current I_D in the linear and saturation regions is given by equation (1) and (2), respectively

$$I_D = \frac{W}{L}\mu C_O(V_G - V_T - \frac{V_D}{2})V_D \quad (1)$$

$$I_D = \frac{W}{2L}\mu C_O(V_G - V_T)^2 \quad (2)$$

where V_D and V_G are the drain and gate voltages; W and L are the channel width and length; C_O is the capacitance per unit area of the insulator; and μ is the carrier mobility.

The channel transconductance g_m in the linear and saturation regions are given by equation (3) and (4), respectively

$$g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D=cons\tan t} = \frac{W}{L}\mu C_O V_D \quad (3)$$

$$g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D=cons\tan t} = \frac{W}{L}\mu C_O(V_G - V_T) \quad (4)$$

The field-effect mobility μ can be calculated from the slope of the plot of $\sqrt{I_D}$ versus V_G in the saturation regime. Fig. 2 shows the I-V characteristic curves of the OTFT with N_2-annealed SiO_2. This device has a channel length and width of 32 μ m and 297 μ m, respectively. The thicknesses of pentacene and SiO_2 are 30 nm and 238 nm respectively. The field-effect mobility in the saturation region is 0.33 cm^2/Vs. The threshold voltage is -30.5 V and the subthreshold slope is 3.4 V/decade. The device has an on/off current ratio of $1.2x10^6$.

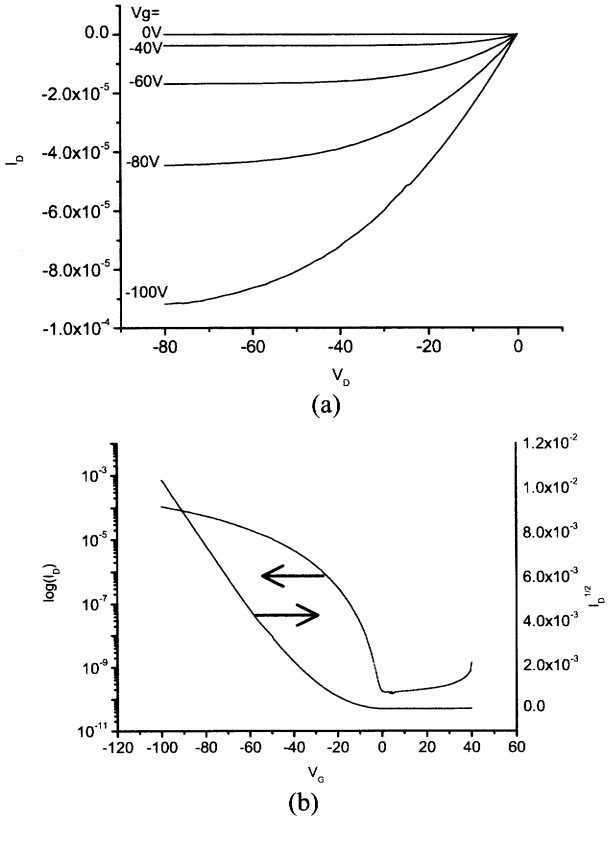

Fig. 2 FET characteristics of a pentacene thin-film transistor with a 238-nm film fabricated on N_2-annealed SiO_2/Si substrate. L = 32 μm and W = 297 μm. The field-effect mobility in the saturation region is 0.33 cm^2/Vs at V_D = –80 V. (a) I_D versus V_D characteristics. (b) $I_D^{1/2}$ versus V_G characteristics.

Fig. 3 shows the I-V characteristic curves of the OTFT with NH_3-annealed SiO_2. This device has a channel length and width of 33 μ m and 266 μ m, respectively. The thicknesses of pentacene and oxynitride are 30 nm and 274 nm respectively. The field-effect mobility at saturation region is 0.53 cm^2/Vs. The threshold voltage is -25.6 V and the subthreshold slope is 2.4 V/decade. The device has an on/off ratio of $1.3x10^6$.

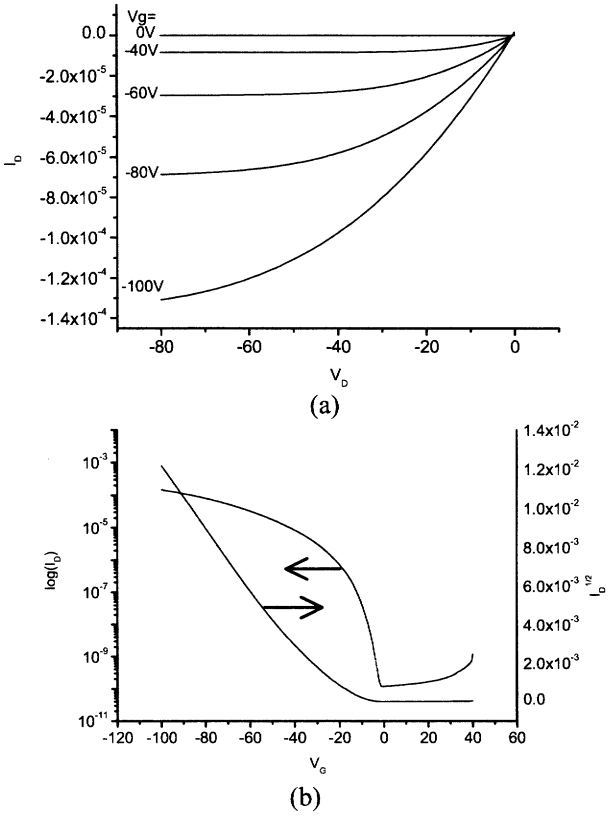

Fig. 3 FET characteristics of a pentacene thin-film transistor with a 274-nm film fabricated on NH_3-annealed SiO_2/Si substrate. L = 33 μm and W = 266 μm. The field-effect mobility in the saturation region is 0.53 cm^2/Vs at V_D = –80 V. (a) I_D versus V_D characteristics. (b) $I_D^{1/2}$ versus V_G characteristics.

When comparing the mobilities of these two devices, the mobility of OTFT with NH_3-annealed SiO_2 is 60% higher than its counterpart. Under high temperature and in pure ammonia gas, oxygen atoms in SiO_2 layer are replaced by nitrogen atoms forming an oxynitride layer [8]. The nitrogen concentration decreases with the distance from the exposed SiO_2 surface [8]-[10]. The incorporation of N can reduce dangling bonds and mechanical stress, resulting in a passivated surface [11]. This provides a "better" surface for the deposition of the pentacene layer, and the pentacene layer could be formed

with improved morphology. As a result, the field-effect mobility increases.

There is a 15% decrease in magnitude of the threshold voltage for the OTFT with NH_3-annealed SiO_2 although it has a thicker gate dielectric. The decrease in threshold voltage may be due to the fact that hydrogen species in the oxynitride film induced by the NH_3 annealing increase the trapping of electrons [12], which is equivalent to a built-in negative gate voltage. Therefore, the OTFT can be turned on by using smaller gate voltage.

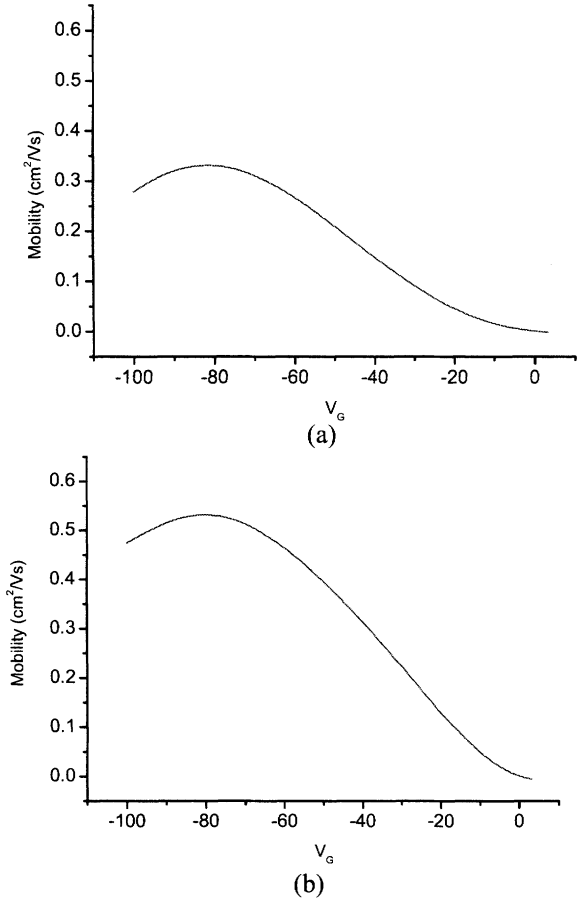

Fig. 4 Mobility versus V_G in N_2 (a) and in NH_3 (b) at V_D = -80 V.

Fig. 4 shows the relation between the field-effect mobility and gate voltage. At low gate voltage, the field-effect mobility increases with the gate voltage. This phenomenon can be explained by the multiple trapping and release (MTR) model developed by Thiais group [13]-[15]. In their model, the field-effect mobility is gate-bias dependent. When the gate bias is increased, the Fermi level gradually approaches the nearest delocalized band edge. There exist near the delocalized bands localized levels, which act as traps for charge carriers. At low gate bias, nearly all induced charges go to the localized levels, where their mobility is very low and do not contribute to charge transport. With an increase of the gate voltage, the Fermi level approaches the delocalized band and more traps are filled, which leads to an increase of the concentration of mobile carriers in the delocalized levels. As a result, the effective mobility increases. Fig. 4 shows that the maximum mobility reaches 0.33 cm^2/Vs and 0.53 cm^2/Vs for N_2 annealed and NH_3 annealed respectively.

Further increase of the gate voltage will lead to a decrease in mobility in both cases. This may due to the fact that, at high gate voltage, too many carriers accumulate at the interface between the dielectric layer and the pentacene active layer. Scattering among carriers hinders the movement and results in lower mobility.

IV. Conclusion

We have demonstrated a method commonly used in the semiconductor industry to modify the gate dielectric of OTFT for better device performance. The method is to do a NH_3 annealing after the growth of the SiO_2 dielectric. Results show that OTFT built on NH_3-annealed SiO_2 has a mobility increased by over 50% to 0.5 cm^2/Vs.

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