Improved I-V Characteristics of SiC MOSFETs by TCE Thermal Gate Oxidation

B. L. Yang, L. M. Lin, J. P. Xu and P. T. Lai

Abstract-The effects of TCE (trichloroethylene) thermal gate oxidation on the electrical characteristics of SiC MOSFETs are investigated. It is found that TCE thermal gate oxidation can improve the I_d-V_d characteristics, increase the field-effect mobility, and reduce the threshold voltage and sub-threshold slope of the devices. The better device characteristics are believed to be attributed to the TCE-induced reductions of charges in the gate oxide and traps at the SiC/SiO$_2$ interface, and also to the gettering of charged impurities and reduction of physical defects by the chlorine incorporated in the gate oxide.

I. INTRODUCTION

Since MOSFETs were successfully realized on the cubic polytype SiC in the early 1980's [1], SiC-based MOSFETs and other MOS-related structures have become a very hot research topic. SiC finds applications in high-temperature, high-frequency and high-power electron devices due to its wide bandgap, high electron mobility and excellent thermal conductivity [2,3]. Among these studies, improving the performance of SiC MOSFETs by different fabrication technologies is one important theme. Previous research has demonstrated that the properties of the SiO$_2$/SiC interface can be improved by TCE oxidation [4, 5]. In this work, we focus on the effects of TCE thermal gate oxidation on the electrical characteristics of SiC MOSFET, including its field-effect mobility, threshold voltage and sub-threshold slope.

II. EXPERIMENT

p-type (0001) Si-face 6H-SiC wafers with a doping concentration of $6.45\text{x}10^{15}/\text{cm}^3$ and a 5-μm epitaxial layer used in this investigation were purchased from CREE Research Inc. The wafers were cleaned using H_2SO_4 and the conventional RCA method followed by a 15-s dip in 5% HF solution. Channel length and width (L and W) were 10 μm and 130 μm. 350-nm SiO$_2$ sputtered on the SiC wafers was used as the mask for the phosphorus implant of source and drain regions. The implant condition was 100 keV/$2.45\text{x}10^{15}/\text{cm}^2$ + 60 keV/$1.45\text{x}10^{15}$ /cm^2. The implanted phosphorus was activated for 2 hrs at 1200 ^{0}C. 19-nm gate oxide was grown at 1100 ^{0}C in the control sample (in pure dry-O$_2$ ambient) and the TCE sample (in TCE plus oxygen ambient, ratio of TCE to oxygen was 0.05). The TCE vapor was added to the oxidizing ambient by a gas controller, and the amount of TCE was controlled by varying the flow rate of dry nitrogen through a bubbler filled with liquid TCE kept at 0 °C. The wafers were loaded into an oxidation furnace at 800 °C, and then the furnace temperature was raised to 1100 °C. The wafers were oxidized, and the grown gate oxide was annealed for 30 min. in N$_2$ ambient at 1100 °C. Then the furnace temperature was reduced to 800 °C at a rate of –3 °C/min. Finally, after the contact holes were opened for the source and drain, about 1-μm aluminum was thermally evaporated on the wafers and then patterned as the electrodes of the MOSFETs. The device parameters were measured at room temperature using HP 4156A Precision Semiconductor Parameter Analyzer.

III. RESUTS AND DISCUSSIONS

Fig. 1 shows the I_d-V_d characteristics of the MOSFETs. It can be seen that Id of the TCE sample is much larger (about 1.5 times) than that of the control sample. The field-effect mobility μ_{FE} can be calculated using the following formula at a drain voltage $V_d = 0.1$ V [6]:

$$\mu_{FE} = \frac{dI_d}{dV_g}\frac{1}{C_{ox}V_D}\left(\frac{L}{W}\right) \qquad (1)$$

where I_d is the drain current, L the channel length , W the channel width and C_{ox} the gate-oxide

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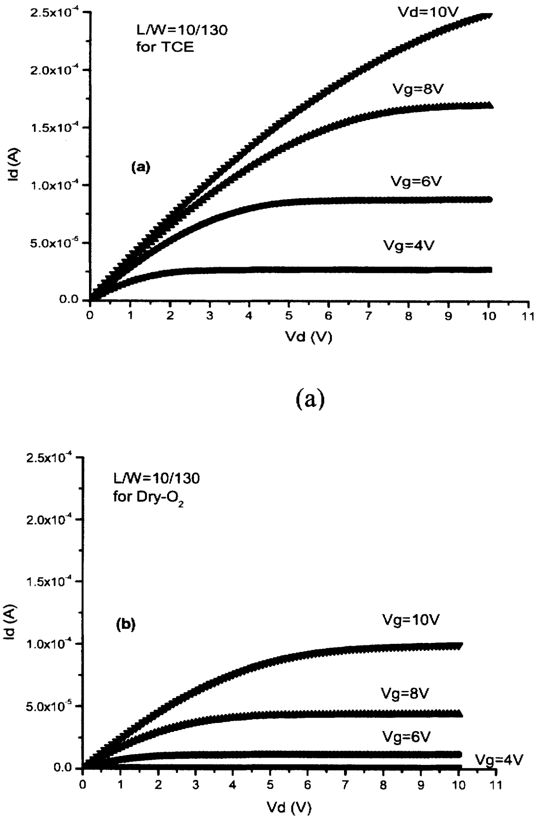
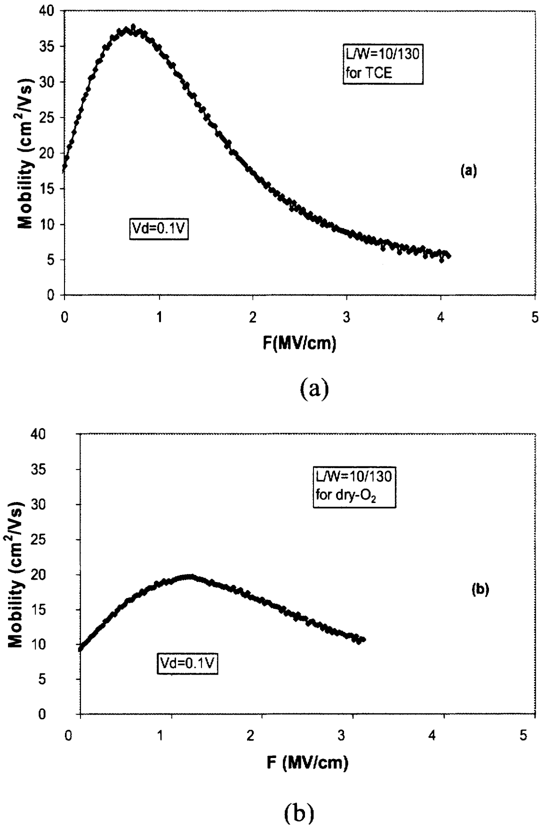
capacitance extracted from a MOS capacitor. The dependence of μ_{FE} on effective electrical field (F) applied to the gate electrode is shown in Fig. 2 (F = (Vg – V_t)/gate-oxide thickness). It can be found that the field-effect mobility of the TCE sample is much higher than that of the control sample.



(a)

(b)

Fig. 1 Measured I_d-V_d characteristics of the samples: (a) TCE; (b) Dry-O_2.



(a)

(b)

Fig. 2 Electron mobility of the samples versus effective gate field: (a) TCE; (b) Dry-O_2.

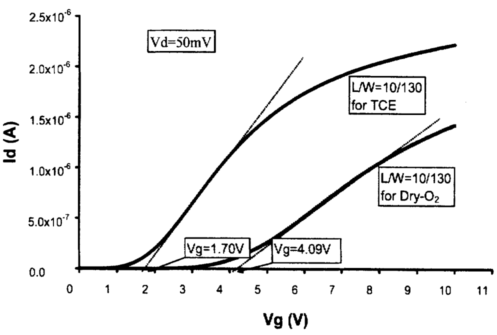


Fig. 3 Measured I_d-V_g characteristics of the samples.

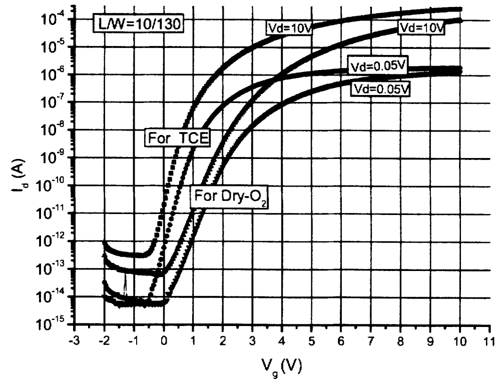


Fig. 4 Sub-threshold characteristics of the samples.

The threshold voltage V_t is measured by extrapolating the I_d versus V_{gs} curve to $I_d = 0$ for $V_D = 50$ mV, as shown in Fig. 3. The value of V_t is 1.62 V for the TCE sample and 3.91 V for the control sample. V_t of TCE samples reduced about 2 V, as compared to that of the control samples. If the oxide charge Q_{ox} and oxide capacitance C_{ox} of MOSFET are measured, V_t can be determined from the formula below [7]:

$$V_t = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_{SiC} 2\phi_B}}{C_{ox}} \tag{2a}$$

$$V_{fb} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} \tag{2b}$$

$$\phi_B = \frac{kT}{q} \ln\left(\frac{N_a}{n_i}\right) \tag{2c}$$

where V_{fb} is the flat-band voltage, q the elementary charge, N_a the acceptor concentration of the SiC substrate, ε_{SiC} the SiC permittivity, ϕ_{ms} the work-function difference between aluminum-gate and 6H-SiC, k the Boltzmann constant, T the device temperature in Kelvin and n_i the intrinsic carrier concentration of SiC. With $\phi_{ms} = -2.53$ V [5], the third term in (2a) = 2.6 V, the fourth term in (2a) = 0.4 V, $V_t = 1.62$ V for the TCE sample and 3.91 V for the control sample, the oxide charge Q_{ox} in (2b) can be calculated to be $-1.3\text{x}10^{12}$ cm^{-2} and $-3.3\text{x}10^{12}$ cm^{-2} for the two samples respectively.

The sub-threshold slope characteristics of the samples are shown in Fig. 4. It can be observed that the difference between the on current and off current is about 8 orders for a V_d range of 0.05 ~ 10 V. The interface quality of the MOSFETs was characterized in the weak inversion region by the slope of $\log(I_d)$ versus V_g curve, which is only affected by the capture of minority carriers by interface states [8]. The sub-threshold slope can be calculated by the following formula [9]:

$$S = \frac{dV_{gs}}{d[\log(I_d)]} \qquad \text{(3a)}$$

and is correlated to the density of interface states by

$$S \approx \left(\frac{kT}{q}\right)\ln(10)\left[\frac{C_{ox}+C_{it}+C_D}{C_{ox}}\right] \qquad \text{(3b)}$$

where C_D is the capacitance of the depletion layer, and C_{it} represents the capacitance associated with the interface-state density $D_{it} = C_{it}/q$ per eV and cm^2. The calculated results using (3a) show that S is 320 ~ 531 mV/dec for the control sample and 201 ~ 211 mV/dec for the TCE sample for a V_d range of 0.05 V ~ 10 V. The S of the TCE sample is smaller (about 1.5 ~ 1.7 times) than that of the control sample. Therefore, according to the formula (3b) that the sub-threshold slope increases with the interface-state density, the TCE sample should have fewer interface states. As a result, less carrier scattering by reduced interface states and also oxide charges gives higher electron mobility, as shown in Fig. 2a.

It has been reported that TCE thermal oxidation can reduce the charges in the gate oxide and the traps at the SiC/SiO_2 interface because the addition of chlorine can remove carbon clusters at the SiO_2/SiC interface, getter charged impurities and reduce physical defects in the gate oxide [4, 5]. As a result, the MOSFET has higher μ_{FE}, smaller flat-band voltage, V_t and sub-threshold slope. However, the detailed physical mechanisms require more investigations.

IV. SUMMARY

In this work, a study on the effects of TCE thermal gate oxidation on the I-V characteristics of SiC MOSFETs has been done. The experimental results demonstrate that TCE thermal gate oxidation can improve the electrical characteristics, increase the field-effect mobility, and reduce the threshold voltage and sub-threshold slope of the devices. The better device performance should be associated with the TCE-induced reductions of charges in the gate oxide and traps at the SiC/SiO_2 interface, and also gettering of charged impurities and removal of physical defects in the gate oxide. The detailed physics involved still need further study.

ACKNOWLEDGEMENT

The authors wish to thank Mr. C. L. Chan for help in fabricating samples. This work is financially supported by the RGC grant of Hong Kong.

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