DSP CONTROLLED POWER CONVERTER

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Abstract

A digital controller is designed and implemented by a Digital Signal Processor (DSP) to replace the Pulse Width Modulator (PWM) and error amplifier compensation network in a two wheeler forward converter.
The DSP controller is designed in three approaches:-
a) Discretization of analog controller --- the design is based on the transfer function of the error amplifier compensation network.
b) Digital PID controller design --- the design is based on the general form of the pulse transfer function of PID controller.
c) Deadbeat controller design --- the design is based on the open-loop pulse transfer function of the power converter.
The controller design is optimised by running computer simulation with the MATLAB numerical calculation package and the experimental results agree with the simulated analysis.

1 Introduction

Conventionally, switched mode power converter is controlled by monolithic IC which included the functions of oscillator, error amplifier and pulse width modulator (PWM). To stabilise the control loop, a compensation network should be connected to the error amplifier. This compensation network affects the stability and the frequency response of the converter. Thus the performance of the converter is highly dependent on the design of the compensation network which consists of resistors and capacitors. However, these components are often influenced by environmental disturbances such as electrical noise, temperature and ageing etc.

As microelectronics and microprocessors have been highly developed in the last decade, the realisation of sophisticated and inexpensive digital control system becomes feasible. The advantages of digital controllers are:
a) being digital in nature, they are less dependent on the accuracy and stability of passive and active components; and
b) they can be configured by software.

The latter feature is especially important when digital controllers are used to close feedback loops. It is because they permit one to realise sophisticated control laws which are difficult, and sometimes impossible, to realise by analog compensation network. Therefore, it is worth to investigate the methods of designing digital controllers.

This paper presents the methods of designing a digital controller for a two wheeler forward converter. The designs are optimised by running computer simulation and the controller is then implemented with the DSP, TMS320C30, produced by Texas Instrument. The Evaluation Module (EVM) of this processor is used in the development. The EVM consists of a TMS320C30 DSP chip, a PC host communication interfacing circuit and an analog interfacing circuit.

2 Power Circuit

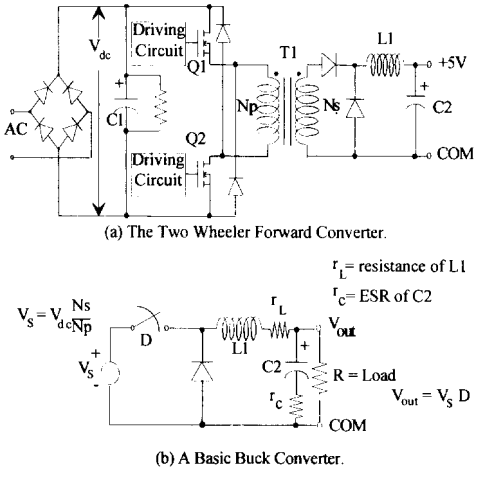

Fig.1 The Power Circuit of Two Wheeler Forward Converter

Fig. 1 (a) shows the two wheeler forward converter with 110 V ac input and 5 V dc output. The bridge rectifier BR1 rectifies the ac line to a raw high-voltage V_{dc} and the input capacitor C1 filters V_{dc} which in turn is fed into the MOSFETs Q1 and Q2. The MOSFETs are turned on and off simultaneously at a rate of 20 kHz, thus high-frequency ac voltage is produced across the transformer T1. The ac

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voltage is coupled to the secondary winding of the transformer, rectified and then filtered to dc voltage. The operation of the converter is the same as a buck converter (Fig.1 (b)). The input and output of a buck converter is related by

$V_{out} = V_S D$.....(1) where D is the duty cycle.

To design the DSP controller, the transfer function of the converter is required. For constant input voltage, the control-to-output transfer function [1] G(s) is

$$G(s) = \frac{V_{out}(s)}{D(s)}$$

$$G(s) = V_S \frac{sRC_2r_c+R}{s^2C_2L_1(R+r_c)+s[RC_2r_c+C_2r_L(R+r_c)+L_1]+r_L+R} \quad ...(2)$$

where $L_1 = 180\mu H$; $r_L = 0.2\Omega$;

$C_2 = 1000\mu F$; $r_C = 0.08\Omega$;

$V_s = 16.7$ V ; $R = 1\Omega$ (Full Load).

3 Z - Transform

The Z-transform is a highly valuable approach for formulating, analysing and solving problems in the discrete domain. Similar to the advantages of the Laplace transform in the continuous time domain, the major benefit is in the reduction of the complexity of equations to relatively simple algebraic equations. The basic Z-transform may be defined as follow

$$Z[f_i] = F(z) = \sum_{i=0}^{\infty} f_i z^{-i} \quad .....(3)$$

where z is a complex variable and f_i is a set of data which represents a continuous-time function sampled in discrete time interval. The complex variable in discrete domain is related to the complex variable in continuous time domain by

$z = e^{sT}$ .....(4) where T is the sampling period.

4 Sampling Frequency

The sampling theorem states that a sampled continuous signal may be reconstructed from its samples if and only if the frequency contents of the signal is lower than half of the sampling frequency. Therefore, the sampling frequency F_S of the A/D converter is at least two times the expected bandwidth of the system. In general, the sampling frequency should be as high as possible, but it is usually limited by the speed of the A/D converter and the DSP. Moreover, the power converter is actually discrete system because it is controlled by the duty cycle which can only be changed at discrete time. Therefore, a sampling rate higher than the operating frequency of the power converter is actually discrete system because it is controlled by the duty cycle which can only be changed at discrete time. For the DSP controller mentioned in this paper, the sampling frequency is chosen to be 10 kHz.

5 System Analysis

5.1 Difference Equation and Pulse Transfer Function

The DSP controlled power converter is represented by the block diagram shown in Fig. 2.

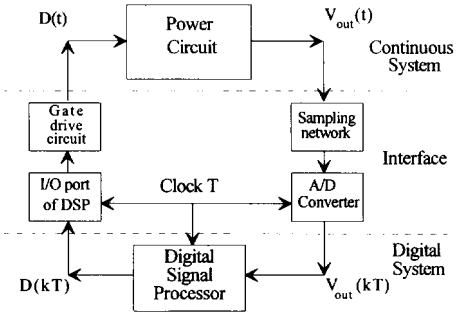

Fig. 2 Block Diagram of DSP Controlled Power Converter.

In Fig. 2, the A/D Converter converts continuous output signal $V_{out}(t)$ to digital form which is readable for DSP. The conversion is done at discrete instants so that the DSP receives the data $V_{out}(T)$, $V_{out}(2T)$....., $V_{out}(kT)$ at t = T, 2T.....kT respectively. When the DSP receives a data at kT, it processes the data and generates a constant frequency pulse signal with variable duty cycle D(kT). As the output of the converter is controlled by the duty cycle, the feedback loop is closed. The input data and the output of DSP are related by a linear difference equation with constant coefficients:

$$D(kT) + a_1D((k-1)T) + a_2D((k-2)T) + ...+ a_kD(0)$$
$$= b_0V_{err}(kT) + b_1V_{err}((k-1)T) + ...+ b_kV_{err}(0) \quad .....(5)$$

where $V_{err}(kT) = V_{out}(kT) - V_{ref}$

V_{ref} is a reference value and $V_{err}(kT)$ is the error voltage. Taking Z-transform in Equ. 5 and using the backward shift property of Z-transform,

$$K(z) = \frac{D(z)}{V_{err}(z)} = \frac{b_0z^k + b_1z^{k-1} + ... + b_k}{z^k + a_1z^{k-1} + a_2z^{k-2} + ... + a_k} \quad .....(6)$$

where K(z) is the Pulse Transfer Function (PTF) of the DSP controller. The concept of transfer function in frequency domain can be applied in digital system using pulse transfer function.

5.2 System Discretization

Continuous system can be discretized by Z-transform. The resultant PTF $G_0(z)$ of the discretized system is called the ZOH equivalent of G(s). $G_0(z)$ is given by

$$G_0(z) = (1 - z^{-1})Z[\frac{G(s)}{s}]$$

However, the digital controller is designed in such a way that the data transmission and processing time is exactly equal to T. This means the output voltage of the power converter sampled at t = kT will be used to compute the duty cycle of driving signal at t = (k+1)T. Therefore, there is one sampling period time delay for a signal to go through the feedback loop. Since the complex variable z represents one sample delay, the resultant PTF of the system will be

$$G_0(z) = \frac{(1-z^{-1})}{z} Z[\frac{G(s)}{s}] \quad \text{.....(7)}$$

$G_0(z)$ can be obtained by Equ. (2) and (7),

$$G_0(z) = \frac{(1-z^{-1})}{z} Z[\frac{G(s)}{s}] = K\frac{N_1 z + N_2}{z(z^2 + D_1 z + D_2)} \quad \text{.....(8)}$$

where $K = \frac{V_s R r_c}{L_1(R+r_c)}$;

$$N_1 = \frac{1}{w_0}(1 - \frac{ab}{w_0^2 + a^2})e^{-aT}\sin(w_0 T) - \frac{b}{w_0^2 + a^2}[e^{-aT}\cos(w_0 T) - 1] \ ;$$

$$N_2 = \frac{b}{w_0^2 + a^2}e^{-aT}[e^{-aT} - \cos(w_0 T)] - \frac{1}{w_0}(1 - \frac{ab}{w_0^2 + a^2})e^{-aT}\sin(w_0 T) \ ;$$

$D_1 = -2e^{-aT}\cos(w_0 T)$; $D_2 = e^{-2aT}$;

$$a = \frac{RC_2 r_c + C_2 r_L(r_c + R) + L_1}{2C_2 L_1(R + r_c)} ; \quad b = \frac{1}{C_2 r_c} ;$$

$$w_0 = \sqrt{\frac{r_L + R}{C_2 L_1(R + r_c)} - a^2}$$

5.3 Stability Criterion

When a system is analysed in frequency domain, its stability is depended on the locations of poles in the s-plane. The control theory states that the system is stable if all poles of the system transfer function are located in the left half plane of the s-plane. For Z-transform, the left half plane of the s-plane is mapped into the unity circuit in z-plane. (as shown in Fig. 3) Therefore, a digital system is stable if all the poles of the closed-loop pulse transfer function are located inside the unity circle.

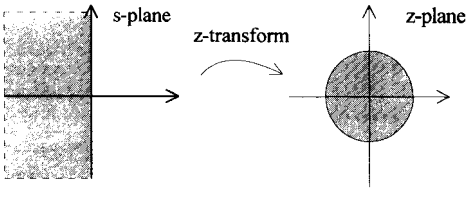

Fig. 3 The mapping of s-plane and z-plane

5.4 Frequency Response Analysis

Similar to continuous system, the frequency response of the discretized system can be evaluated. Then a suitable controller can be designed to achieve the optimum system performance. The gain-phase plot for the open-loop converter can be obtained by plotting

$$\text{Gain} = \sqrt{\text{Real}[G_0(e^{jwT})]^2 + \text{Imag}[G_0(e^{jwT})]}$$

$$\text{Phase} = \tan^{-1}\frac{\text{Imag}[G_0(e^{jwT})]}{\text{Real}[G_0(e^{jwT})]}$$

The gain and phase of $G_0(z)$ is plotted by MATLAB and shown in Fig. 4.

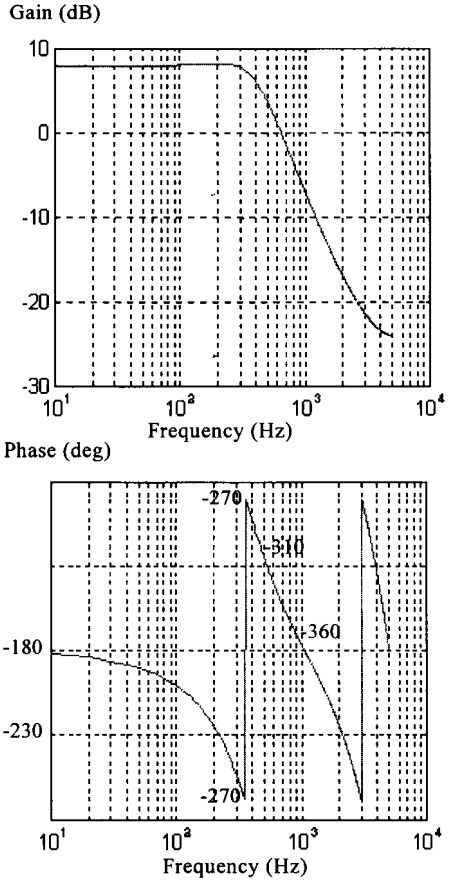

Fig. 4 Gain-Phase Plot of $G_0(z)$

6 Controllers Design

6.1 Analog Compensation Network

The circuit shown in Fig. 5 is often used to compensate the open-loop transfer function of switched mode power converter. This compensation network has very high DC gain and well controlled roll off. The transfer function [1] is

$$K(s) = \frac{V_k(s)}{V_{err}(s)} = -\frac{(s/s_{z1} + 1)}{s/s_{p1}(s/s_{p2} + 1)} \quad \text{.....(9)}$$

where

$$s_{z1} = \frac{1}{C_4 R_3} \; ; \; s_{p1} = \frac{1}{R_1(C_3 + C_4)} \; ; \; s_{p2} = \frac{C_3 + C_4}{R_3 C_3 C_4}$$

The error amplifier compensation network has high gain at low frequency. This enhances the gain of the system so that the line and load regulation can be improved. In contrast, the gain of the network decreases continuously at high frequency. Thus the high frequency ripple and noise from the output of the power converter cannot be magnified in the control loop. Moreover, the phase in between fz1 and fp2 is boosted up in order to obtain the optimum phase margin.

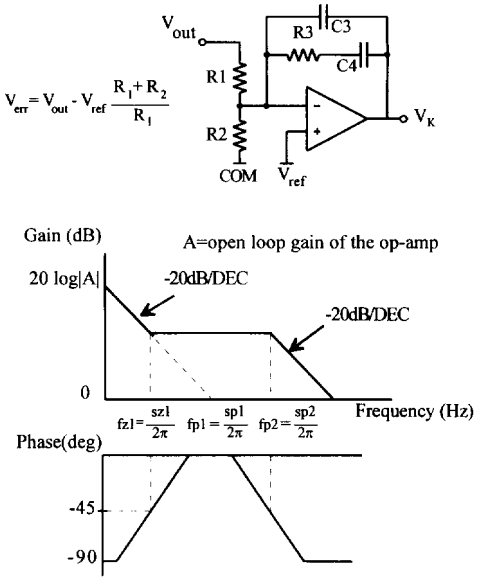

Fig. 5 Error Amplifier Compensation Network

By superimposing the gains and phases of the stages around the loop, the expected loop gain and phase of the overall system are generated. Using this method, a compensation network is designed and the loop gain and phase of the resultant converter are measured by Gain-Phase Analyser. The Gain-phase plot is shown in Fig. 6.

The bandwidth of the resultant converter is 1150 Hz and the phase margin is 40°.

6.2 Discretization of Analog Compensation Network

Analog compensation network can be discretized by bilinear transformation [2]. This transformation simply substitutes the complex variable s by

$$s = \frac{2}{T}\frac{1 - z^{-1}}{1 + z^{-1}}$$

Then the pulse transfer function of the discretized analog controller will be

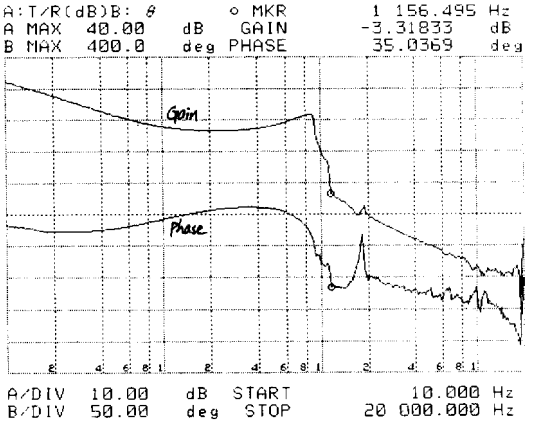

Fig. 6 Gain-phase Plot for K(s)G(s)

(Analog Compensation Network)

$$K(z) = K\left(\frac{2}{T}\frac{1 - z^{-1}}{1 + z^{-1}}\right)$$

$$= \frac{s_{p1} s_{p2} T}{2 s_{z1}}\left[\frac{(2 + s_{z1}T)z^2 + (2 s_{z1}T)z + (s_{z1}T^2 - 2)}{(2 + s_{p1}T)z^2 - 4z + (2 - s_{p1}T)}\right] \quad \text{.....(10)}$$

By inverse Z-transform, K(z) is transformed to a difference equation and implemented by the DSP.

The loop gain and phase of the resultant converter can be checked by MATLAB.

where

$$\text{Gain} = \sqrt{\text{Real}[K(e^{jwT})G_0(e^{jwT})]^2 + \text{Imag}[K(e^{jwT})G_0(e^{jwT})]^2}$$

$$\text{Phase} = \tan^{-1}\frac{\text{Imag}\left[K(e^{jwT})G_0(e^{jwT})\right]}{\text{Real}\left[K(e^{jwT})G_0(e^{jwT})\right]}$$

The loop gain and phase of the converter can be measured by Gain-Phase Analyser. The measured result is compared with the simulated result (dotted line) in Fig. 7.

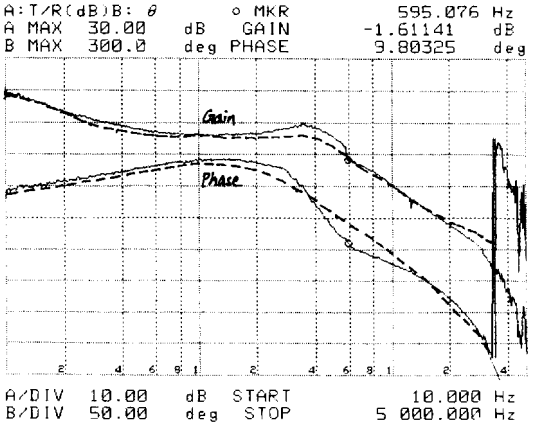

Fig. 7 Gain-phase Plot of $K(z)G_0(z)$

(Discretized Analog Controller)

The bandwidth of the closed-loop system is 590 Hz and the phase margin is 10° . It is a marginal design, however, the system is theoretically stable.

6.3 Digital PID Controller Design

To design a digital PID controller for the power converter, the transfer function of an analog PID controller is first considered.

$$K(s) = K_p + K_i\frac{1}{s} + K_d s$$

where K_p is the proportional gain, K_i is the integral gain, and K_d is the derivative gain.

Similar to the Laplace transform in continuous time domain, the integrator and differentiator can be represented by pulse transfer function in discrete domain.

$$\text{Integrator} = \frac{T(z+1)}{2(z-1)};$$

$$\text{Differentiator} = \frac{z-1}{Tz}$$

Thus the pulse transfer function of a digital PID controller is

$$K(z) = K_p + K_i\frac{T(z+1)}{2(z-1)} + K_d\frac{z-1}{Tz} \quad \text{.....(11)}$$

To simplify the design, K(z) can be designed such that the zeros of K(z) cancel the poles of $G_0(z)$. It can be easily done by selecting suitable values of K_p , K_i , and K_d. However, it is necessary to check the location of poles of the resultant closed-loop system. For a stable digital system, all the poles of the system should be located inside the unity circuit in z-plane.

The resultant pulse transfer function is transformed into a difference equation by inverse Z-transform and implemented by DSP.

The loop gain and phase of the resultant converter are plotted by MATLAB (dotted line) and Gain-phase analyser, the results are shown in Fig. 8.

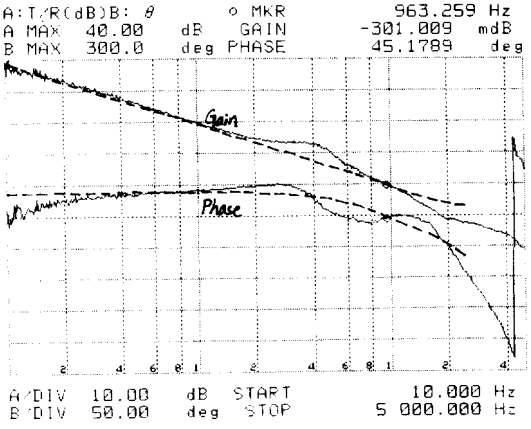

Fig. 8 Gain-phase Plot of $K(z)G_0(z)$ (PID Controller)

The bandwidth of the resultant converter is 963 kHz and the phase margin is 45°.

6.4 Deadbeat Controller Design

Deadbeat Control is also called Finite Settling Time Control which forces the output of the system to its expected value after a finite number of sampling intervals. To design a deadbeat controller, the $G_0(z)$ is directly transformed into a difference equation by using inverse Z-transform.

$$G_0(z) = \frac{V_{err}(z)}{D(z)} = K\frac{N_1 z + N_2}{z(z^2 + D_1 z + D_2)}$$

$$V_{err}(k) + D_1V_{err}(k-1) + D_2V_{err}(k-2) = KN_1D(k-2) + KN_2D(k-3)$$

Increasing k by one and by two in the above equation will give

$$V_{err}(k+1) + D_1V_{err}(k) + D_2V_{err}(k-1) = KN_1D(k-1) + KN_2D(k-2)$$

$$V_{err}(k+2) + D_1V_{err}(k+1) + D_2V_{err}(k) = KN_1D(k) + KN_2D(k-1)$$

Combining these equations will give,

$$V_{err}(k+2) + (D_2 - D_1^2)V_{err}(k) - D_1D_2V_{err}(k-1)$$
$$= KN_1D(k) + K(N_2 - N_1D_1)D(k-1) - KN_2D_1D(k-2)$$

As mentioned before, the digital controller has one sample delay. When the A/D converter samples a data $V_{err}(k)$ at kT , the deadbeat controller gives D(k) at (k+1)T (after one sample delay) and forces the $V_{err}(k+2)$ to zero at (k+2)T. Therefore, the expected output error is exactly equal to zero after two sampling period. To do so, let $V_{err}(k+2)$ equal to zero in the above equation,

$$D(k) = \frac{D_2 - D_1^2}{KN_1}V_{err}(k) - \frac{D_1D_2}{KN_1}V_{err}(k-1)$$
$$+\frac{N_1D_1 - N_2}{N_1}D(k-1) + \frac{N_2D_1}{N_1}D(k-2) \quad \text{.....(12)}$$

Then a difference equation of the deadbeat controller is obtained and it can be directly implemented by DSP.

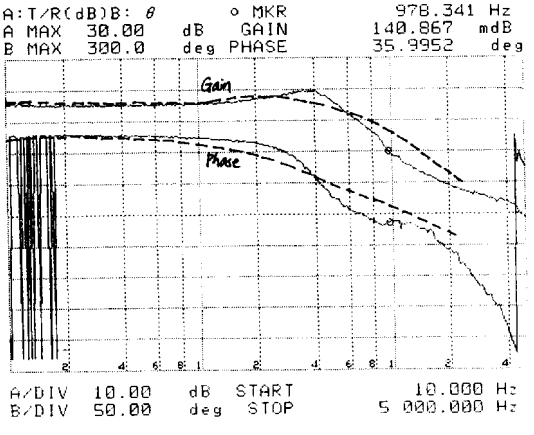

Fig. 9 Gain-Phase Plot of $K(z)G_0(z)$ (Deadbeat Controller)

The loop gain and phase of the resultant converter is shown in Fig. 9.

The bandwidth of the resultant system is 978 Hz and the phase margin is 35°.

6.5 Control Algorithm

A control algorithm should be designed and implemented by programming the DSP. The flow chart of the controller program is shown in Fig. 10.

The value of duty cycle is calculated by the difference equation which is obtained by the aforementioned methods.

6.6 Other Features

Besides the function of output regulation, the digital controller can perform the functions of over-voltage protection and soft start. Over-voltage protection is implemented by continuous checking the output voltage. When it is over the pre-set limit, the DSP will stop generating the driving signal and the power converter is shutdown. At the same time, soft start is implemented by increasing the duty cycle slowly when the control program is started.

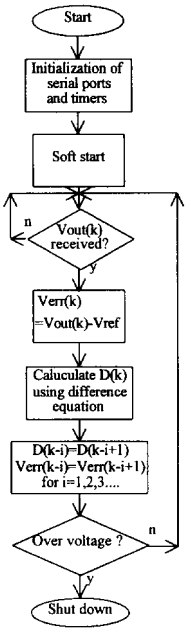

Fig 10. Flow Chart

7 Results and Discussions

To compare the performance of the controllers, the loop gain of the power converter at 10 Hz, the bandwidth and the phase margin are listed in the following table.

	Analog Controller	Discretized Analog Controller	Digital PID Controller	Deadbeat Controller
Bandwidth (Hz)	1,150	590	963	978
Phase Margin (degree)	40	10	45	35
Gain at 10 Hz	32	19	40	15

The result shows:-

a) the performance of the discretized analog controller is the most unsatisfactory;

b) the power converter with deadbeat controller has satisfactory bandwidth and phase margin but the controller is not capable of providing high gain at low frequency; and

c) the performance of digital PID controller is as good as the analog controller.

Designing the digital controller via analog design is simple and the control theory for continuous system can be applied. Therefore, discretization of analog controller is a good method for the designer who is familiar with analog design. However, this method gives an additional phase shift to the system, thus the performance of the resultant digital system is not as good as the continuous system.

PID controller design is catered for the characteristic of the power converter, the design can remove the original poles of the open-loop power converter and relocates it to the optimum position, it is the reason why PID controller has the most satisfactory performance.

The design of deadbeat controller is highly dependent on the accuracy of G(s) because the pulse transfer function is derived from the ZOH equivalent of G(s). For the deadbeat controller, the output error is forced to zero within two sampling periods, this usually requires a large variation of duty cycle. Since the range of duty cycle is limited, the requirement is not satisfied. Therefore the advantage of deadbeat controller is not obvious.

8 Conclusions

The DSP controller for a two wheeler forward converter is successfully designed by three methods:-

a) discretization of error amplifier compensation network;

b) PID control; and

c) Deadbeat control.

The DSP controller designed by the above methods is capable of controlling the output of the converter. By loop gain and phase measurement, the performance of the DSP controller is evaluated. The result shows that PID control is the best design method for implementing the DSP controller. Since the controller is implemented by software, the design is simple and flexible. For this reason, soft start and over-voltage protection is easily implemented in the power converter.

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