A Fast Response Full Bridge Power Factor Corrector

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ABSTRACT

A fast response Full Bridge Power Factor Corrector (FBPFC) is presented in this paper. The converter is combined by two interleaved boost cells and a conventional full bridge converter. As the interleaving technique is applied, the input ripple current of FBPFC are reduced. Experimental result shows that the maximum power factor is 0.98 even without input filter.

I. INTRODUCTION

As the IEC1000-3-2 becomes compulsory requirement for the electronic equipment in Europe, a front end Power Factor Pre-regulator (PFP) is usually installed to an ac/dc converter in order to reduce input harmonic currents and increase power factor. Boost PFP is always designed to have poor dynamic response because of the inherent low frequency ripple voltage at its output capacitor, therefore, a dc/dc converter must be there to give fast output regulation. To improve size, cost and efficiency of the power converter, many researches have investigated the possibility of simplifying the two-cascade-stage system by combining the power switches in the boost converter and the dc/dc converter [1-4]. For the dc/dc converter, duty cycle and switching frequency of its power switches should be constant when its output is well regulated. However, duty cycle or switching frequency of boost PFP operated in Continuous Inductor Current Mode (CICM) vary with its sinusoidal input voltage. Thus it is impossible to combine the power switches of the two converters. The solution for this discrepancy is to operate the boost PFP in Discontinuous Inductor Current Mode (DICM) because input current of a DICM boost converter can naturally follow the sinusoidal input voltage with constant switching frequency and duty cycle. Unfortunately, the combined converter has the following drawbacks: 1) DICM boost PFP draws pulsating input current and the peak input current is much higher than that of a CICM boost PFP. As the combined converter have the same property, its high input ripple current makes the design of input filter difficult [5,9]. 2) The combined converter has an energy storage capacitor. Voltage across the capacitor is very high at light load, this increases voltage stress on the energy storage capacitor and power switches [2].

Interleaving technique [6-9] is an effective method to reduce the input ripple current of DICM boost PFP. Using this technique, part of the ripple current can be canceled out and the peak current is also reduced as the input current is shared by a number of boost cells. The improvement is very obvious when just two boost cells are used [9]. If more than one boost cells are used, then it is worth to consider combining this interleaved PFP with multiple switches dc/dc converter (e.g. full bridge converter).

For the second drawback, R. Redl [2] suggested to operate the dc/dc converter in DICM because the energy storage capacitor voltage becomes independent from the load when both the boost PFP and the dc/dc converter operate in DICM.

In this paper, the interleaving technique will be briefly introduced. The interleaved boost PFP are compared with the single cell boost PFP. Then a fast output response Full Bridge Power Factor Corrector (FBPFC) which is combined by two interleaved boost cells and a conventional Full Bridge Converter (FBC) will be presented. As interleaving technique is applied in the FBPFC, its input ripple current is lower than a common DICM PFP. Moreover, the output response of the

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FBPFC is as fast as a common ac/dc converter since its output section is a conventional FBC. Its operating principle and some design considerations are explained in detail. The output section of the FBPFC is designed to operate in DICM when the energy storage capacitor voltage exceed a predefined limit. Finally, a 200W FBPFC is built and tested to verify the design.

II. INTERLEAVING TECHNIQUE

An interleaved boost PFP is shown in fig. 1. The PFP is constructed by two boost cells, all boost cells are kept running in DICM.

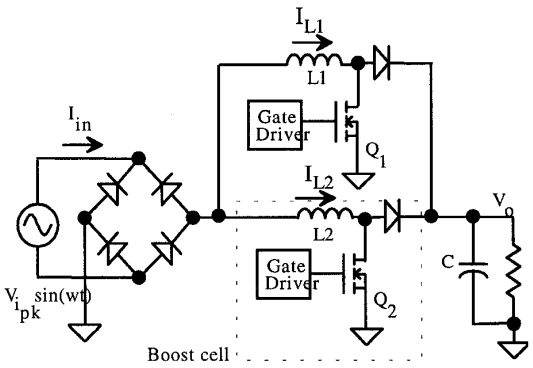

Fig. 1. Interleaved power factor pre-regulator.

The driving signal of one cell is shifted in time by an appropriate amount to other cells as shown in fig. 2.

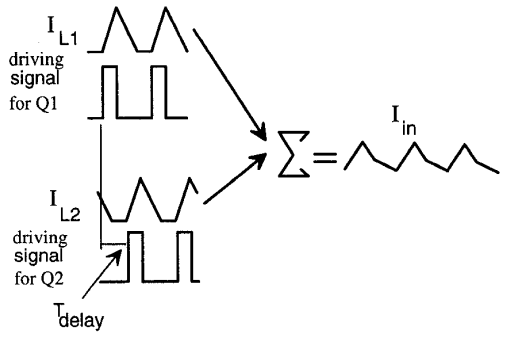

Fig. 2. Interleaving technique.

As the input current of the whole PFP is the sum of the inductor current of two boost cells, the resultant ripple current is reduced. It is intuitively known that the most effective way to minimize the ripple current is setting T_{delay} equal to half switching period so that the current pulses can be evenly distributed within a switching period.

III. COMPARISON OF INTERLEAVED DESIGN WITH SINGLE CELL DESIGN

In this section, a 2-cells interleaved boost PFP and a single boost PFP are compared. The comparison includes input inductor (inductance, copper loss and size), input peak current, and the current rating of their components. To have a fair comparison, the PFPs are assumed to have same rated input power. The input power of a DICM boost cell [5] is

$$P = \frac{V_{ipk}^2 D^2 T_s}{2\pi L} \int_0^{\pi} \frac{\sin^2\theta}{1-\alpha\sin\theta} d\theta \qquad (1)$$

where $\alpha = \frac{1}{M} = \frac{V_{ipk}}{V_o}$, D is the duty cycle and T_s is the switching period.

A. Rated input power of a DICM boost cell

The input power is directly proportional to the square of duty cycle. Before considering the rated power of a boost cell, the maximum allowable duty cycle should be first determined. To keep a boost cell operated in discontinuous mode, the off time of power switch should be long enough for the inductor current fall to zero before the starting of another cycle. Therefore, the criterion for discontinuous mode is

$$T_{on} + T_d \le T_s \qquad (2)$$

where $T_{on} = DT_s$ and T_d is the conduction time of the output rectifier. As the maximum value of T_d is

$$T_{d(\max)} = \frac{V_{ipk}}{V_o - V_{ipk}} T_{on} = \frac{1}{M-1} T_{on} \qquad (3)$$

that means the criterion becomes

$$D(1 + \tfrac{1}{M-1}) \le 1 \quad \text{or} \quad D \le 1 - \alpha \qquad (4)$$

Therefore, the rated power of the DICM boost cell will be

$$P_r = \frac{V_{ipk}^2 (1-\alpha)^2 T_s}{2\pi L} \int_0^{\pi} \frac{\sin^2\theta}{1-\alpha\sin\theta} d\theta \qquad (5)$$

B. Inductance of input inductor

For an interleaved PFP, power is shared by the cells and the rated power handled by an individual cell will be $P_r/2$. If the requirement of input voltage, output voltage, switching frequency and rated power are identical, then the inductance of the input inductor in the interleaved PFP should be

$$L_i = 2 \times L_s \tag{6}$$

where L_s is the inductance of the input inductor in a single cell PFP with rated power P_r because the power is inversely proportional to the inductance according to (5).

C. Peak current

The peak current drawn by a single cell PFP is

$$I_{pk,s} = \frac{V_{i_{pk}} T_{on}}{L_s} \tag{7}$$

For an interleaved PFP, the peak current drawn by each cell will be

$$I_{pk,i} = \frac{V_{i_{pk}} T_{on}}{2L_s} = \frac{I_{pk,s}}{2} \tag{8}$$

As the peak current is proportional to the average current in the inductor, power switch and output rectifier, the current rating of these components in the interleaved PFP is half of that in a single cell PFP.

D. Copper loss and size of input inductor

In designing the size of magnetic components, copper loss is an important factor to be concerned as it is the main cause of thermal problem. For a single cell PFP, the copper loss of the inductor is calculated by

$$P_{cl} = I_{av}^2 R_c = I_{av}^2 \frac{\rho n l}{A_c} \tag{9}$$

where I_{av} is the average current flow in the inductor, R_c is the equivalent resistance of the inductor wire which is equal to $\frac{\rho n l}{A_c}$ (ρ = resistivity of copper, A_c = effective cross section area of the copper wire, n = number of turns of inductor winding, l = length of copper wire per turn). Note that l is approximately equal to a constant if the n and A_c is small.

If the inductor is redesigned with the same core for the interleaved PFP, the average current flow will be equal to $I_{av}/2$, the number of turns will be $\sqrt{2} \cdot n$ (as inductance is proportional to n^2) according to the previous sections.

Assume each inductor of an interleaved PFP can tolerate the same copper loss without causing thermal problem, the required cross section area $A_{c,i}$ of the copper wire can be found by

$$P_{cl} = I_{av}^2 \frac{\rho n l}{A_c} = \left(\frac{I_{av}}{2}\right)^2 \frac{\rho \sqrt{2}\, n l}{A_{c,i}}$$

$$\text{i.e. } A_{c,i} = \frac{1}{2\sqrt{2}} A_c \tag{10}$$

For the inductor of single cell PFP, the volume of copper is nlA_c. Comparing to the inductor of the interleaved PFP, the volume of copper is

$$\sqrt{2}\, nl \frac{1}{2\sqrt{2}} A_c = \frac{1}{2} nlA_c \tag{11}$$

Therefore, the copper volume of the input inductor in the interleaved PFP is half of that in a single cell PFP. Since the size of an inductor is related to the volume of copper wire, the individual inductor in the interleaved PFP is smaller than that in a single cell PFP. However, total copper loss is doubled comparing to a single cell PFP and this may cause loss of efficiency.

IV. FULL BRIDGE PFC CONVERTER WITH CONVENTIONAL OUTPUT SECTION

A. Operating principle

A FBPFC is shown in fig. 3. It consists of a conventional FBC and two interleaved boost cells with the power switches of the boost cells and FBC (Q_1 and Q_2) combined.

Control strategy of the power switches is same as that of a conventional FBC but the actual path of power flow is slightly different. When Q_1 and Q_3 are turned on, energy stored in the capacitor C_1 is transferred to output through an isolation transformer. At the same time, current through L_1 will rise as Q_1 provides a current path. When all switches are turned off, energy stored in the output inductor L_o sustain the output current and energy stored in L_1 is transferred to C_1 through the body diode of Q_4. Similarly, current through L_2 will rise and energy in C_1 is transferred to output when Q_2 and Q_4 are turned on. Since Q_1 and Q_2

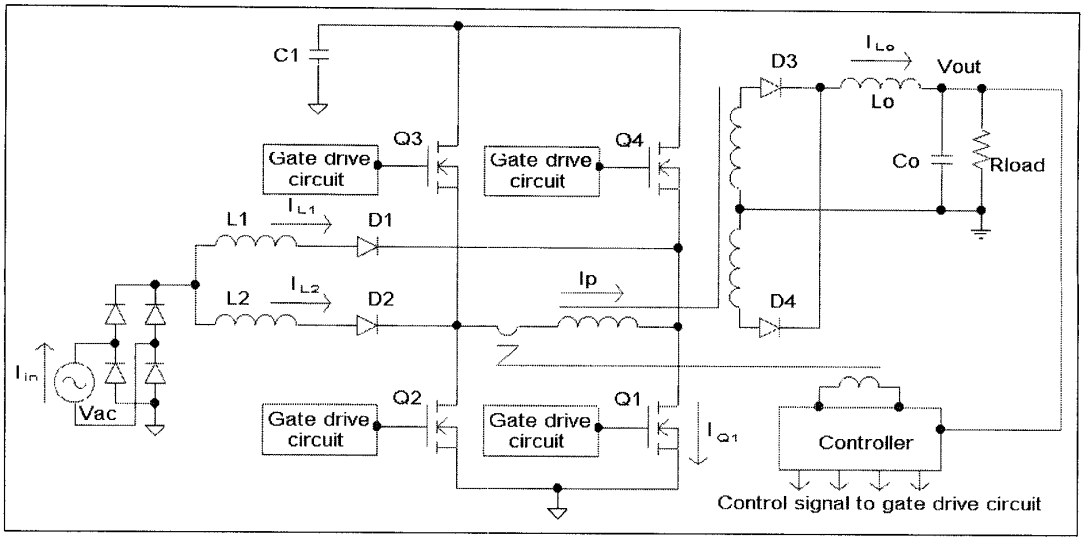

Fig. 3. The Full Bridge PFC Converter.

are turned on alternately, the inductor current I_{L1} and I_{L2} are out of phase and some of the ripple current in I_{in} is canceled out.

V. DESIGN CONSIDERATION

To design the FBPFC, one of the considerations is the energy storage capacitor voltage V_{C1}. High V_{C1} is usually undesirable because this require a high breakdown voltage power switch. The magnitude of V_{C1} depends on both the input line voltage and output power, and a lower V_{C1} is generally obtained at low line and high load.

For the full bridge converter, the steady state voltage ratio is

$$\frac{V_o}{V_{C1}} = 2DT_r \tag{12}$$

where T_r is the transformer truns ratio. Noted that the effective switching frequency of a FBC is 2 times the switching frequency of the power switches, therefore, the value of duty cycle is multiplied by 2.

For the input power of the FBPFC is the sum of power drawn by the two boost cells, combining (1) and (12) will give

$$P_{in} = 2P = \frac{a^2 V_o^2 T_s}{4L_1 T_r^2 \pi} \int_0^{\pi} \frac{\sin^2\theta}{1-a\sin\theta} d\theta \tag{13}$$

Note that $\alpha = \frac{V_{i_{pk}}}{V_{C1}}$. Using (13), the value of V_{C1} can be found by numerical iteration method.

The controller of FBPFC (Fig. 3) is very simple, a common voltage feedback or current mode dual output controller (e.g. UC3846) can be adopted. However, current mode PWM controller is a better choice because it can avoid flux saturation due to volt-seconds unbalance in the transformer. As the current through the power switches Q_1 and Q_2 is the sum of primary current I_p and input inductor current, it is not suitable to be used as control signal like other current mode controlled converters. Therefore, I_p should be used as the current control signal instead. The primary current is fed to the controller through a current transformer (as shown in fig. 3) and a full wave rectifier.

VI. DESIGN EXAMPLE

A FBPFC is designed with the following specification:

Input power: $P_{in} = 200W$,
Input line range: $V_{in} = 80\text{-}140V$,
dc output voltage: $V_o = 48V$,
Switching frequency: $F_s = \frac{1}{T_s} = 20kHz$,
Range of V_{C1}: < 400V,
Output hold up time: $t_{hold\text{-}up} > 10ms$

To provide sufficient hold up time, the maximum duty cycle and the minimum value of V_{C1} should be considered. Duty cycle should be less than 0.5 for a FBC. (In fact, it should be

around 0.46 because the driving signal should have some dead time.) Considering the critical condition -- full load and low line (80V), the steady state duty cycle is maximum and V_{CI} is minimum under this condition. The value of α is also maximum under this condition. If V_{C1} is set equal to 200V under this condition, then

$$\alpha_{\max} = \frac{80\times\sqrt{2}}{200} = 0.57 \quad (14)$$

To meet the criterion mentioned in section III-A, the maximum steady state duty cycle should be

$$D_{\max} = 1 - \alpha_{\max} = 0.43 \quad (15)$$

If duty cycle is set equal 0.4 in the low line and full load condition, then the transformer truns ratio T_r from (12) is equal to

$$T_r = \frac{V_o}{2DV_{C1}} = \frac{48}{2\times0.4\times200} = 0.3 \quad (16)$$

When ac line is cut off, V_{CI} will drop and duty cycle will be increased in order to sustain the dc output until reaching its limited value (0.46). That means the dc output can be sustained until V_{CI} drop to a value V'_{C1} which can be calculated by (12)

$$V'_{C1} = \frac{48}{2\times0.46\times0.3} = 174V \quad (17)$$

Energy released from C_1 should provide 200W power for 10ms, therefore, the required capacitance of C_1 can be calculated by the following energy equation:

$$P \times t_{hold-up} = \frac{1}{2}C_1(V_{C1}^2 - V_{C1}'^2) \quad (18)$$

$$C_1 = \frac{2\times200\times0.01}{200^2-174^2} = 411\mu F \quad (19)$$

That means a 470μF electrolytic capacitor is sufficient to meet the hold-up time requirement.

On the other hand, the required inductance of the input inductors can be calculated by (13)

$$L_1 = \frac{\alpha^2 V_o^2 T_s}{4P_{in}T_r^2\pi}\int_0^{\pi}\frac{\sin^2\theta}{1-\alpha\sin\theta}d\theta = 0.5mH \quad (20)$$

Having these component values, the values of V_{CI} under different condition can be calculated by (13). The result is shown in fig. 4.

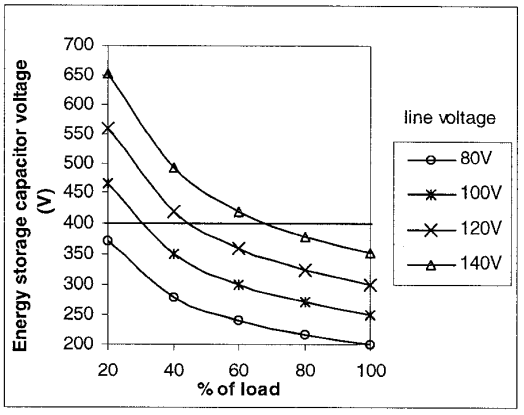

Fig. 4 V_{C1} vs percentage of load. (Data from calculation)

From fig. 4, V_{CI} exceeds the limit (400V) when the line voltage is 140Vac and the output load is below 60%. In order to limit V_{CI}, the output section of the FBPFC should be operated in DICM when the limit is reached and this can be done by a proper design of the inductance of output inductor. When the output section is operated in the borderline of DICM, the average output current I_o will be equal to half of the peak output inductor current ΔI . For output power equal to 120W (60% full load),

$$\Delta I = 2I_o = \frac{2P_o}{V_o} = 5A \quad (21)$$

The equation describing the output section of the FBPFC is

$$V_{C1}T_r - V_o = L_o\frac{\Delta I}{DT_s} \quad (22)$$

By (21) and (22), the required output inductance is found to be 144 μH.

VII. EXPERIMENTAL RESULT

To verify the design, a FBPFC is built and tested under different condition. A controller is designed to stabilize the converter for the output section operated in both CICM and DICM. Output regulation of the FBPFC is tested by stepping the output load from 10% to 100% at a frequency 50Hz. The result (fig. 5) shows that recovery time is within 5ms and overshooting and undershooting voltage are within 2% of the output voltage. The output response is as fast as a common ac/dc converter.

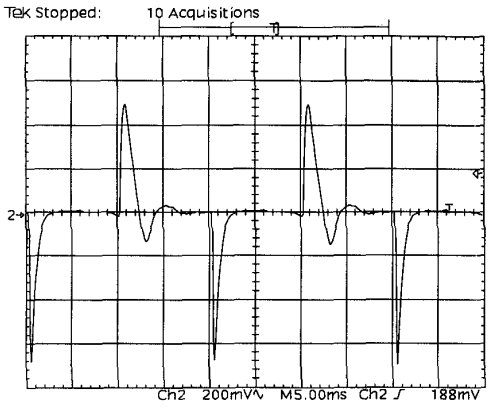

Fig. 5. Result of output transient test.

The energy storage capacitor voltage is measured and plotted in fig. 6, it shows that the values of V_{C1} stay within the limit.

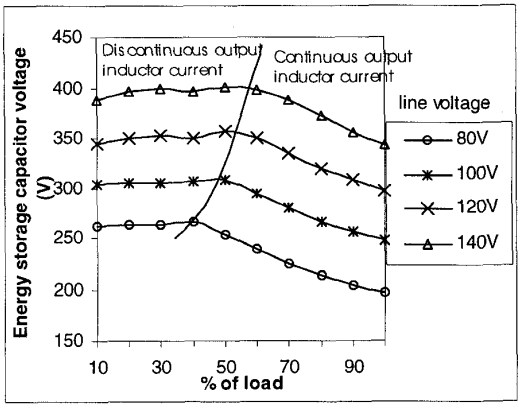

Fig. 6. V_{C1} vs percentage of load. (Data from experiment)

When the load drops below a certain limit, output section of the FBPFC goes into DICM and V_{C1} will stop increasing. Input current of the FBPFC operated in full load is shown in fig. 7, it shows that the input current envelop (the lower trace) can follow the sinusoidal input voltage (the upper trace) and some ripple current is canceled out. At full load and low line, the power factor is maximum and found to be 0.98 even without input filter.

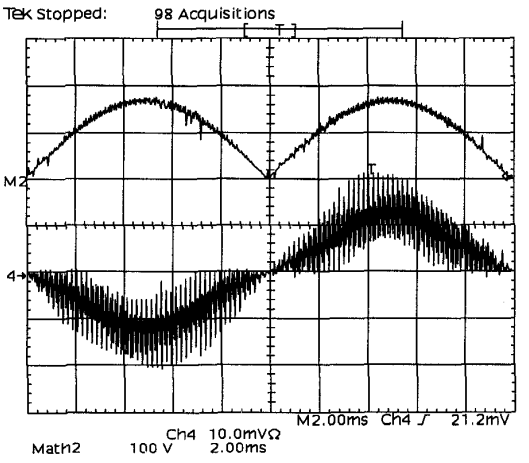

Fig. 7. Rectified input line (upper trace) and input current - 2A/div. (lower trace)

VIII. CONCLUSION

Table I. summarize the comparison result of an interleaved PFP and a single cell PFP.

Table I. Comparison of interleaved PFP and single cell PFP

	Single cell PFP	Interleaved PFP
Rated Power for each cell	P_r	$P_r/2$
Peak/average current in the component	$I_{pk,s}$	$I_{pk,s}/2$
Current rating of power switch and output rectifier	I_r	$I_r/2$
Inductance of input inductor in each cell	L_s	$N \times L_s$
Copper volume of individual inductor	nlA_c	$nlA_c/2$
Total copper loss of inductors	P_{cl}	$2 \times P_{cl}$

Although the interleaving technique increases the component count, the actual increase of cost may be not significant. It is because using more boost cells can share the current flow in the inductors and power switches so the lower current rating devices (lower price) can be adopted. Actually, some high power PFP use more than one power switches and output rectifiers because the high current rating device is not available in the market.

A Full Bridge Power Factor Corrector (FBPFC) is designed and evaluated, the result shows that the output response is as fast as a common ac/dc converter and it draws sinusoidal input current. As interleaving technique is applied, the input peak current and the current ripple are much lower than that of other DICM boost PFP. The result shows that the maximum power factor is 0.98 even without input filter. The voltage of energy storage capacitor is also limited to an acceptable level by designing the output section operated in DICM at light load.

REFERENCES

[1] M. Madigan, R. Erickson and E. Ismail, "Integrated high quality rectifier-regulators", Proceedings of PESC '92, pp. 1043-1051.

[2] R. Redl, L. Balogh and N. Sokal, "A new family of single-stage isolated power-factor correctors with fast regulation", Proceedings of PESC ' 94, pp. 1137-1144.

[3] Y. Jiang and F. C. Lee, "Single-stage single-phase parallel power factor correction scheme", Proceedings of PESC ' 94, pp. 1145-1151.

[4] M. M. Jovanovic, Dan M. C. Tsang and F. C. Lee, "Reduction of voltage stress in integrated high-quality rectifier-regulators by variable-frequency control", Proceedings of APEC ' 94, pp. 569-575.

[5] Kwang-Hwa Liu and Yung-Lin Lin, "Current waveform distortion in power factor correction circuits employing discontinuous-mode boost converters", Proceedings of PESC ' 89, pp. 825-829.

[6] Laszlo Balogh and Richard Redl, "Power-factor correction with interleaved boost converters in continuous-inductor-current mode", Proceedings of APEC ' 93, pp. 168-174.

[7] Brett A. Miwa, David M. Otten and Martin F. Schlecht, "High efficiency power factor correction using interleaving techniques", Proceedings of APEC ' 92, pp. 557-568.

[8] Michael S. Elmore, "Input current ripple cancellation in synchronized, parallel connected critically continuous boost converters", Proceedings of APEC ' 96, pp. 152-158.

[9] C.H. Chan and M.H. Pong, "Input current analysis of interleaved boost converters operating in discontinuous-inductor-current mode", Proceedings of PESC '97.