A PFC Topology with Low Input Current Distortion Suitable for Aircraft Power Supplies

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Abstract—This paper presents an AC-DC converter topology for realization of PFC converters for applications where the mains frequency is high and a low input current harmonics is required, e.g., in aircraft power systems. The proposed topology eliminates crossover distortion due to the presence of input rectifiers and the inevitable input current phase lead. The idea is to stack a DC voltage on top of the AC mains voltage to prevent voltage polarity reversal in the input, eliminating the input bridge rectifier. This eliminates the crossover distortion, which can be significant for supply systems having a high mains frequency. In addition, the proposed PFC converter allows bi-directional energy flow, ensuring all inductors work in continuous conduction mode and hence eliminating the distortion due to the abrupt change of dynamic response when the operating mode changes. Analysis and design of the power and control circuits will be given and discussed. An experimental system will be presented for verification purposes.

Fig. 1. Crossover distortion

Fig. 2. Distortion due to mode change

I. INTRODUCTION

The aim of PFC converters is to reduce the input current harmonics and provide high power factor to the AC mains supply. A bridge rectifier followed by a boost converter operating at critical conduction mode or in continuous conduction mode under average current mode control is being widely used for PFC applications because of its simplicity [1],[2]. Researchers have revealed two major distortions in boost type PFC configurations [3],[4].

1) It has been shown by Sun [3] that the use of average current mode control method and a filtering capacitor placed after the input bridge rectifier for eliminating high-frequency ripple current will introduce a leading phase to the input current relative to the input mains. Near the zero crossing point of the input AC voltage, the input current reverses in advance of the voltage due to the phase lead, and the input bridge rectifier will be reverse biased and cease to conduct current. This causes a step change in the input current and gives rise to crossover distortion. The significance of this distortion increases with the mains frequency and can be very serious when the power system operates at 400 Hz or above in airborne applications.

2) Another distortion is caused by the change of operating mode of the boost inductor when the load and/or input voltage is changed. The dynamics of the converter changes abruptly, causing distortion to the input current. Although critical conduction mode operation can alleviate the problem, it is undesirable for high power applications since the high ripple current flow in the inductor and switches increases the conduction loss. Moreover, the problem can be reduced by adding a
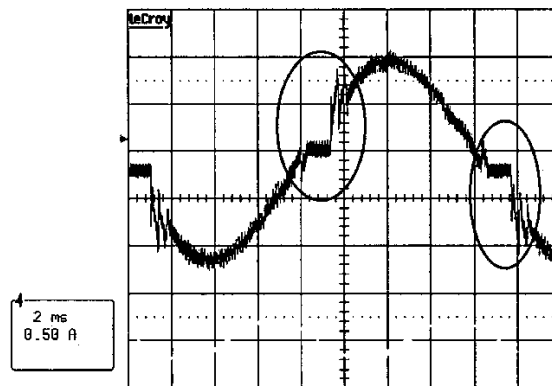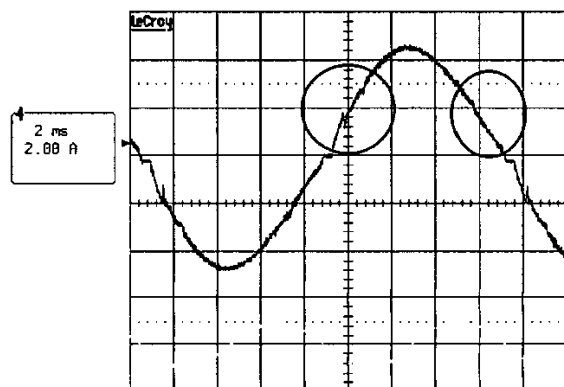
special correction factor to the input current sampling circuit [4], at the expense of an increased complexity of the control circuits.

Figure 1 shows the crossover distortion of input current of a PFC caused by the phase lead of input current to the mains voltage and the input bridge rectifier. Figure 2 shows the distortion at the change of operating mode.

In this paper we propose a PFC converter topology that can eradicate the distortions described above. This topology is based on the rectifierless AC-DC conversion topology presented in [5], which uses two DC-DC converters to provide a DC stacking voltage to the AC input voltage, thereby preventing polarity change of the input voltage and hence eliminating the need for input rectifiers. The basic configuration is shown in Fig. 3 (a). In particular, the specific choice of constituent DC-DC converters, as shown in Fig. 3 (b), has been found
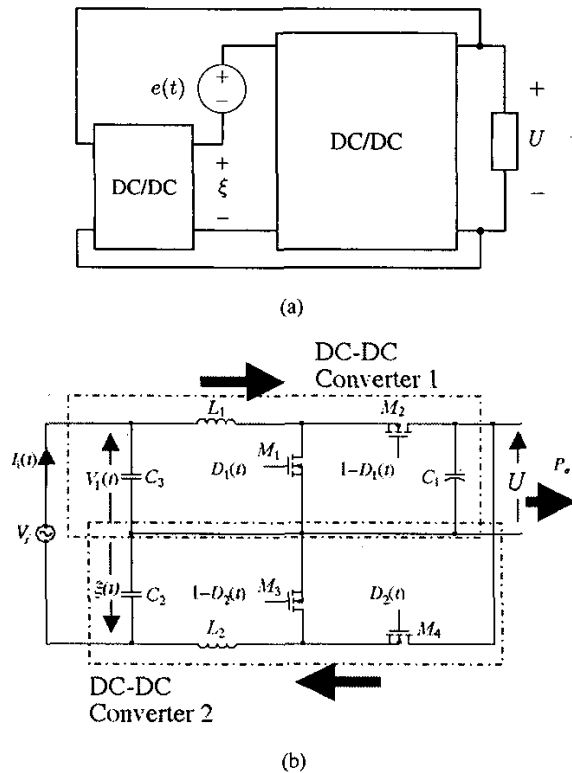
(a)

(b)

Fig. 3. Rectifierless AC/DC converter circuit. (a) General configuration; (b) specific circuit choice.
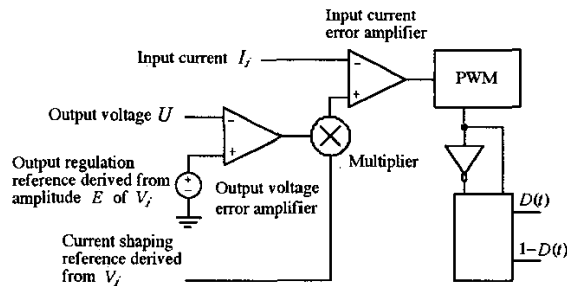

Fig. 4. Control circuit for power factor correction

to have lowest voltage stress on the switches and is selected for the implementation of PFC converters. Moreover, it has been revealed [5] that this rectifierless topology suffers from circulating power loss, which becomes significant when the stacking voltage is large. Thus, in this paper, instead of using a constant DC stacking voltage, we introduce a variable stacking voltage, resulting in significant reduction of the circulating power and loss.

In Section II, we will review the operation of the proposed circuit, and explain how circulating power loss can be reduced in this circuit. In Section III we will present experimental results verifying the operation of the circuit and its ability of eliminating distortion at high line frequency (400 Hz). Finally, Section IV gives the conclusion.

II. OPERATION ANALYSIS

The power conversion stage consists of two DC-DC bi-directional converters, as shown in Fig. 3 (b). DC-DC converters 1 and 2 are boost and buck converter according to the power flow directions shown by the solid arrows. To realize the input rectifierless AC-DC conversion, DC-DC converter 2 should provide a stacking voltage $\xi(t)$ to the mains Vi such that the input voltage of DC-DC converter 1, V_1, is always positive regardless of V_i. To satisfy this condition, the output voltage U and $\xi(t)$ must satisfy

$$U > D_2(t)U = \xi(t) > E\sin 2\pi f_e t \quad \text{for all } t \quad (1)$$

where all symbols are defined in Fig. 3.

This implies that U must be greater the amplitude of the input AC voltage E and the overall conversion is a step-up operation. Since the conversion ratio of DC-DC converter 1 is equal to $1/(1 - D_1(t))$, the relationship between U, V_i, $D_1(t)$ and $D_2(t)$ is given by

$$U = \frac{V_i}{1 - D_1(t) - D_2(t)}. \quad (2)$$

A. Reduction of Circulating Power

The topology used for PFC converter implementation has a drawback in conversion efficiency due to circulation power. It has been shown in [5] that the circulating power is equal to $4\xi/\pi E$ times the output power P_o when stacking voltage ξ is kept constant. This means that the minimum circulating power flows around DC-DC converters 1 and 2 is $4P_o/\pi$ since ξ must be greater than E. To reduce the circulating power, we proposed to add a time varying component, which is in anti-phase to V_i, to the stacking voltage in order to provide "just enough" stackup DC voltage during the negative cycle. It can be done by equating the duty cycle of M_1 and M_2, i.e., $D_2(t) = D_1(t) = D(t)$. Under this condition, the stacking voltage $\xi(t)$ as well as the output voltage U and the input voltage to DC-DC converter 1 can be derived as follows.

$$U = \frac{V_i}{1 - 2D(t)} \quad \text{or} \quad D(t) = \frac{1}{2}\left(1 - \frac{V_i}{U}\right) \quad (3)$$

$$\xi(t) = D(t)U = \frac{1}{2}(U - V_i) \quad (4)$$

$$V_1(t) = \xi(t) + V_i = \frac{1}{2}(U + V_i). \quad (5)$$

We can see that $\xi(t)$ contains a time varying component $V_i/2$, which is in antiphase to V_i. In addition, (5) shows that V_1 is always positive with $U > E$ and satisfies the basic requirement.

To derive the circulating power when the converter operates for PFC, we can assume that the input current I_i is controlled to follow the shape of the mains V_i with amplitude equal to $2P_o/E\eta_{overall}$, where $\eta_{overall}$ is the overall efficiency of the converter, i.e.,

$$I_i = \frac{2P_o}{E\eta_{overall}}\sin 2\pi f_e t. \quad (6)$$

Then, the circulating power $P_{circulate}$ is given by [5]

$$P_{circulate} = 2f_e \int_0^{1/2f_e}(V_i + \xi(t))I_i.dt - P_o$$

$$= \left(\frac{2U}{\pi E \eta_{\text{overall}}} - \frac{1}{2} \right) P_o. \qquad (7)$$

It can be seen that the minimum circulation power $(2/\pi - 1/2)P_o$ can be achieved when U is made close to E. The circulating power is reduced by a factor of 9.32 when compared with $4P_o/\pi$.

Obviously, if η is the efficiency of each constituent converter, the total loss due to the circulating power is

$$\text{loss}_{\text{circulate}} = 2P_{\text{circulate}} \left(\frac{1}{\eta} - 1 \right). \qquad (8)$$

Also, as power goes directly to the output through DC-DC converter 1, the loss is

$$\text{loss}_{\text{direct}} = P_o \left(\frac{1}{\eta} - 1 \right). \qquad (9)$$

Hence, the overall efficiency is

$$
\begin{aligned}
\eta_{\text{overall}} &= \frac{P_o}{P_o + \text{loss}_{\text{circulate}} + \text{loss}_{\text{direct}}} \\
&= \frac{P_o}{P_o + P_o \left(\frac{1}{\eta} - 1 \right) \left(\frac{4U}{\pi E \eta_{\text{overall}}} \right)} \\
&= 1 - \frac{4U}{\pi E} \left(\frac{1}{\eta} - 1 \right).
\end{aligned} \qquad (10)
$$

Alternatively, we can write

$$\eta = \frac{1}{1 + \frac{\pi E}{4U} (1 - \eta_{\text{overall}})} \qquad (11)$$

which can be used to estimate the constituent converter efficiency from the measured overall efficiency.

B. Control Circuit Realization for PFC

The simplified control circuit shown in Fig. 4 is used for the PFC control. The input current error amplifier forces the input current to follow the reference derived from V_i. The reference voltage for regulating the output voltage U is made proportional to the input voltage amplitude. This makes U decrease with E and reduces the ratio U/E at low AC voltage input which helps to reduce circulation power derived in (7). The theoretical basis of the control possibility has been discussed in [2],[6].

III. EXPERIMENTAL RESULTS

A PFC converter using the proposed topology has been built for verification. The output voltage was made to vary with the input mains amplitude as described in the previous section. Some test results are shown in Table I.

From the results of Test 1 and using (11), we can estimate the constituent converter efficiency η, i.e., $\eta = 96.6\,\%$. We can check consistency with the results of Test 2. Assuming $\eta = 96.6\,\%$ for Test 2, we get the overall efficiency as 86.5 %, which agrees with the measured one.

Figure 5 shows the operating waveforms of V_1, $\xi(t)$, V_i and I_i. We can see that $\xi(t)$ is in anti-phase to V_i and its magnitude reduces when V_i is positive in order to reduce the circulation power.

Figures 6 and 7 show the operating waveforms at 400 Hz mains frequency and no significant distortion has been found.
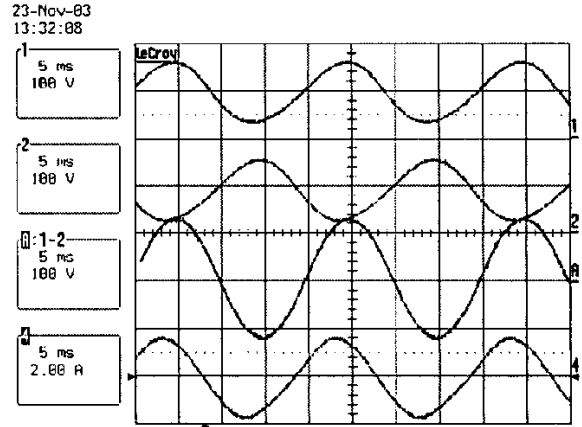

Fig. 5. Waveforms of V_1 (Ch1), $\xi(t)$ (Ch2), V_i (ChA) and I_i (Ch4), for input voltage 90 V (rms) and line frequency 50 Hz.
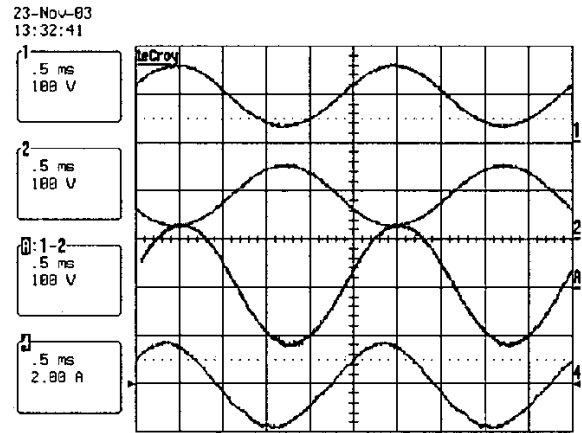

Fig. 6. Waveforms of V_1 (Ch1), $\xi(t)$ (Ch2), V_i (ChA) and I_i (Ch4), for input voltage 230 V (rms) and line frequency 400 Hz.

TABLE I
TEST RESULTS

Test	Input Voltage $E/\sqrt{2}$ (rms)	Output Voltage U	Output Power P_o	Measured Efficiency η_{overall}
1	90 V	174.4 V	100 W	93.8 %
2	90 V	382.6 V	100 W	87.3 %
3	230 V	380.2 V	100 W	94.5 %

Figure 8 is the blow-up waveforms of V_i and I_i, and no crossover distortion has been observed even when a noticeable phase lead of the input current due to the input filter is present at 230 V, 400 Hz input.

Figures 9 and 10 show the operating duty cycle at different values (0 V and 300 V) of V_i. The calculated (using (3)) and the measured duty cycles are in perfect agreement. At $V_i = 0$ the calculated and measured duty cycle are 0.5 and 0.499 while at $V_i = 300$ V the calculated and measured duty cycle are 0.105 and 0.119, respectively.
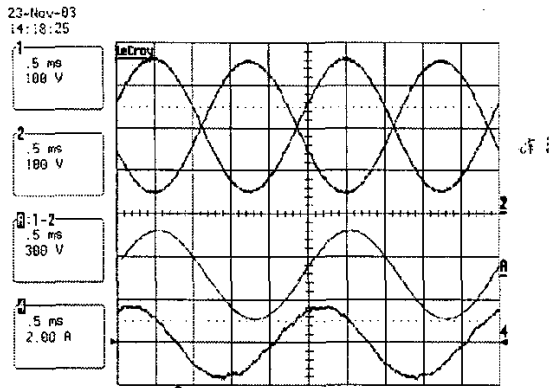
23-Nov-03
14:18:25

.5 ms
100 V

.5 ms
100 V

1-2
.5 ms
300 V

.5 ms
2.00 A

LeCroy

Fig. 7. Waveforms of V_1 (Ch1), $\xi(t)$ (Ch2), V_i (ChA) and I_i (Ch4), for input voltage 90 V (rms) and line frequency 50 Hz.

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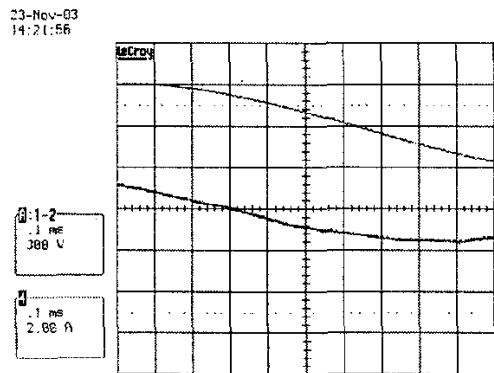14:21:56

1-2
.1 ms
300 V

.1 ms
2.00 A

LeCroy

Fig. 8. Waveforms of V_i (ChA) and I_i (Ch4), for input voltage 230 V (rms) and line frequency 400 Hz.

23-Nov-03
14:24:34

1-2
5 µs
300 V

5 µs
20.0 V

LeCroy

duty(3) ΠΠ   49.91 %

Fig. 9. Waveforms of V_i (ChA) and $D(t)$ (Ch3) at zero crossing point.

23-Nov-03
14:28:51

1-2
5 µs
300 V

5 µs
20.0 V

LeCroy

duty(3) ΠΠ   11.93 %

Fig. 10. Waveforms of V_i (ChA) and $D(t)$ (Ch3) at input voltage 300 V (rms).

IV. CONCLUSION

An input rectifierless PFC converter with low input current distortion has been proposed and verified experimentally. It eradicates the crossover distortion due to the input rectifier and the phase lead of input current introduced by the filter and control circuits in conventional PFC converters, which is a significant problem at high mains frequencies. No distortion due to mode changing has been found since the converter allows bi-directional energy flow and all inductors work at continuous conduction mode at all times. A control circuit has been designed to reduce the circulation power and provide higher conversion efficiency. This makes the proposed PFC converter suitable for airborne power systems requiring low input current harmonics with a relatively high mains frequency. Possible future work way proceed along the idea of rectifier-less configurations [7] as well as other practical design tradeoff considerations [8].
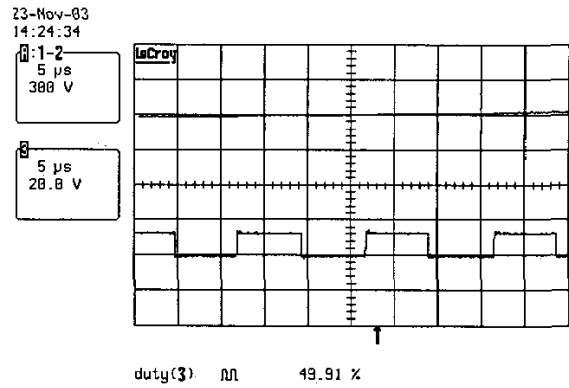
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