A Single Phase Voltage Regulator Module (VRM) With Stepping Inductance for Fast Transient Response

Dylan Dah-Chuan Lu, *Member, IEEE*, Joe C. P. Liu, *Member, IEEE*, Franki N. K. Poon, *Member, IEEE*, and Bryan Man Hay Pong, *Senior Member, IEEE*

***Abstract*—A single-phase fast transient converter topology with stepping inductance is proposed. The stepping inductance method is implemented by replacing the conventional inductor in a buck converter by two inductors connecting in series. One has large inductance and the other has small inductance. The inductor with small inductance will take over the output inductor during transient load change and speed up dynamic response. In steady state, the large inductance takes over and keeps a substantially small ripple current and minimizes root mean square loss. It is a low cost method applicable to converters with an output inductor. A hardware prototype of a 1.5-V dc–dc buck converter put under a 100-A transient load change has been experimented upon to demonstrate the merit of this approach. It also serves as a voltage regulator module and powers up a modern PC computer system.**

***Index Terms*—Buck converter, fast transient, voltage regulator (VR).**

I. Introduction

FAST transient response is a crucial issue in dc–dc converters for modern microprocessors. The load current may change between full load and nearly no load conditions within nano-seconds range. This fast load change demands the output terminal of the power supply to deliver full loading current within nano-seconds time range. Although a decoupling capacitor helps reduce the effect of the high current transient, the associated voltage regulator module (VRM) is still required to have a high slew rate of 150 A/μs or more.

The barrier of output current slew rate is determined by the equivalent output inductance of the buck regulator. Reducing output inductance is a way to satisfy the requirement. However, small inductance will produce side effects such as high ripple current. Switching converter engineers are facing a new design challenge to provide high output current slew rate and maintain low ripple current, low ripple voltage, and high efficiency at the same time.

A small output inductance of a single converter may increase the output current slew rate, but this will also produce higher ripple voltage and ripple current which is not acceptable. Nevertheless, it is possible to reduce high ripple current by putting several converters in parallel and each converter has a relatively large output inductance.

An interleaving parallel converter [1]–[9] is one special form of parallel converter configuration which produces small equivalent output inductance. An interleaved converter is generally accepted as a solution to provide fast transient response while keeping the output inductors from being too small. However, there are unresolved issues with the interleaved converter. It gives good performance during the transient state, but the steady state performance is still not satisfactory due to higher conduction losses induced by peak currents in each phase. In addition to the many inductors in the multiple phases, the component count of associated circuits such as gate drivers and current sensing networks also multiplies with the number of phases put in parallel. Current sharing among the multiple phases of an interleaved parallel converter is also a challenging issue [7]–[9]. Moreover, in order to produce wide bandwidth response to meet stringent requirement these days, high switching frequency is mandatory. Consequently, switching losses will also be increased.

Prior work [10], [11] showed a method of using a paralleled linear regulator to "clamp" the output voltage within a certain limit. It gives very good performance in the steady state but it is theoretically dissipative during the transient condition, although the loss can be small.

A single-phase fast transient converter using stepping inductance is proposed in this paper [12]–[14]. It is theoretically lossless, and is able to produce a high output current slew rate at the transient state and low ripple at steady state. It is an alternate solution to a multiphase power converter at low cost and it is easy to implement. The objective of this paper is to demonstrate this single-phase converter and the capability to switch between different inductance values for transient and steady states. This paper also shows this single-phase converter can be designed to meet tight VRM requirements such as the Intel VRD10.1.

II. Theory

This section shows the basic configuration of the stepping inductance converter. The stepping inductance method can be implemented on any converter topology with an output inductor–capacitor LC filter as shown in Fig. 1(a). Fig. 1(a) shows the basic configuration of the stepping inductance converter. The output series inductors L_o, L_r, and output capacitor C_o form the output filter of a basic dc–dc converter. Inductor L_r is chosen to be much smaller than L_o. Inductor $L_{\rm aux}$ is magnetically coupled with L_o. $L_{\rm aux}$, V_1, V_2, S_1 and

Manuscript received August 26, 2005; revised June 5, 2006. This paper was presented in part at APEC'01, March, 2001. Recommended for publication by Associate Editor P. K. Jain.

D. D.-C. Lu is with the School of Electrical and Information Engineering, The University of Sydney, Sydney NSW 2006, Australia (e-mail: dylan.lu@ee.usyd.edu.au).

J. C. P. Liu and F. N. K. Poon are with PowereLab Limited, The University of Hong Kong, Hong Kong.

B. M. H. Pong is with the Power Electronics Laboratory, Department of Electrical and Electronic Engineering, The University of Hong Kong, Hong Kong.

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Digital Object Identifier 10.1109/TPEL.2006.889909

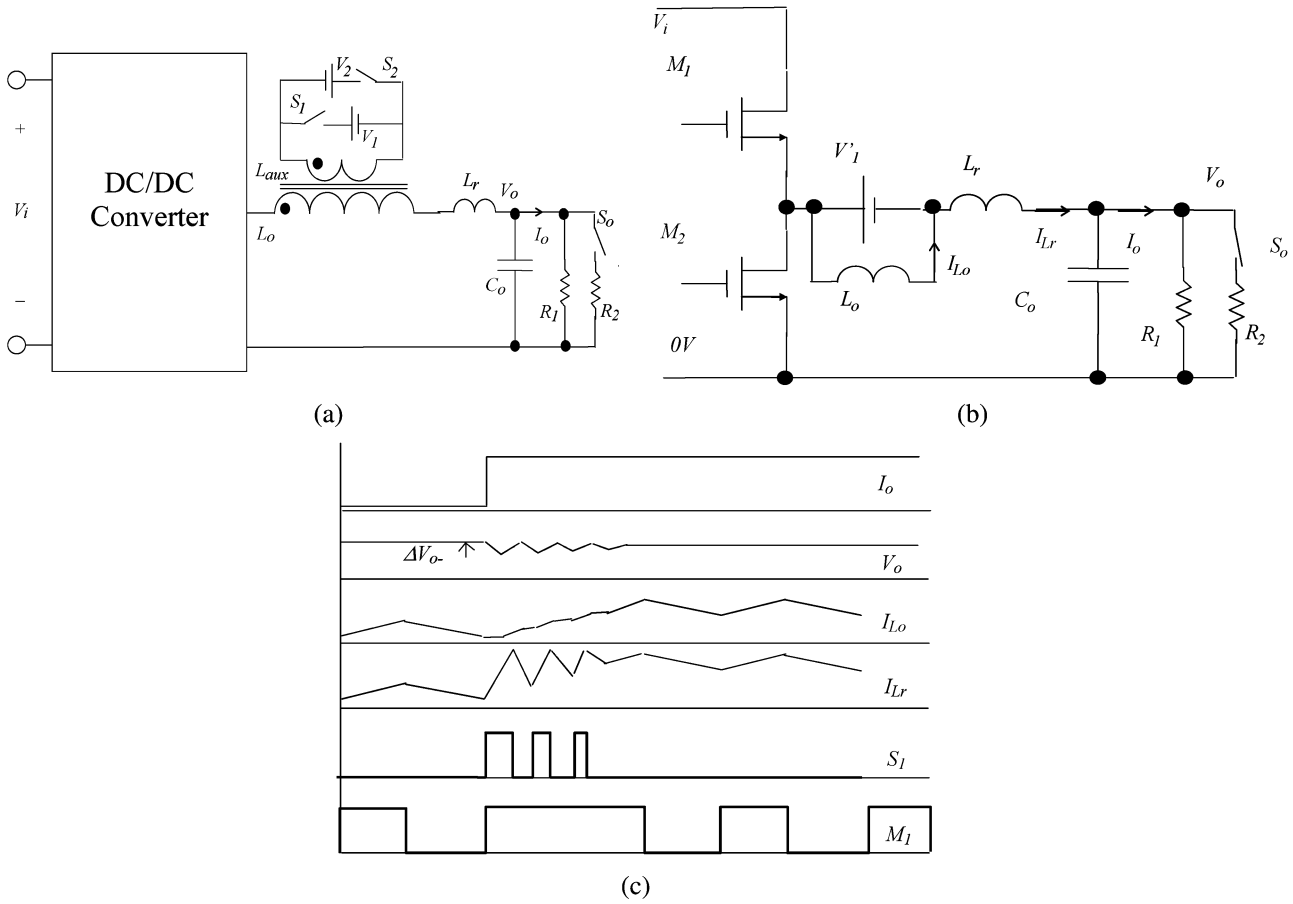


Fig. 1. Stepping inductance converter: (a) basic configuration; (b) equivalent circuit on a buck converter during transient; and (c) simplified operation waveforms.

S_2 together form an auxiliary circuit to "short circuit" the large value inductor L_o during load transient. S_1 is programmed to turn on during a fast and large increase in load current. S_2 is programmed to turn on during a fast and large decrease in load current. The number of turns of $L_{\rm aux}$ is chosen to reduce the reflected current flow through S_1, S_2 in order to reduce their conduction losses.

Here, only positive change of current is described. Fig. 1(b) shows the equivalent circuit when S_1 is turned on when there is a step and large increase in load current. Once S_1 is turned on, the equivalent total output inductance will change from $L_o + L_r$ to a much smaller L_r. This increases output inductor current slew rate in the period where the transient occurred. This also reduces voltage deviation due to large step change in load current.

Fig. 1(c) shows the operation of the fast transient converter by various waveforms. When the load current I_o increases in a step, the output voltage starts to drop accordingly. The auxiliary switch S_1, with a series voltage source V_1, is programmed to turn on in order to provide a step reduction of the equivalent output inductance. The equivalent output inductance will change to a much smaller value L_r, and provides output inductor current I_{Lr} with high slew rate. Once the fast output inductor current reaches the level of the output load current, the drop of the output voltage V_o will stop and start to rise, as the output inductor current is higher than the load current and flows into C_o. Auxiliary switch S_1 can be programmed to turn off when the voltage V_o rises back to a certain level.

During the load transient there is a short period in which S_1 switches on and off when the output voltage stabilizes. As L_o is much greater than L_r, the equivalent output inductor current will be dominated by I_{Lo} after S_1 is turn off. Although the magnitude of I_{Lo} is increased during the period when S_1 is turn on, it is not high enough to reach the level of load current I_o, hence V_o will drop again after S_1 is turned off. Nevertheless, S_1 can be programmed to turn on again when the output voltage drops below a certain level. These on and off states will repeat until the magnetizing current I_{Lo} reaches a level equal to the load current. M_1 is expected to keep turning on between that on and off state of S_1 in order to make I_{Lo} equal to I_o as soon as possible and produce minimum transition time for the converter to go back to steady operation as quickly as possible.

The main purpose of the voltage source V_1 is to produce minimum transition time. It keeps the output inductor L_o current increasing when S_1 and M_1 are turned on. V_1 can be chosen from 0 V to a certain value such that the reflected voltage across L_o will not cause reverse current to flow through M_1 when S_1 is on.

When the output current decreases in a fast a large step the operations are comparative to the mechanisms so described. At that time S_2 will turn on correspondingly and provide a high negative slew rate current to avoid voltage build up at C_o. A transition period will be created in which S_2 will turn on and turn off until the current flowing in inductor L_o reduces to the steady state load current.

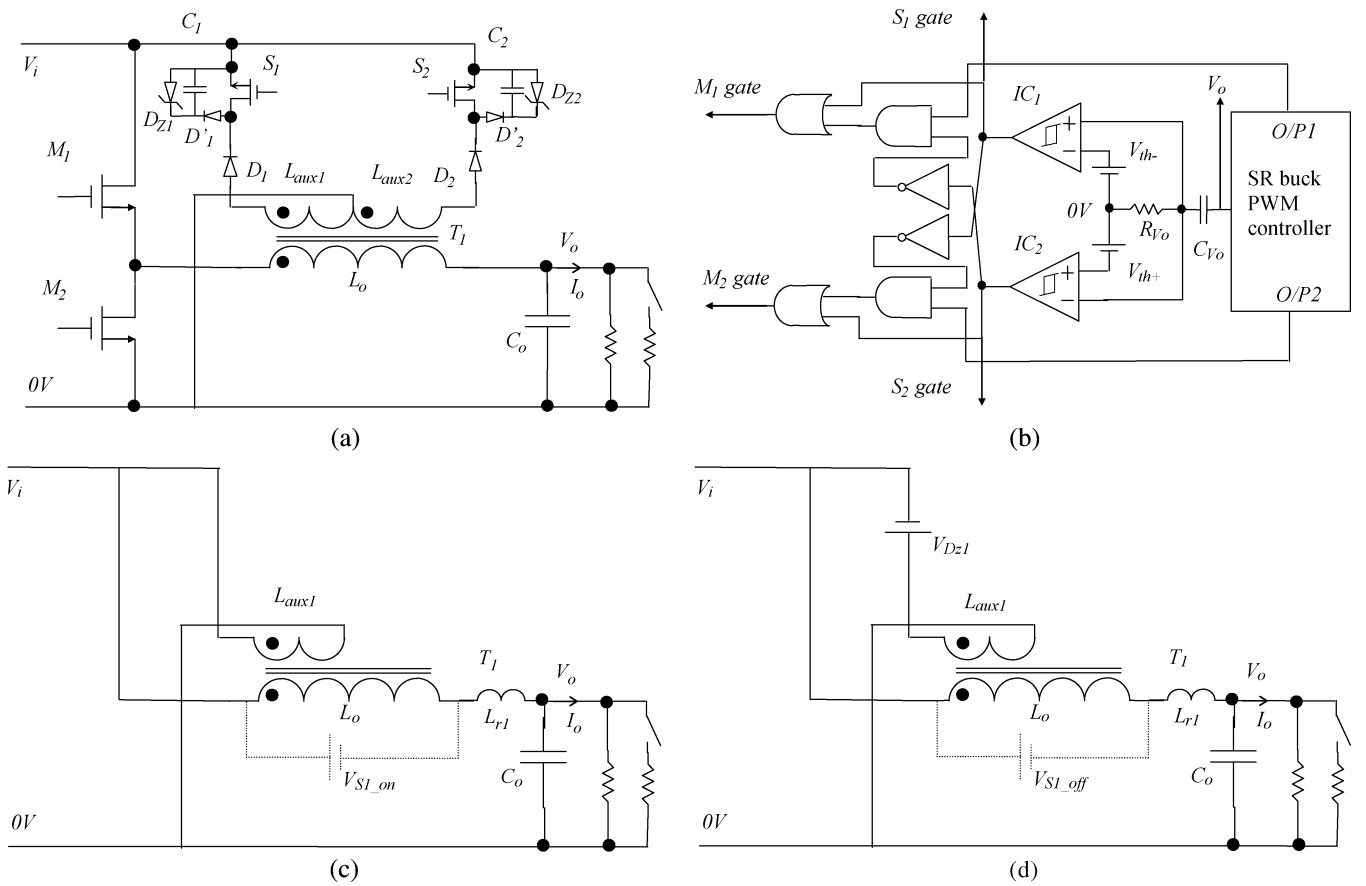


Fig. 2. Simplified practical implemental: (a) simplified circuit of stepping inductance converter; (b) hysteresis control and PWM circuit; (c) equivalent circuit when both S_1 and M_1 is turned on, and (d) equivalent circuit when S_1 is turned off and M_1 is turned on.

III. Control

The proposed solution consists of a conventional buck converter with a time-varying inductance. In the steady state, the stepping inductance circuit ceases operation and the output inductor keeps both itself and a large inductance to keep the current ripple small. A linear and compensated voltage mode control suffices to regulate the output voltage. In the transient load change, where a fast response of output is needed, the stepping inductance circuit works to "short-circuit" the output inductor, and the slew rate will be increased and limited by the leakage inductance. A hysteresis controller takes control of the stepping inductance circuit and overrides the signal from the slower linear controller. This control ensures the output voltage is bounded by the preset tolerance bands or hysteresis window, as shown in Fig. 3. The linear controller resumes until the output voltage falls within the hysteresis window. Although the transition of controls will cause some output oscillation, it is bounded by the hysteresis window to ensure output regulation.

IV. Implementation

Practical circuit implement is simple. Voltage source V_1 or V_2 can be realized by making use of the input voltage, although output voltage is also possible. Switches S_1, S_2 can be realized by a small MOSFET, the small inductance L_r can be the leakage inductance between winding L_o, $L_{\rm aux1}$, and $L_{\rm aux2}$. Proper timing of S_1 and S_2 can be realized by hysteresis control according to the change of output voltage V_o.

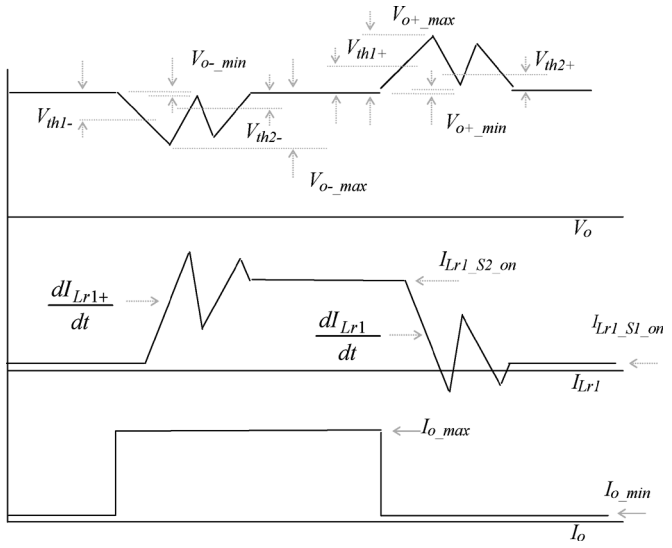


Fig. 3. Definition and exaggerated and microscopic view between the relation of output voltage, inductor current, and loading current.

Fig. 2(a) shows a practical implementation of the stepping inductance converter concept. Two separated windings or inductors $L_{\rm aux1}$, $L_{\rm aux2}$ are magnetically coupled to L_o and form a transformer T_1. S_1, S_2 are responsive to positive or negative change of load current.

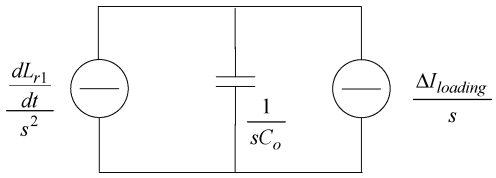


Fig. 4. Equivalent model during transient loading condition and S_1 or S_2 turned on.

Diodes D_1, D_2 prevent reverse current flow. D_1', D_2', C_1, C_2, D_{z1}, and D_{z2} form a snubber circuit to absorb current reflected from leakage inductance L_{r1} when S_1 or S_2 is turned off. It is understood that other kinds of snubber or nondissipated snubbers may also be used in this application.

Fig. 2(b) shows a realization of the control circuit. The SR buck pulsewidth modulation (PWM) controller can be any typical dual output PWM controller such as a Sync–Rect buck converter. Two hysteresis comparators, I_{C1} and I_{C2}, are responsible for detecting the negative or positive change of output voltage. A logic circuit ensures no simultaneous conduction of M_1 and M_2, and no simultaneous turn on of switches S_1 and M_2 or S_2 and M_1.

Fig. 2(c) shows a simplified equivalent circuit when S_1 and M_1 are turned on. S_1 is turned on if the output voltage drops below a predetermined level V_{th1-}. M_1 will be turned on too as the buck PWM controller detects a voltage drop at output voltage V_o. After S_1 is turned on, the magnetizing inductor L_o is shorted out by an equivalent voltage source V_{S1_on}. It has a value determined by the input voltage and turns ratio of L_o and $L_{\rm aux1}$. Hence, the voltage across the equivalent leakage inductor L_{r1} is equal to V_i minus V_o and V_{S1_on}. This value is designed to be substantially large so that there is enough voltage across the small leakage inductor L_{r1} to generate current with a high slew rate and pump current to the output fast enough to counteract the output voltage drop. In practice, the overall equivalent inductance L_{r1} can be as small as the parasitic inductance of T_1 and the printed circuit board (PCB) trace. Hence, it is possible to tackle fast load transients (especially those in microprocessor application).

Fig. 2(d) shows the simplified equivalent circuit when S_1 is turned off and M_1 is still turned on. S_1 is turned off if the change of output voltage has risen back to a predetermined level V_{th2-}. V_{th2-} is the trigger level of a hysteresis comparator which monitors the output voltage drop. The current I_{Lr1} flowing in leakage inductor will be reflected to $L_{\rm aux1}$ and reset by the voltage source V_{Dz1} formed by snubber as described above. It is possible to use a lossless snubber to further reduce the losses in this reset mechanism.

S_1 will be kept turning on and off until the magnetizing current flowing in L_o rises up to the level of the load current.

V. Design Parameters

Fig. 3 shows a microscopic and exaggerated view during a load transient condition. Figs. 2(c),(d) and 3 explain the transient. Here, we assume a) the change of output voltage is comparably small with the output voltage and b) the output current has a very large step change which is much larger than the ripple

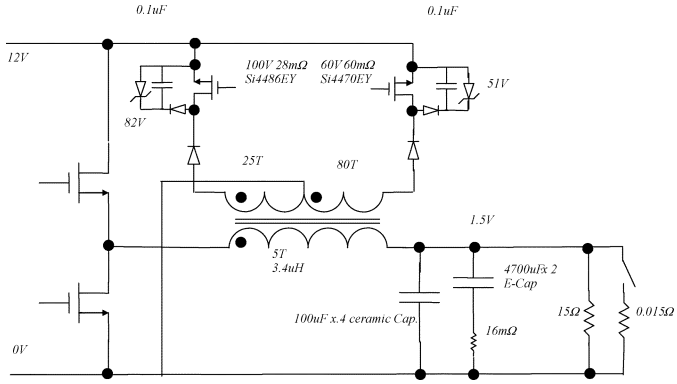


Fig. 5. Simplified experimental circuit.

current flowing in L_{r1}. S_1 or S_2 will turn on when the output voltage drops or rises through the first threshold voltage V_{th1-} or V_{th1+}, according to cases with a step increase or decrease in load current (see Figs. 4 and 5).

Positive output current slew rate dI_{Lr1+}/dt of L_{r1} depends on voltage across L_{r1} and as

$$\frac{dI_{Lr1+}}{dt} = \frac{V_i - \left(V_o + V_i \frac{N_{Lo}}{N_{\rm Laux1}}\right)}{L_{r1}}. \tag{1}$$

Similarly, negative output current slew rate dI_{Lr1-}/dt is

$$\frac{dI_{Lr1-}}{dt} = \frac{-\left(V_o - V_i \frac{N_{Lo}}{N_{\rm Laux2}}\right)}{L_{r1}} \tag{2}$$

where N_{Lo} = number of turn of L_o, $N_{\rm Laux1}$ = number of turn of $L_{\rm aux1}$.

The behavior of the output voltage transient can be analyzed according to the following mode by assuming a step change of loading current. In order to find out the voltage change across C_o, the turning point at which maximum deviated output voltage $\Delta V_{o-\_\max}$, $\Delta V_{o+\_\max}$ is produced has to be found out. The peaks can be found out by setting its differentiation equal to zero. Physically, when current I_{Lr1} flowing in L_{r1} catches up with load current $I_{o\_\max}$, or when $I_{Lr1} = I_{o\_\max}$, the output voltage stop dropping and start to rise again. The following equation shows the maximum output voltage drop $\Delta V_{o-\_\max}$ can be worked out by simple circuit analysis

$$\Delta V_{o-\_\max} = V_{th1-} + \frac{(I_{o\_\max} - I_{Lr1\_S1\_on})^2}{2C_o \frac{di_{Lr1+}}{dt}}. \tag{3}$$

Similarly the maximum voltage rise $\Delta V_{o+\_\max}$ during transient is

$$\Delta V_{o+\_\max} = V_{th1+} + \frac{(I_{o\_\min} - I_{Lr1\_S2\_on})^2}{-2C_o \frac{di_{Lr1-}}{dt}}. \tag{4}$$

The inductor current will continue to increase or decrease until the changing output voltage hits a second threshold voltage V_{th2-} or V_{th2+}. Beyond this second turning point the output voltage is in change in the opposite manner. The negative minimum deviated voltage $V_{o-\_\min}$ against V_o can be also found out by considering the voltage induced on C_o caused by the peak

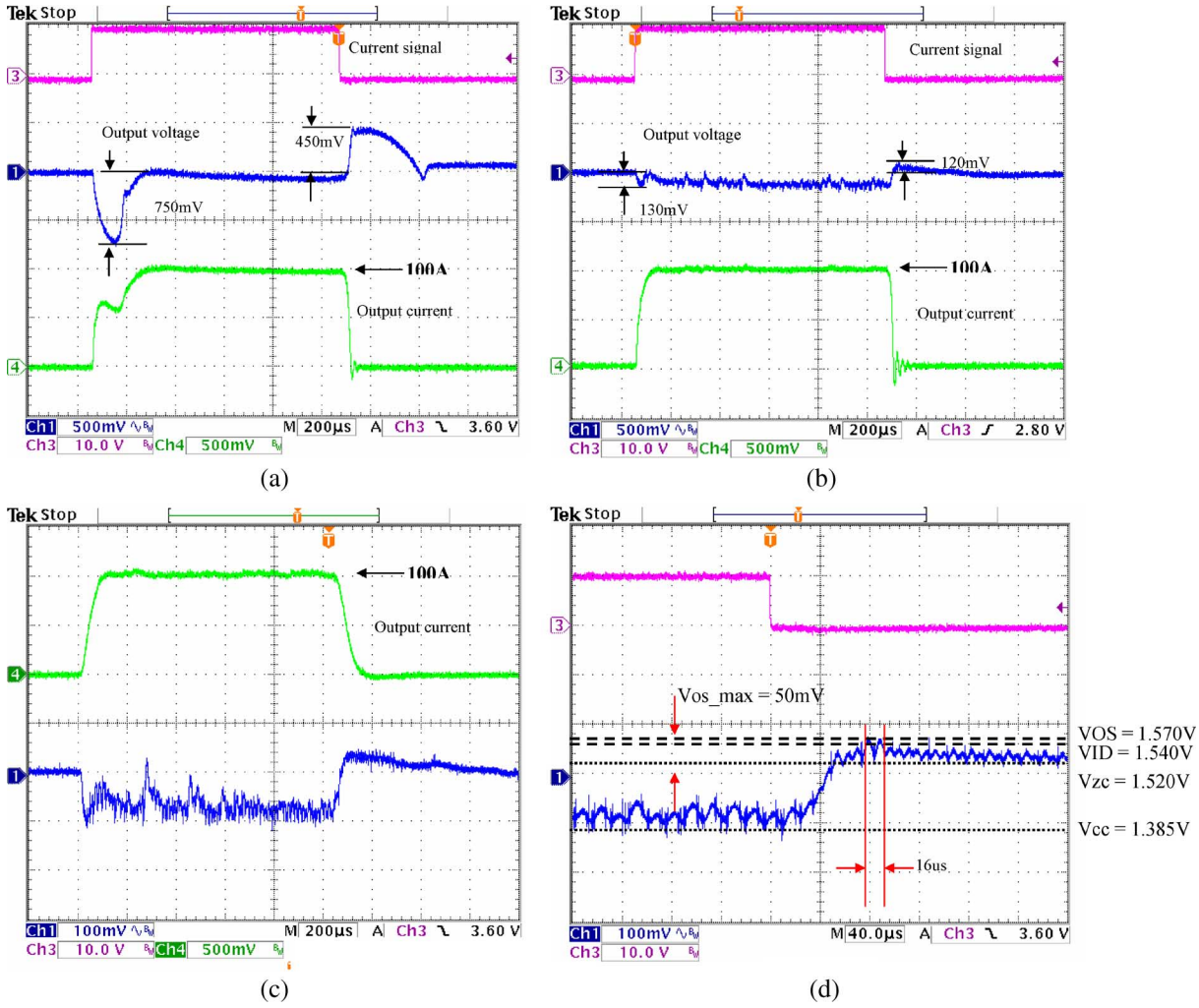


Fig. 6. Experimental result of output voltage variation, CH1—output voltage at 500 mV/Div, CH3—load current signal; CH4—load current at 100 A/Div: (a) without stepping inductance and (b) with stepping inductance; (c) with stepping inductance and extra capacitors at output; and (d) magnified view of voltage overshoot complying VRD10.1 requirement.

excessive inductor current I_{Lr1} dropping back to output current level, that is

$$\Delta V_{o-\_\min} = V_{th2-} - \frac{3\left[(I_{o\_\max} - I_{Lr1\_S1\_\mathrm{on}})^2 + 2C_o\frac{dL_{r1+}}{dt}(V_{th1-} - V_{th2-})\right]}{2C_o\frac{\left[V_o + (V_i + V_{Dz1})\frac{N_{Lo}}{N_{\mathrm{Laux1}}}\right] + V_i}{L_{r1}}}. \quad (5)$$

Similarly, positive minimum deviated voltage $V_{o+\_\min}$ again V_o is

$$\Delta V_{o+\_\min} = V_{th2+} - \frac{3\left[(I_{o\_\max} - I_{Lr1\_S2\_\mathrm{on}})^2 + 2C_o\frac{dL_{r1-}}{dt}(V_{th1+} - V_{th2+})\right]}{2C_o\frac{\left[(V_i + V_{Dz1})\frac{N_{Lo}}{N_{\mathrm{Laux2}}} - V_o\right]}{L_{r1}}}. \quad (6)$$

An important criteria is needed to avoid self-oscillation of the hysteresis control mechanism. One must avoid having the minimum deviated voltage $V_{o-\_\min}$ or $V_{o+\_\min}$ to cross over the output voltage level and touch the opposite threshold. The following criteria should be met:

$$V_{th1+} + V_{o-\_\min} > 0 \text{ and } V_{th1-} + V_{o+\_\min} > 0. \quad (7)$$

VI. Experimental Results

A 12-V input and output at 1.5-V/100-A buck converter is built. Loading current is switched between $I_{o\_\max} = 100$ A and $I_{o\_\min} = 0.1$ A at a frequency of 100 Hz.

The following figures show the setup and values. Output inductor $L_o = 3.4$ μuH, $N_{Lo} = 5$ T, with very small output ceramic capacitor of $C_o = 100$ μF×8 and switching frequency $f_s = 200$ kHz. Auxiliary winding $N_{\mathrm{aux1}} = 25$ T, $N_{\mathrm{aux2}} = 80$ T are chosen 5 to 16 times of N_{Lo} to reduce the losses of auxiliary MOSFETs S_1 and S_2. S_1, S_2 are Si4486EY 100-V 28-mΩ and Si4470EY 60-V 60-mΩ small MOSFETs, respectively. $D_1 = D_2 = D_1' = D_2' = 10$ MQ 100 N. Leakage inductance is measured as $L_{r1} = 40$ nH, which includes trace inductance. $D_{z1} = 82$-V 1/2-W zener, $D_{z2} = 51$-V 1/2-W zener. $C_1 = C_2 = 0.1$ μF. $V_{th+} = 350$ mV and $V_{th-} = 150$ mV.

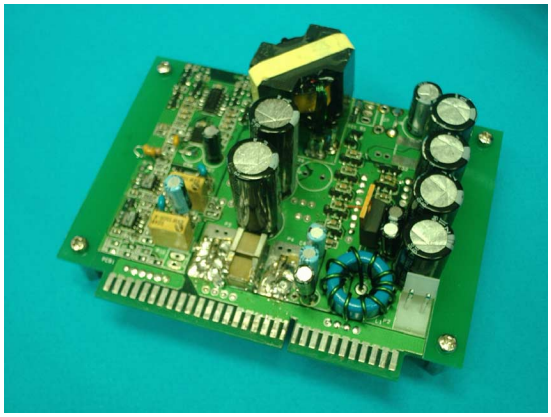


Fig. 7. Stepping inductance evaluation prototype photograph.

Fig. 6 shows the experimental results of output voltage variation, CH1—output voltage at 500 mV/Div, CH3—load current signal, CH4—load current at 50 A/Div: a) without stepping inductance and b) with stepping inductance. It can be seen that the proposed stepping inductance method reduced the output voltage ripple by six times and three times at undershoot and overshoot conditions, respectively.

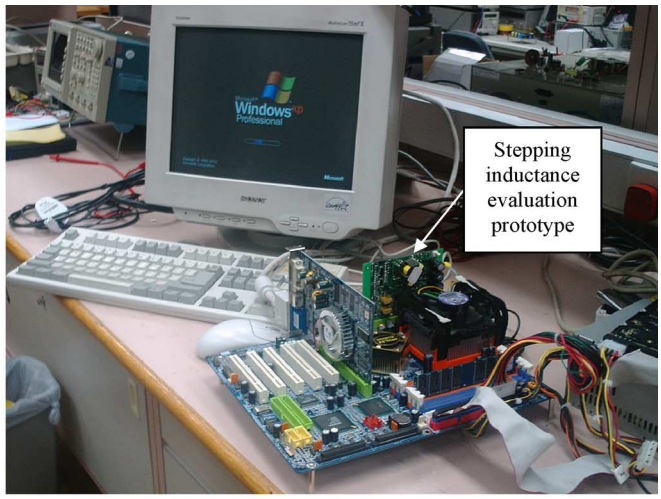
In an attempt to comply with the VRD 10.1 requirement by Intel, extra capacitors (Os-Con 2200 μF $\times$ 6) have been added to the load. Fig. 6(c) shows the output voltage when the load current changes from 0.1 to 100 A. The voltage overshoot as shown in Fig. 6(d), meets the 50-mV overshoot and 25-μs overshoot duration as required by the VRD Design Guide [16]. Fig. 7 shows the photograph of the stepping inductance evaluation hardware prototype. Comparing the four-phase interleaved method in [18], which uses 3-mF capacitance to tackle 50-A step load change, to the proposed solution using 1.4 mF to tackle 100-A step load change. The proposed solution saves 1.6-mF capacitance and offers twice the performance.

The voltage deviations are calculated according to the equations so derived, assuming the ripple current of the output inductor is relatively small as compared to the loading current step change. Hence, an approximation can be made

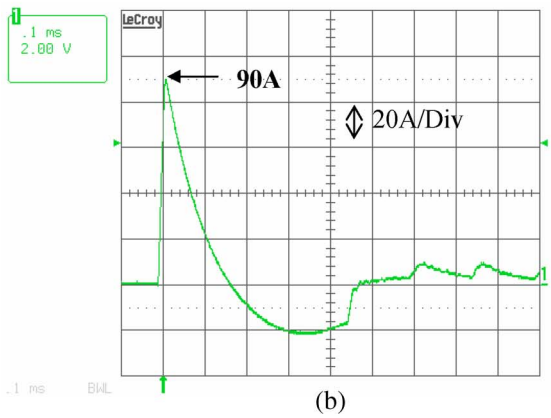
$$I_{Lr1\_S1\_\mathrm{on}} = I_{o\_\min} \text{ and } I_{Lr1\_S2\_\mathrm{on}} = I_{o\_\max}.$$

The maximum voltage change $\Delta V_{o-\_\max}$ and $\Delta V_{o+\_\max}$ with 100-A loading change is calculated as $\Delta V_{o-\_\max} =$ 133 mV and $\Delta V_{o+\_\max} =$ 147 mV. The experiment result shows the real situation is better than the calculated result. The reason that the auxiliary switch S_1 and S_2 actually turn on before the deviated output voltage hit the first threshold voltage V_{th1-} or V_{th1+}. It is caused by noise spikes induced from the very high slew rate of load current.

An immediate application of the stepping inductance converter is to serve as a VRM for modern PC environment with fast CPU speed. The evaluation prototype has been used to power a PC, as shown in Fig. 8(a), with the following configuration: Intel P4 3.2-GHz CPU (Extreme edition), 512-MB DDR-RAM, Gigabyte 8KNXP-Ultra Motherboard, Asus V3005 Display Card, and Window XP Professional Edition operating system. Note that the on-board three-phase buck converters have been



(a)



(b)

Fig. 8. (a) VRM application for modern PC environment with fast CPU (Intel P4 3.2 GHz) and (b) startup current of converter output.

removed and the power source is solely provided by the stepping inductance prototype. According to the requirement of VRD 10.1 [16], it is possible to have a dynamic current step as much as 95 A. This can be seen, as shown in Fig. 8(b), during the startup process of the power supply when the power switch is closed.

Since the conduction losses in auxiliary switch S_1 and S_2 are greatly reduced by the turns ratio of N_{Lo}, N_{Laux1} and N_{Laux2}, the temperature rise of the MOSFETS S_1 and S_2 and snubber zener diodes D_{z1}, and D_{z2} are small. A detailed loss analysis has been presented in [15], showing the auxiliary circuit causes negligible losses compared to the overall power loss. And the comparison of proposed stepping inductance converter to other VRM topologies such asmultiphase VRM in terms of size, ripple reduction, and efficiency has been reported in [17]. In simple words, the stepping inductance converter offers better fast transient response than three-phase VRM and compatible steady state ripple current and efficiency without expanding the number of phases of voltage modules.

A transient fast change in input current will be produced by the fast output current due to a fast load transient. This is true for all fast transient converters. An input filter is needed to slow down the input current during load transient condition. Such input filter can also provide filtering effect for steady state operation.

VII. Conclusion

A stepping inductor method for converters with an output inductor is presented. The stepping inductance converter is very suitable for fast transient VRM application. It can be applied to a conventional buck converter to greatly improve transient response with only two additional small MOSFETs and diodes. It is also theoretically lossless.

The control circuit is also easy to implement and can be integrated with a generic buck PWM controller integrated circuit. Extra cost and design effort for such an improvement is minimal, as only a low cost small size component or logic circuit are needed.

Steady-state performance of the proposed solution is equivalent to today's sophisticated SR buck converter, and has, practically, very little power loss due to transient operation.

For a multiphase buck converter, the number of phases will be increased as the current demand increases due to the increasing CPU speed. Consequently, the number of buck controllers and sensing devices, and hence the cost, will be increased. But the proposed solution employs only a single-phase buck converter to produce steady-state current and with a stepping inductance circuit to tackle transient load change. It is expected that the size and cost is much lower.

It has been shown that such an approach is very suitable for fast transient response VR used on a microprocessor and other fast loading change applications.

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Dylan Dah-Chuan Lu (S'00–M'04) received the B.Eng. (with honors) and Ph.D. degrees in electronic and information engineering from The Hong Kong Polytechnic University, Hong Kong, in 1999 and 2004, respectively.

He was a Research Assistant with the Electronic and Information Engineering Department, Hong Kong Polytechnic University, from 1999 to 2000. From 2002 to 2003, he was a Research Student Trainee with Newton Power Limited. In 2003, he joined PowereLab Limited (a spin-off company at The University of Hong Kong) as a Senior Engineer. His major responsibilities include project development and management, circuit design, and contribution of research in the area of power electronics. Currently, he is a Lecturer in the School of Electrical and Information Engineering, The University of Sydney, Australia. He has published a number of international conference and journal papers on the analysis and design of power electronics circuits. He holds one U.S. patent. His interests are in the areas of computer-aided design of power converters, dc–dc converter for VRM application, electronic ballast, controls, power-factor-correction circuits, and soft-switching techniques.

Joe C. P. Liu (M'99) was born in Hong Kong. He received the B.S. degree in electrical and electronic engineering from the University of Hong Kong, Hong Kong, in 1993.

After graduation, he joined ASTEC Custom Power, Hong Kong, as an Electronic Engineer, and in 1996 joined Artesyn Technologies (Asia Pacific), Ltd., as a Senior Research Engineer. He is now working with the Power Electronics Laboratory, The University of Hong Kong. His research interest includes high-efficiency synchronous rectification, zero-voltage switching, and converter topologies.

Franki N. K. Poon (M'95) received the B.Eng. degree (with honors) in electronic engineering from the City University of Hong Kong, Hong Kong, in 1995, and the Ph.D. degree from Hong Kong Polytechnic University, in 2003.

After graduation, he worked with Artesyn Technologies (Asia Pacific) Limited for three and a half years before joining the Power Electronics Laboratory, University of Hong Kong. He is now working in a spin off company, PowerELab, Ltd., University of Hong Kong. He has more than 20 patents. His current interest includes soft switching techniques, EMI modeling, PFC topologies, synchronous rectification, converter modeling, PWM inverters, simulation technique, and fast transient regulators.

Bryan Man Hay Pong (M'84–SM'96) was born in Hong Kong. He received the B.Sc. degree in electronic and electrical engineering from the University of Birmingham, Birmingham, U.K., in 1983 and the Ph.D. degree in power electronics from Cambridge University, Cambridge, U.K., in 1987.

After graduation he was a Senior Design Engineer and then a Chief Design Engineer with National Semiconductor Hong Kong where he was involved in electronic product design. Afterwards, he joined ASTEC International where he was a Principal Engineer and then a Division Engineering Manager. He is now an Associate Professor at the University of Hong Kong, Hong Kong. He is in charge of the Power Electronics Laboratory and leads a team to carry out research in switching power supplies. He has co-invented a number of patents. His research interests include synchronous rectification, EMI issues, power factor correction, magnetic component design, soft switching and digital control of power converters.