Design of Hybrid Continuous-Time Discrete-Time Delta-Sigma Modulators

Hing-Kit Kwan, Siu-Hong Lui, Chi-Un Lei, Yansong Liu, Ngai Wong, and Ka-Leung Ho

Department of Electrical and Electronic Engineering,
The University of Hong Kong
Pokfulam Road, Hong Kong
{kwanhk, luip, culei, ysliu, nwong, klho}@eee.hku.hk

***Abstract*—Recent attention has been drawn to the hybrid Delta-Sigma (ΔΣ) structure featuring the integration of continuous-time (CT) and discrete-time (DT) structures in the loop filter. It combines the accurate loop filter characteristic of a DT ΔΣ modulator and the inherent anti-aliasing of a CT ΔΣ modulator. We present a design methodology for building a CT-DT ΔΣ modulator via the transformation from a DT ΔΣ modulator prototype. We also demonstrate the tradeoff of applying this structure to cascaded Delta-Sigma modulators compared to pure CT or DT implementations.**

***Index Terms*—Sigma-Delta modulation, oversampling, ADC, design methodology**

I. Introduction

Recent attention has been drawn to the hybrid ΔΣ structure featuring the integration of initial stage(s) of continuous-time (CT) integrator(s) and subsequent discrete-time (DT) integrators in the loop filter [1], [2], e.g., Fig. 1. Such mixed-mode ΔΣ modulator has several merits over conventional ΔΣ modulators using only DT loop filters [1]:

1) The initial CT integrator(s) can provide inherent anti-aliasing filtering to the input signal. Hence, the anti-aliasing filter preceding the modulator can be removed or the requirement to the anti-aliasing filter is relaxed to reduce the complexity and power consumption.

2) Since there is no sampling of the input voltage prior to the loop filter, signal-dependent charge injection, clock feed-through and sampled noise do not exist in the first stage. The sampling takes place within the loop filter where these noises are shaped and suppressed.

3) Any signal-dependent glitches coupled to the input of the modulator are averaged out over the clock period by the CT integrator, thereby harmonic distortions due to the coupling are attenuated.

4) When there is no feedforward path from input to the second and subsequent stages, the input impedance of the first-stage integrator is purely resistive, and no electromagnetic interference (EMI) is emitted back to the input pins.

Meanwhile, a single-loop CT-DT ΔΣ modulator still possesses most of the advantages of a switched-capacitor (SC) single-loop DT ΔΣ modulator, such as accurate and robust loop filter characteristics against process variations, and insensitivity to clock jitter etc., as the subsequent integrators (in majority) are still constructed by DT SC circuitry. The timing control loop in [1] has significantly increased the insensitivity of the CT stage integrators against modulator clock jitter, and hence has considerably reduced this dominant error source [3] affecting the initial CT stages of a CT-DT ΔΣ modulator [4]. This also removes the need of other means to increase the clock jitter immunity of the CT stages, which in turn greatly simplifies the design while maintaining a high signal-to-noise ratio (SNR).

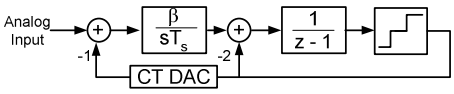

Fig. 1. An example CT-DT ΔΣ modulator.

Despite the potential advantages of a CT-DT ΔΣ modulator over its purely DT counterpart, little has been reported for the proper modeling and design of the former. Subsequently, we propose an analytical framework to systematically design a CT-DT ΔΣ modulator with an arbitrary number of initial CT integrator stages based on the transformation from a DT ΔΣ modulator prototype. Our main innovation and contribution lie in the matching of a DT ΔΣ modulator to a CT-DT ΔΣ structure for actual realization. In particular, it will be shown that the proposed design flow produces a step-invariant CT-DT ΔΣ modulator as compared with the DT ΔΣ modulator prototype. Extension to other waveform-invariant designs follows similarly. In the final part of this paper, the application of this DT-CT structure on the cascaded ΔΣ topology is proposed and investigated. It is shown that the DT-CT implementation of cascaded ΔΣ modulator can provide the same level of anti-aliasing as a CT cascaded modulator, which has also attracted much attention in recent work [5], [6], [7].

II. Continuous-Time Integrator and Inherent Anti-aliasing

We begin by analyzing the DT model of a CT integrator at the input of a CT-DT ΔΣ modulator. Referring to the upper half of Fig. 2, we start from the CT relationship of a 1st-order CT ΔΣ modulator [8],

$$y(t) = \int_0^t (x(t) - v(t))dt \,, \tag{1}$$

where $x(t)$ is the input signal, $y(t)$ is the output of the first CT integrator, and $v(t)$ is the CT DAC feedback signal. Assuming a non-return-to-zero (NRZ) feedback waveform out of the CT DAC, an equivalent model can be found (lower half of Fig. 2) which is described by the difference equation

$$y(n) = y(n-1) + x_{pf}(n-1) - v(n-1) \,, \tag{2}$$

where $x_{pf}(n) = \frac{1}{T_s}\int_{nT_s}^{(n+1)T_s} x(\tau)d\tau = (g_{pf} * x)(n)$ represents a zero-order-hold (ZOH) sampled value with $g_{pf}(t) = \begin{cases} 1/T_s, & -T_s \le t < 0 \\ 0, & \text{otherwise} \end{cases}$.

Taking the z-transform of (2), the CT integrator can be modeled as the step-invariant transform of $1/s$,

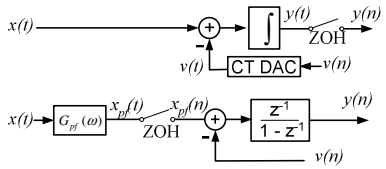

Fig. 2. DT modeling of the first-stage CT integrator.

$$y(z) = [x_{pf}(z) - v(z)]\frac{z^{-1}}{1-z^{-1}}, \tag{3}$$

as in Fig. 2. The pre-filter $G_{pf}(\omega)$, with the impulse response $g_{pf}(t)$, establishes a complete state value equivalence between the CT integrator and the DT model for an arbitrary input $x(t)$. The pre-filter $G_{pf}(\omega)$ also accounts for the inherent anti-aliasing effect of the CT first stage: the Fourier transform of $g_{pf}(t)$ results in $\left|G_{pf}(\omega)\right| = \left|\left(\sin(\frac{\omega T}{2})\right)/\left(\frac{\omega T}{2}\right)\right|$. Under an oversampling rate M, it provides an attenuation of $\left|\sin(\frac{2M-1}{2M}\pi)/(\frac{2M-1}{2M}\pi)\right|$ to the frequencies that alias into the passband band edge. This level of attenuation is approximately the same as that of a 1st-order Butterworth anti-aliasing filter with cutoff at the passband edge, but the inherent anti-aliasing rolls off much faster than the latter between $(\frac{2M-1}{2M})f_s$ and f_s. Moreover, in $G_{pf}(\omega)$, zeros at the multiples of f_s provide a first-order nulling to the frequencies aliasing into the DC. Therefore, if one stage of CT integrator is used, the order of the anti-aliasing filter preceding the modulator can be reduced by at least one.

Inherent anti-aliasing effect of a group of initial CT stages can be found by considering the corresponding prefilter [8]

$$G_{pf}(s) = \left.\frac{L_{oc}(s)}{L_{od}(z)}\right|_{z=e^s}, \tag{4}$$

where $L_{oc}(s)$ and $L_{od}(z)$ are the transfer functions of this group of CT stages and its equivalent DT model transfer function, respectively.

III. Design Methodology

We propose a general design flow to construct a CT-DT ΔΣ modulator as summarized in Fig. 3. Starting with a prescribed specification, we first build a DT modulator prototype. A DT initial model is used because there exist rich literature and software tools for designing conventional DT SC ΔΣ modulators [9], [10]. With the equivalence between the DT prototype and the final CT-DT ΔΣ modulator thus designed, we can perform analysis on the DT model which would carry over to the CT-DT modulator. Moreover, the modulator stability and integrator overloading condition can be analyzed easily on the DT model. The requirement of the anti-aliasing filter can also be specified at this stage. A rule of thumb of the minimum attenuation required is,

$$A_{\min} = 20\log(\sqrt{1.5}\times 2^B), \tag{5}$$

where *B* is the effective number of output bits in the analog-to-digital converter (ADC) to be designed [11]. In the early stage of the design process, the effective number of bits of a ΔΣ ADC can be estimated from the approximated dynamic range equation,

$$DR \approx \frac{3}{2}2^{2N}\frac{(2L+1)OSR^{(2L+1)}}{\pi^{2L}}, \tag{6}$$

where *OSR* is the oversampling rate, *L* is the order of the ΔΣ modulator and *N* is the number of the bits of the internal quantizer [12].

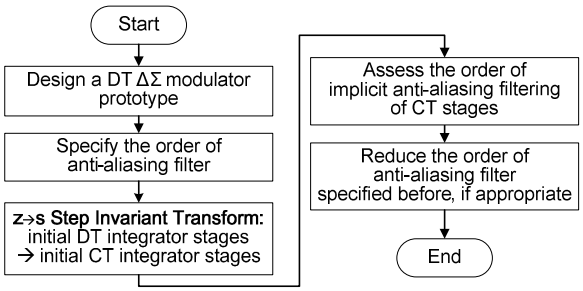

Fig. 3. Flowchart for the proposed CT-DT ΔΣ modulator design flow.

Next, the transfer function of the portion of the DT prototype loop filter that needs to be implemented by CT circuitry is written up. It is then converted into a CT counterpart by the z-domain to Laplace domain ($z \to s$) step invariant transform. Designer can decide the portion of DT stages to be converted to CT stages according to the inherent anti-aliasing filter wanted. Basically, for every integrator implemented with CT, the order of the anti-aliasing filter preceding the modulator can be reduced by at least one.

When there is no negative real pole in the DT loop filter transfer function, the $z \to s$ transform is unique and well-defined, e.g., see [13], and can be done by either: a ZOH pole mapping of $z_1 = e^{s_1 T_s}$ that maps the z-domain pole z_1 to a s-domain pole s_1; the `d2c` command in Matlab; or simple table lookup (e.g., Table 2 of [14]). This transformation assumes a NRZ CT DAC feedback waveform; however, any CT DAC feedback waveform of duration less than one clock period is acceptable with an extra step: increase the CT DAC feedback coefficients by a factor of $T_s / \int_0^{T_s} v(t)dt$, where $v(t)$ is the internal CT digital-to-analog-converter (DAC) feedback waveform.

The Laplace domain transfer function obtained is then mapped to CT integrator circuits. Cascading the CT circuitry and the portion of untransformed DT circuitry results in the final hybrid CT-DT structure with initial CT integrator stages and feedback DAC, which has a step response matched to that of the DT prototype. Ref. [2] uses a SC DAC instead of a CT DAC for further reducing the sensitivity to clock jitter. Our proposed methodology is also applicable to the design of this specific CT-DT ΔΣ modulator. Finally, the inherent anti-aliasing of CT stages is assessed according to (4) at frequency $(\frac{2M-1}{2M})f_s$, the frequency at which signal with frequency components higher than this would alias into the passband. If the attenuation to the aliasing signal by CT stages is sufficient, the order of the anti-aliasing filter preceding the modulator can be reduced or the filter can be removed accordingly.

IV. Design Examples and Simulation Results

We validate the proposed design methodology by applying it to different DT ΔΣ modulator prototypes. The first example is a 4th-order DT prototype from [15] as shown in Fig. 4(a). It is converted into a CT-DT modulator with two initial CT stages and two subsequent DT stages. The transfer function of the DT portion to be transformed (surrounded by dotted lines) is expressed as

$$X(z) = (\frac{0.1}{z-1})^2 U(z) - [(\frac{0.1}{z-1})^2 + (\frac{0.1}{z-1})]\cdot Y(z). \tag{7}$$

Taking the CT DAC waveform as NRZ, via any method mentioned in Section III, the equivalent CT model of the two initial stages can be found to be

$$X(s) = (\frac{0.01}{(sT_s)^2} - \frac{0.005}{sT_s})U(s) - (\frac{0.01}{(sT_s)^2} - \frac{0.105}{sT_s})\cdot Y(s). \tag{8}$$

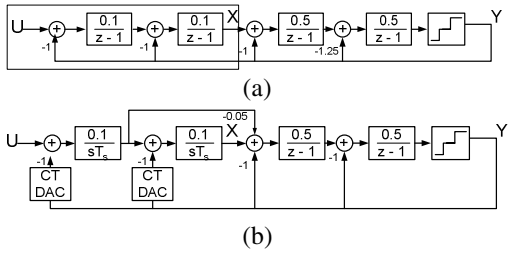

Fig. 4. (a) DT ΔΣ modulator prototype. (b) Designed CT-DT ΔΣ modulator.

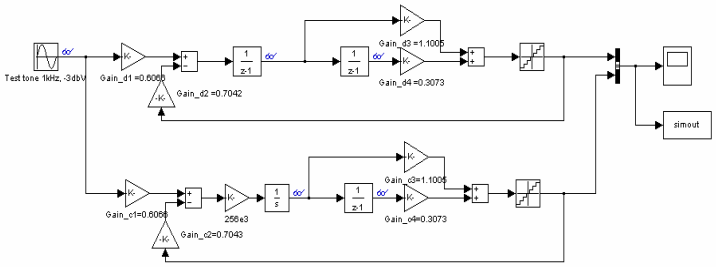

Fig. 5. Simulink setup for validating the proposed design methodology.

This portion of the transfer function is implemented by CT circuitry and cascaded with the untransformed portion of the prototype to give the final CT-DT ΔΣ modulator as shown in Fig. 4(b). The loop filters of the prototype and the designed CT-DT modulator are verified to have identical step response in the Matlab Simulink environment. Fig. 5 shows the setup up for verifying another design. The DT ΔΣ modulator in the upper part of the figure is another initial prototype designed with an oversampling rate $M = 64$ to further verify our design flow. The DT prototype is also converted to its CT-DT equivalence in the lower part of Fig. 5 according to the proposed design flow. Due to the high sampling rate, the anti-aliasing filter for the DT modulator is designed to be a 1st-order Butterworth lowpass filter. Fig. 6 shows the open-loop step responses of the DT and the CT-DT ΔΣ modulators, respectively. The two curves show that, when driven by a unit step input, the open-loop CT-DT and DT loop filters produce the same input values to the quantizer at the clocking instants. This demonstrates the equivalence of the CT-DT and DT ΔΣ modulators.

To demonstrate the inherent anti-aliasing feature of the CT-DT ΔΣ modulator, we clock the modulators equipped with 4-bits internal quantizer at 256kHz and digitize a 1kHz -3dBV signal tone added with a -13dBV noise tone at 255.5kHz. This noise tone will alias into the passband. Without any anti-aliasing filter, the CT-DT ΔΣ modulator achieves a SNR of 64dB, while the SNR of the DT prototype equipped with an additional 1st-order Butterworth filter is just 51dB. From Fig. 7, the inherent anti-aliasing of the CT-DT ΔΣ modulator provides a further 13dB attenuation on this aliasing tone.

Another test is performed to highlight the insensitivity of the CT-DT ΔΣ modulator against sampling errors, such as signal-dependent charge injection, clock feedthrough and sampled coupling harmonics in a mixed-signal environment. Since a ΔΣ modulator is a closed-loop system, the DAC feedback signal follows the input signal quite closely. We assume the signal to the integrators, i.e. difference between the input and DAC feedback, has a flat power spectrum as the quantization noise. We model all the sampling noises by a -120dB additive white noise at the positions where the CT signal is sampled into a DT signal, namely, at the inputs of the 1st DT integrator of the DT prototype and the 1st DT integrator of the designed CT-DT ΔΣ modulator. In this simulation, the CT-DT ΔΣ modulator achieves a SNR of 93dB, while the SNR of the DT

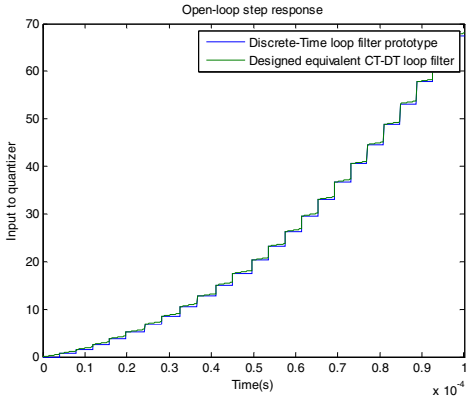

Fig. 6. Output plots showing the equivalence of the DT and CT-DT ΔΣ modulators by the open-loop step response.

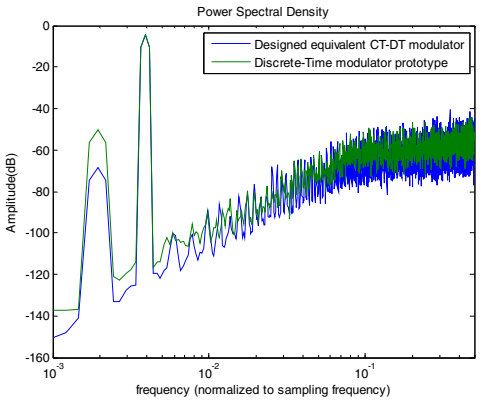

Fig. 7. Output plot (power spectral density) subject to an aliasing noise tone.

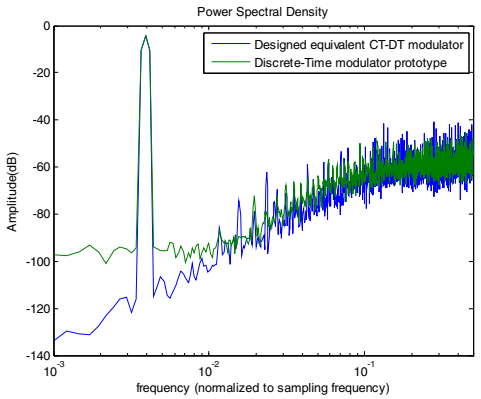

Fig. 8. Output plot (power spectral density) subject to sampling nonideality.

prototype is only 78 dB, as shown in Fig. 8. This difference can be equated to a gain of about 2.5 effective number of bits (ENOBs).

V. Multi-Stage Cascaded CT-DT ΔΣ Modulators

So far, most cascaded ΔΣ modulators in the literature use DT SC circuit in their implementations. CT cascaded modulators are proved feasible, but are still uncommon. Based on our design methodology, we propose to implement cascaded modulator with hybrid CT-DT circuitry. Fig. 9 (a) and (b) show a cascaded DT prototype and its CT equivalent, respectively. Fig. 9 (c) and (d) show the CT-DT implementations designed by our approach, with one and two

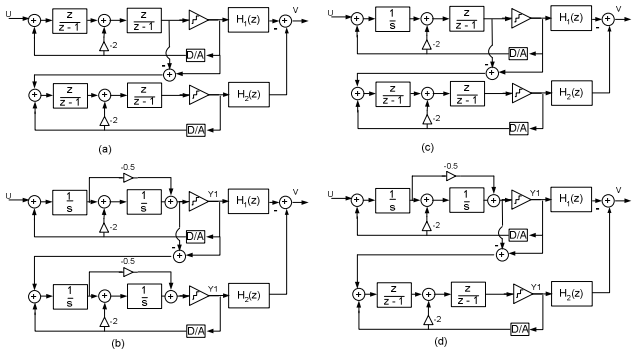

Fig. 9. (a) DT cascaded ΔΣ modulator prototype. (b) CT equivalent. (c) Designed CT-DT ΔΣ modulator with 1 CT integrator. (d) Designed CT-DT ΔΣ modulator with 2 CT integrators.

integrators implemented by CT circuitries, respectively. Monte Carlo simulations on these four topologies are carried out and the results are summarized in Table 1. The maximum SNR loss due to circuit mismatch is obtained by running 100 simulations assuming: (i) the DT circuit is implemented with SC circuit and the standard deviation of capacitor mismatch is less than 1%, as it is in the 0.18μm CMOS process; (ii) the CT circuitry is implemented by RC integrators, in which the standard deviation of the RC product mismatch is 10% (The absolute RC value can vary in the order of 20% in practice [7]).

From the simulation results, we can see that one of the CT-DT structures, the cascaded 2-2 ΔΣ modulator with first stage second order modulator implemented with CT circuit and a second stage modulator implemented with DT circuit (Fig. 9 (d)), can achieve the same level of anti-aliasing suppression as a cascaded 2-2 continuous-time ΔΣ modulator (Fig. 9 (b)) derived from the same DT cascaded ΔΣ prototype. Anti-aliasing filter can be omitted if the ADC is targeted at resolution equal to or less than 8 bits. Although it is more prone to circuit parameter mismatch than DT cascaded prototype (Fig. 9 (a)), it is still more robust against process variation than the cascaded 2-2 continuous-time topology, and the mismatch problem can be solved with suitable digital correction scheme, e.g. [16]. Furthermore, the DT-CT cascaded topology with only one CT integrator (Fig. 9 (c)) shows a clear tradeoff between the inherent aliasing filtering in complete CT cascaded topology and the insensitivity to mismatch in complete DT cascade topology. All these observations open up new possibility to design high-order ΔΣ modulators with inherent anti-aliasing feature by hybrid CT-DT cascaded topologies.

VI. Conclusion

A framework has been proposed to systematically design a CT-DT ΔΣ modulator based on the transformation from a conventional DT ΔΣ modulator prototype. Starting with a prescribed DT ΔΣ prototype, the methodology gives rise to a CT-DT ΔΣ modulator with a step-invariant response. Our method greatly reduces the design effort and the CT-DT ΔΣ modulator thus designed is readily realizable with conventional circuitry. Simulations have confirmed the efficacy of the CT-DT implementation. The novel idea of implementing cascaded ΔΣ topologies by hybrid DT-CT structure has also been explored, which shows promising performance and design tradeoff.

Table 1. Comparison between different implementations of cascaded 2-2 ΔΣ modulator.

	DT	CT-DT (1 CT integrator)	CT-DT (2 CT integrators)	CT
Anti-aliasing suppression (dB)	0	29.8	49.7	43.6
Max. SNR loss due to circuit mismatch (dB)	9.8	11.1	15.6	16.5

References

[1] K. Nguyen, R. Adams, K. Sweetland and H. Chen, "A 106-dB SNR hybrid oversampling analog-to-digital converter for digital audio," *IEEE Journal of Solid State Circuits*, vol. 40, no. 12, pp. 2408-2415, Dec. 2005.

[2] B. Putter, "A 5th-order CT/DT multi-mode ΔΣ modulator," to appear in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, Feb. 2007.

[3] V. F. Dias, G. Palmisano and F. Maloberti, "Noise in mixed continuous-time switched-capacitor sigma-delta modulators," *IEE Proc.*, vol. 139, no. 6, pp. 680-684, Dec. 1992.

[4] B. P. Del Signore, D. A. Kerth, N. S. Sooch and E. J. Swanson, "A monolithic 20-b delta-sigma A/D converter," *IEEE Journal of Solid State Circuits*, vol. 25, no. 6, pp. 1311-1316, Dec. 1990.

[5] R. Tortosa, A. Aceituno, J.M. de la Rosa, A. Rodriguez-Vazquez and F.V. Fernandez, , "A 12-bit@40MS/s Gm-C Cascade 3-2 Continuous-Time Sigma-Delta Modulator," *Proc. IEEE International Symposium on Circuits and Systems(ISCAS) 2007*, pp.1-4, May 2007.

[6] R. Tortosa, J.M. De La Rosa, F.V. Fernandez and A. Rodriguez-Vazquez, "A New High-Level Synthesis Methodology of Cascaded Continuous-Time ΔΣ Modulators," *IEEE Trans. on Circuits and Syst. II: Express Briefs* , vol.53, no.8, pp. 739-743, Aug. 2006.

[7] L. J. Breems, R. Rutten and G. Wetzker, "A cascaded continuous-time Sigma Delta Modulator with 67-dB dynamic range in 10-MHz bandwidth," *IEEE Journal of Solid-State Circuits,* , vol.39, no.12, pp. 2152-2160, Dec. 2004.

[8] R Schreier. and B. Zhang, "Delta-Sigma modulators employing continuous-time circuitry," *IEEE Trans. on Circuits and Syst. I*, vol.43, no. 4, pp. 324-332, Apr. 1996.

[9] R. Schreier and G. C. Temes, *Understanding delta-sigma data converters*. Piscataway, NJ: IEEE Press, 2005.

[10] R. Schreier. The delta-sigma toolbox 6.0(dec. 2004). [Online]. Available: http://www.mathworks.com/matlabcentral/fileexchange

[11] E. C. Ifeacher and B. W. Jervis, *Digital Signal Processing: A Practical Approach*. Harlow: Prentice Hall, 2002.

[12] R. del Rio, F. Medeiro, B. Perez-Verdu, J. M. de la Rosa and A. Rodriguez-Vazquez, *CMOS Cascade Sigma-Delta Modulators for Sensors and Telecom: Error Anlysis and Practical Design*. Netherlands: Springer 2006.

[13] I. Kollar, G. Franklin and R. Pintelon, "On the equivalence of z-domain and s-domain models in system identification," in *Proc. IEEE Instrumentation and Measurement Technology Conference 1996 (IMTC-96)*, vol. 1, pp. 14-19, June 1996.

[14] P. Benabes, M. Keramat and R. Kielbasa: "Synthesis and analysis of Sigma-Delta modulators employing continuous-time filters," *Analog Integrated Circuits and Signal Processing*, vol. 23, no.. 2, pp.141-152, May 2000.

[15] F.O. Eynde, M. Y. Guang and W. A. Sansen, "CMOS Fourth-order 14b 500k-sample/s Sigma-delta ADC Converter," *ISSCC Digest of Technical Papers*, pp. 62-290, Feb 1991.

[16] G. Cauwenberghs and G. C. Temes, "Adaptive digital correction of analog errors in MASH ADCs—Part I: Off-line and blind on-line calibration," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 621–628, July 2000.