A New Switched-Capacitor Boost-Multilevel Inverter Using Partial Charging

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***Abstract*—In this brief, a new switched-capacitor-boost-multilevel (SCBM) inverter is proposed and implemented. This inverter possesses the distinct features of both voltage boost up and near-sinusoidal staircase output voltage. The key is to utilize partial charging in such a way that multiple voltage steps per capacitor can be realized, hence significantly reducing the number of capacitors for a given number of levels. Based on using only two capacitors, a 13-level SCBM inverter is designed and analyzed, with emphasis on assessing its total harmonic distortion. Both simulation and experimental results are given to confirm the theoretical analysis.**

***Index Terms*—Boost converter, multilevel inverter, partial charging, switched capacitor.**

I. Introduction

With ever-increasing demand on power quality of electric supply, the development of multilevel converters has taken on an accelerated pace. Multilevel inverters are composed of an array of power switches and capacitor voltage sources in such a way that they generate output voltages with stepped waveforms [1]. They can work with either fundamental switching frequency or high switching frequency pulsewidth modulation (PWM) [2], [3]. The fundamental switching frequency multilevel inverters take the definite advantage of low switching loss since only several commutations of power devices are performed during one cycle of the output voltages, whereas the number of levels of the staircase waveforms needs to be increased so as to achieve low harmonic distortion.

There are three main topologies of multilevel inverters, namely the diode-clamped multilevel (DCM) one [4], capacitor-clamped multilevel (CCM) one [5], and cascaded multicell multilevel (CMM) one [6]. The DCM inverter is relatively simple, but needs a large number of diodes to clamp the switch voltage stress. The CCM inverter is more flexible than the DCM one, but similarly needs a large number of capacitors to clamp the voltage. Both the DCM and CCM inverters have a key drawback that there are no voltage boosting feature, namely the output peak-to-peak ac voltage must be the same as the input dc voltage. The CMM inverter is based on the series connection of single-phase inverters with separate dc sources. So, it can step up the input dc voltage to produce the ac output with higher voltage level. However, many isolated dc-dc converters are required to provide those dc sources.

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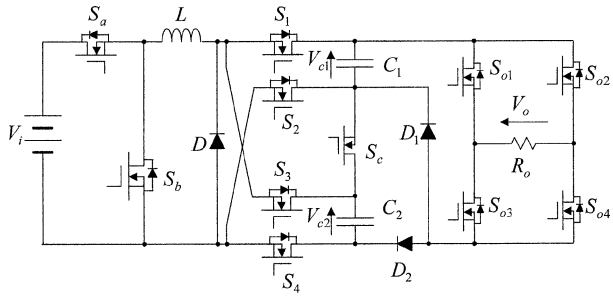

Fig. 1. Proposed SCBM inverter topology.

Recently, a cascade-boost-switched-capacitor converter multilevel inverter (CBSCM) has been proposed [7]. It takes the advantage that the input dc voltage can be stepped up to produce a higher ac voltage without requiring isolated dc sources. However, this CBSCM inverter suffers from the same drawback of those fundamental switching frequency multilevel inverters. Namely, in order to achieve low harmonic distortion, the number of levels needs to be increased, thus resulting in large numbers of capacitors, switches and diodes.

The purpose of this brief is to develop a new switched-capacitor-boost-multilevel (SCBM) inverter. It not only retains the advantageous features of the CBSCM inverter, but also can flexibly increase the number of levels without increasing the numbers of capacitors, switches and diodes. Hence, the proposed inverter can effectively convert a dc battery voltage to a higher ac voltage for various electric appliances. For exemplification, a 42-V 13-level SCBM inverter is design and implemented for automotive electronics [8].

The circuit topology and operating principle of the proposed SCBM inverter will be described in Section II. Then, in Section III, the design procedure will be elaborated, and Fourier analysis of the output voltage will be performed. Finally, PSPICE simulation and experimental verification will be given in Section IV.

II. Proposed Inverter

A. Circuit Topology

The proposed SCBM inverter is shown in Fig. 1, which consists of three stages—the partial charging stage, the switched capacitor stage and the inverter stage. Firstly, the partial charging stage is formed by two switches S_a, S_b, an inductor L, and a diode D. It is actually a combination of a buck converter and a boost converter that allows bidirectional energy flow between the input dc source V_i and the capacitors. During the first and third quarters of a cycle of the ac output, it operates as a buck converter which charges each capacitor to different voltage levels via S_a. During the second and fourth quarter of a cycle,

TABLE I
COMPARISON OF MULTILEVEL INVERTERS WITH 13-LEVEL OUTPUT

	No. of capacitors	No. of switches	No. of diodes
SCBM	**2**	**11**	**3**
DCM	12	24	132
CCM	66	24	0
CMM	6	24	0
CBSCM	6	10	12

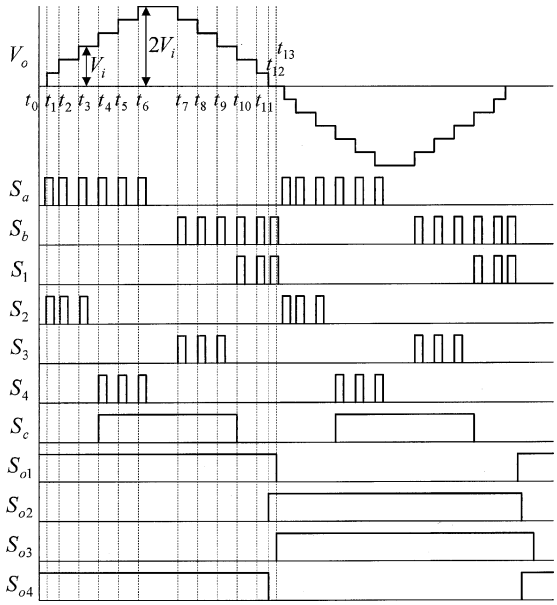

Fig. 2. Theoretical waveforms.

it operates as a boost converter which discharges the capacitors step by step via S_b. Secondly, the switched capacitor stage is formed by five switches S_1, S_2, S_3, S_4, S_c, two capacitors C_1 and C_2 and two diodes D_1 and D_2. Each capacitor is associated with a pair of switches so that it can be charged and discharged independently. The switch S_c in between two capacitors functions to properly add up the capacitor voltages to construct the staircase waveform. So, the number of capacitors and the associated switches can be flexibly increased to further increase the output voltage. Thirdly, the inverter stage is a classical inverter formed by two pairs of switches S_{o1}, S_{o2}, S_{o3} and S_{o4}, which is responsible for changing the polarity of the output voltage V_o. The partially inductive load is represented by L_o and R_o.

It should be noted that the proposed SCBM inverter has a distinct feature that the number of output levels depends only on the number of partial charging levels, and is independent of the number of capacitors. In contrast, the number of output levels and the number of capacitors are mutually coupled for other multilevel inverters. Thus, the SCBM inverter can flexibly increase the number of output levels without requiring additional capacitors and those associated switches and diodes. Taking a 13-level output voltage as an example, the proposed SCBM inverter is compared with the aforementioned multilevel inverters (DCM, CCM, CMM and CBSCM) in terms of the numbers of capacitors, switches and diodes. As listed in Table I, the proposed inverter takes the definite advantages of minimum hardware count and hence minimum production cost for a given number of output levels or limit of harmonic distortion.

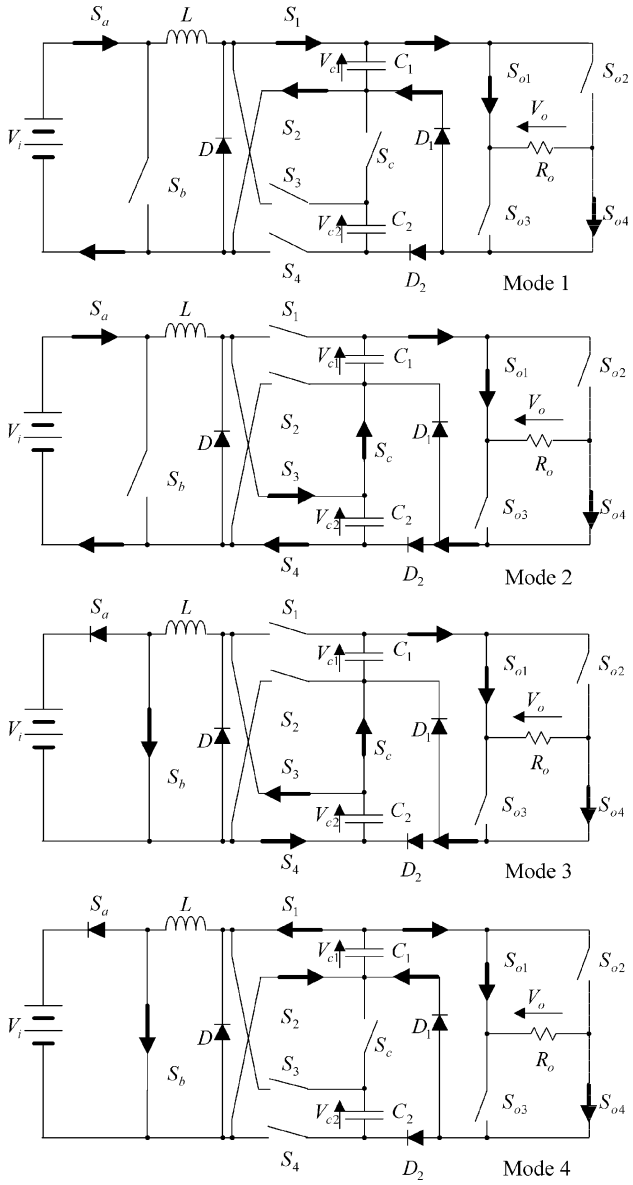

Fig. 3. Topological modes during positive cycle.

B. Operating Principle

The circuit goes through eight modes of operation per cycle. The waveforms of the output voltage and the gating signal of the switches are shown in Fig. 2. The four topological modes (Mode 1–Mode 4) during the positive cycle are illustrated in Fig. 3, whereas the other four modes (Mode 5–Mode 8) during the negative cycle are similar. At t_0, C_1 and C_2 are completely discharged at the end of the previous cycle.

1) Mode 1 [t_1, t_4]: The partial charging stage works as a buck converter. Both S_a and S_2 are turned on in such a way that C_1 is step-by-step charged to three different voltage levels, namely $V_i/3$, $2V_i/3$ and V_i. The corresponding gating pulses are applied at the instants t_1, t_2 and t_3, and hence the durations are determined by setting $V_o(t_1 + \Delta t_1) = V_i/3$, $V_o(t_2 + \Delta t_2) = 2V_i/3$ and $V_o(t_3 + \Delta t_3) = V_i$, respectively. Meanwhile, S_{o1} and S_{o4} are turned on so that V_o is positive.

2) Mode 2 [t_4, t_7]: Similar to Mode 1, S_a and S_4 are turned on in such a way that C_2 is step-by-step charged to $V_i/3$, $2V_i/3$

and V_i. At the same time, S_c is turned on so that C_1 and C_2 are connected in series. The gating pulses are applied at the instants t_4, t_5 and t_6, and the corresponding durations are determined by $V_o(t_4+\Delta t_4)=4V_i/3$, $V_o(t_5+\Delta t_5)=5V_i/3$ and $V_o(t_6+\Delta t_6)=2V_i$, respectively. Again, S_{o1} and S_{o4} are kept on to provide positive V_o.

3) Mode 3 [t_7, t_{10}]: The partial charging stage works as a boost converter. Both S_b and S_3 are turned on in such a way that C_2 is step-by-step discharged to $2V_i/3$, $V_i/3$, and 0. Since S_c is still turned on to connect C_1 and C_2 in series, the durations of the gating pulses applied at the instants t_7, t_8 and t_9 are determined by setting $V_o(t_7+\Delta t_7)=5V_i/3$, $V_o(t_8+\Delta t_8)=4V_i/3$ and $V_o(t_9+\Delta t_9)=V_i$, respectively. Again, S_{o1} and S_{o4} are kept on to provide positive V_o.

4) Mode 4 [t_{10}, t_{13}]: S_c is turned off so that C_1 and C_2 are disconnected. Similar to Mode 3, both S_b and S_1 are turned on in such a way that C_1 is step-by-step discharged to $2V_i/3$, $V_i/3$, and 0. The durations of the gating pulses applied at t_{10}, t_{11} and t_{12} are determined by $V_o(t_{10}+\Delta t_{10})=2V_i/3$, $V_o(t_{11}+\Delta t_{11})=V_i/3$ and $V_o(t_{12}+\Delta t_{12})=0$, respectively. S_{o1} and S_{o4} are kept on until C_1 is completely discharged. Then, S_{o4} is turned off and S_{o2} is turned on to enable freewheeling the inductive load current.

The operations of Mode 5, Mode 6, Mode 7, and Mode 8 are very similar to those of Mode 1, Mode 2, Mode 3, and Mode 4, respectively, except that S_{o2} and S_{o3} are turned on to reverse the polarity of V_o.

Additionally, current or power control can be realized by employing current feedback control which online compares the output current and reference current, hence adjusting the pulse durations. Namely, if the output current is higher than the reference, the pulse durations for the buck modes will be narrowed whereas those for the boost mode will be widened; and vice versa. Such adjustment of pulse durations needs to work with the criterion to be discussed in next section so that the desired waveform of V_o can be achieved.

III. Design and Analysis

A. Design Procedure

One key feature of the proposed SCBM inverter is the voltage boosting capability. Different from the CMM and CBSCM inverters in which the number of output levels and the peak output voltage are mutually coupled, the SCBM inverter takes the definite advantage that these two factors are decoupled so that the number of capacitors depends only on the stipulated value of output voltage. Thus, the voltage gain G of the proposed inverter is simply equal to the number of capacitors N_c as given by

$$G=\frac{\hat{V}_o}{V_i}=N_c. \tag{1}$$

Throughout the operation, each capacitor is step-by-step charged and then discharged so as to achieve p voltage steps per capacitor. For different modes of operation, the output voltage can be expressed as

$$V_o(t_k)=\begin{cases}\frac{kN_c}{2p}V_i, & k\le pN_c\\ \left(2N_c-\frac{k}{p}\right)V_i, & pN_c<k\le 2pN_c\end{cases} \tag{2}$$

where $k=1,2,\ldots,2pN_c$. In order to minimize the harmonic distortion, this output voltage should be close to a sinusoidal waveform as given by

$$V_o(t_k)=N_C V_i\sin\omega t. \tag{3}$$

For the proposed 13-level SCBM inverter using two capacitors, $p=3$ and $N_C=2$ are selected. Thus, the switching instants for the positive cycle are denoted as $t_k=\{t_1,\ldots,t_{12}\}$. By using (2), the corresponding output voltage is given by

$$V_o(t_k)=\left\{\frac{V_i}{3},\frac{2V_i}{3}\ldots,2V_i,\ldots\frac{2V_i}{3},\frac{V_i}{3}\right\}. \tag{4}$$

By substituting (4) into (3), the values of t_k for the positive cycle can be determined. Similarly, the switching instants for the negative cycle can readily be determined.

During the positive cycle, a series of pulses are applied to charge C_1 and then C_2. Taking L and R_L as the inductance and equivalent series resistance of the inductor, respectively, and C as the capacitance of each capacitor, it yields

$$V_i=R_L i+L\frac{di}{dt}+\frac{1}{C}\int i\,dt \tag{5}$$

where i is the instantaneous charging current. Since the partial charging stage operates in the discontinuous conduction mode, the inductor current is always zero at the beginning of each charging interval. Thus, by solving (5) with $V_c(t_k)$ as the initial capacitor voltage, the subsequent capacitor voltage $V_c(t)$ can be obtained as

$$\begin{aligned}V_C(t)&=(V_i-V_C(t_k))\left[1-e^{Bt}\left(\cos At+\sqrt{\frac{CR_L^2}{4L-CR_L^2}}\sin At\right)\right]\\&\quad+V_C(t_k)\end{aligned} \tag{6}$$

where the constants A and B are given by

$$A=\frac{1}{2}\sqrt{\frac{4L-CR_L^2}{CL^2}},\quad B=-\frac{R_L}{2L}. \tag{7}$$

Hence, by using (4) and (6), the durations Δt_1 to Δt_6 can be determined. Similarly, by further substituting $V_i=0$ into (6), the durations Δt_7 to Δt_{12} can be obtained.

B. Fourier Analysis

The harmonic contents of the output voltage can be determined by using Fourier series

$$V_o(t)=a_0+\sum_{n=1}^{\infty}(a_n\cos n\omega t+b_n\sin n\omega t). \tag{8}$$

Since $V_o(t)$ is an odd function, $a_n=0$ and b_n is given by

$$b_n=\frac{2}{T}\int_0^T V_o(t)\sin(n\omega t)dt. \tag{9}$$

By substituting (2) into (9), b_n can be expressed as

$$\begin{aligned}b_n=V_i&\left(\sum_{x=1}^{pN_c}\frac{kN_c}{2p}(\cos n\omega t_x-\cos n\omega t_{x+1})\right.\\&\left.+\sum_{y=pN_c+1}^{2pN_c}\left(2N_c-\frac{k}{p}\right)(\cos n\omega t_y-\cos n\omega t_{y+1})\right).\end{aligned} \tag{10}$$

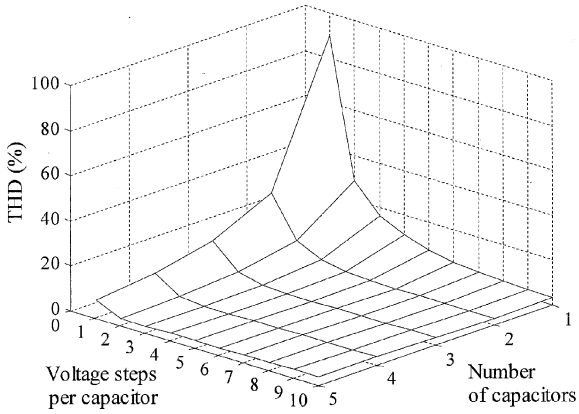

Fig. 4. THD versus levels of partial charging and number of capacitors.

Apart from assessing the whole harmonic spectrum, a commonly used parameter for assessing the harmonic distortion is the total harmonic distortion (THD). The THD of a voltage waveform is defined as

$$\mathrm{THD} = \sqrt{\frac{\sum_{n=2}^{\infty} V_n^2}{V_1^2}} \tag{11}$$

where V_1 and V_n are the fundamental and n-th harmonic voltage components, respectively. Since $V_n = b_n/\sqrt{2}$, (11) can be rewritten as

$$\mathrm{THD} = \sqrt{\frac{\sum_{n=2}^{\infty} b_n^2}{b_1^2}}. \tag{12}$$

By using (10) and (12), the THD can be numerically expressed in terms of p and N_C. The relationship is plotted in Fig. 4. Hence, the designer can easily assess whether the newly designed SCBM inverter complies with the stipulated THD value. For the proposed inverter with $p = 3$ and $N_C = 2$, the estimated THD is 6.97%.

IV. Results

A. PSPICE Simulation

As shown in Fig. 1, the proposed 13-level SCBM inverter is designed with $V_i = 42$ V, $L = 40$ μH, $C_1 = 800$ μF, $C_2 = 800$ μF, $R_o = 70$ Ω and $p = 3$. The output voltage frequency is set at 50 Hz. The whole inverter circuit is practically simulated by using PSPICE. The simulated waveforms of V_o, V_{C1}, I_{C1}, V_{C2}, and I_{C2} are shown in Fig. 5. As expected, the output voltage closely follows a sinusoidal waveform. By integrating the products of V_{C1} and I_{C1} as well as V_{C2} and I_{C2} with respect to time, the energy losses of C_1 and C_2 for a complete charging and discharging cycle are only 0.063 and 0.086 J, respectively. These losses can significantly be reduced by using recently available ultracapacitors which offer much lower equivalent series resistance (ESR) than those electrolytic capacitors. Also, such losses can further be reduced by using larger p to decrease the amplitudes of I_{C1} and I_{C2}.

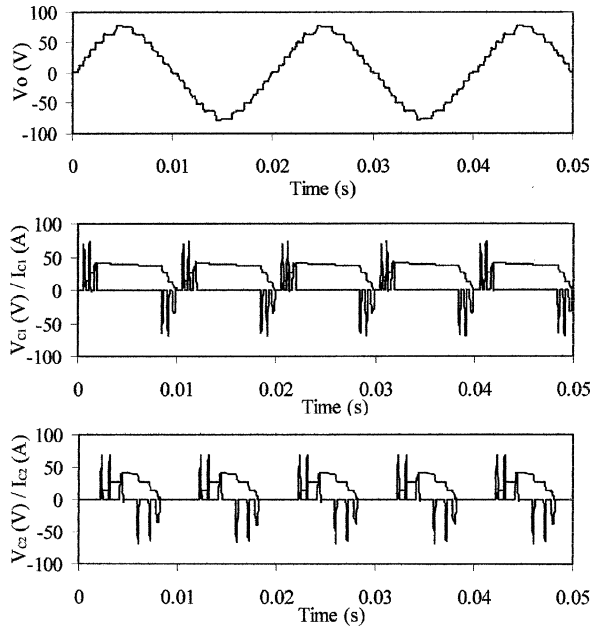

Fig. 5. PSPICE-simulated waveforms.

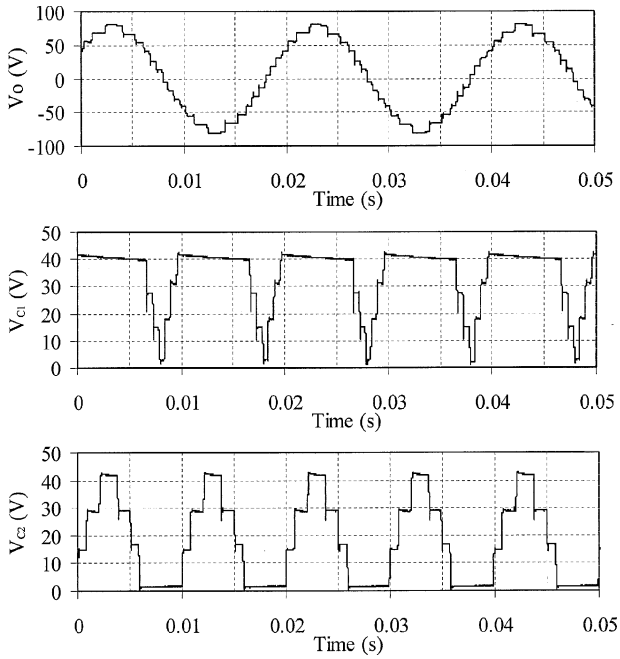

Fig. 6. Measured waveforms.

B. Experimental Verification

Based on the design for PSPICE simulation and the use of MOSFET IRF540 as power switches and MUR10100 as power diodes, the proposed inverter is prototyped. At the rated output power of 40 W, the waveforms of V_o, V_{C1}, and V_{C2} are measured as shown in Fig. 6. It can be seen that the measured waveforms well agree with the simulated ones shown in Fig. 5. Those slight discrepancies are mainly due to the manufacturing tolerance of power switches, diodes and capacitors.

It should be noted that the load is purposely selected as purely resistive so as to illustrate that the proposed inverter operation does not reply on load inductance. Actually, the load can be

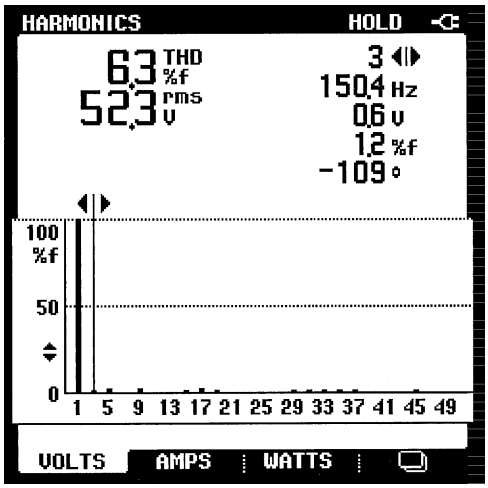

Fig. 7. Measured output voltage spectrum.

TABLE II
HARMONIC CONTENTS

Order	Magnitude (%)
1	100
3	1.1
5	2.3
7	0.6
9	2.7
11	0.3
13	1.0
15	1.3

partially inductive or capacitive, which will certainly provide a more sinusoidal load current.

The harmonic contents of V_o are directly measured by using the Fluke 43B power quality analyzer. The measured voltage spectrum is shown in Fig. 7, and the corresponding magnitudes of the first 15 harmonics are listed in Table II. Without using any filter or inductor at the output terminals, the measured THD of V_o is found to be 6.3%, which well agrees with the theoretical value estimated by (12).

In order to assess the harmonic distortion of the proposed inverter, the output resistor is varied to change the output power from no-load to full-load (40 W). Fig. 8 shows the variation of THD with respect to p.u. output power. It indicates that the THD changes from 5.5% at no-load to 6.3% at full-load, hence the increase of THD due to the loading effect is only 0.8%.

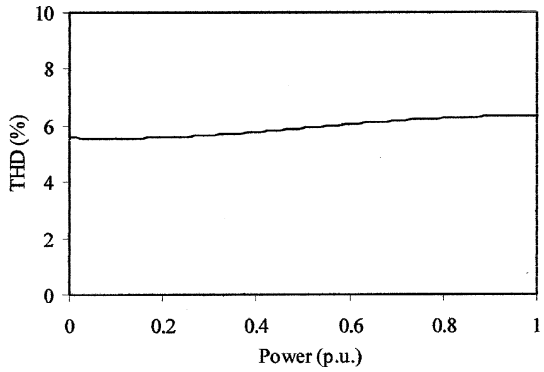

Fig. 8. Measured output voltage THD versus output power.

V. CONCLUSION

A new 13-level SCBM inverter has been proposed and implemented. The key is to utilize partial charging in such a way that multiple voltage steps per capacitor can be realized. The distinctive merit of the proposed inverter is that it can flexibly increase the number of output levels without requiring additional capacitors and the associated switches and diodes. Therefore, for a given limit of THD, the SCBM inverter can offer the minimum hardware count and hence minimum production cost.

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