Low Output Ripple DC–DC Converter Based on an Overlapping Dual Asymmetric Half-Bridge Topology

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Abstract—A new converter topology is described for applications requiring very low output current ripple. The proposed converter consists of two asymmetric half-bridge converters whose output voltages overlap in a finite interval of time. This converter provides well regulated and smooth dc output without the need of an output filter. The output voltage is regulated by direct amplitude modulation. Unlike the standard interleaved converters, the proposed converter is robust to input voltage and operating duty cycle variations. Furthermore, equal current sharing is automatically achieved under all conditions, thus ensuring full utilisation of the output rectifiers for wide input and output ranges. The circuit achieves zero-voltage turnon for all primary switches and zero-current turnoff for the output rectifiers. An isolated dc–dc converter prototype with 5-V output voltage and 20-A output current has been built to verify the design.

Index Terms—DC–DC converter, half-bridge converter, low output ripple, zero-current turnoff, zero-voltage turnon.

I. INTRODUCTION

LOW output current ripple is an important design criterion for dc–dc converters, especially for low-voltage applications. The removal of current ripple is traditionally achieved by output filtering. However, output filtering incurs significant loss which lowers the efficiency of the converter. Also, in practice, output filters take up considerable amount of space and limit the operating temperature. If high-capacity electrolytic capacitors are used, the converter may suffer a reduced life-time. Recently, parallel-connected dc–dc converters with interleaved operating cycles have been a popular design choice for achieving smooth dc output [1]–[4]. However, interleaving can satisfactorily reduce output current ripple only for a narrow range of operating points and the cancellation process is sensitive to input voltage and operating duty cycle variations. Alternatively, a two-stage converter has been proposed to provide low-ripple output [5]. However, the additional cascaded buck regulating stage in-
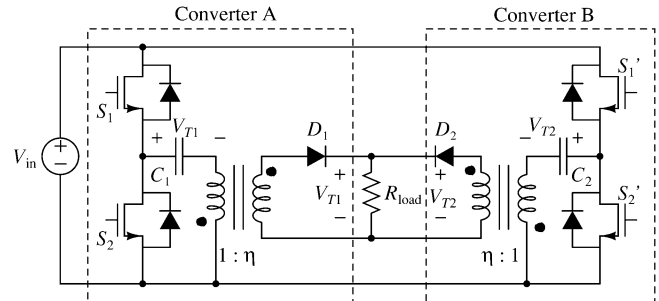
Fig. 1. Basic circuit topology of the proposed low-ripple output dc–dc converter.

evitably lowers the overall conversion efficiency. In this paper we propose a new converter topology which provides smooth dc output for wide ranges of input and load conditions, using very small output filters. The circuit, consisting of two overlapping asymmetric half-bridge converters, is easy to implement, insensitive to input voltage and operating duty cycle changes, and naturally achieves zero-voltage turnon of primary switches and zero-current turnoff of output rectifiers. The rest of the paper is organized as follows. We will introduce the basic topology in the next section, and describe the detailed operation in Section III. Experimental verification will be presented in Section V.

II. OPERATING PRINCIPLE OF NEW LOW-RIPPLE DC–DC CONVERTER

The proposed converter topology is conceptually shown in Fig. 1. It consists of two identical asymmetric half-bridge converters [6], [7] with their outputs connected in parallel. Referring to Fig. 1, S_1 and S_2 in converter A are driven asymmetrically with duty cycle always less than 0.5. The gate drive signals for the switches are shown in Fig. 2(a). Note that a dead time T_d is introduced to prevent cross conduction between S_1 and S_2, as well as to allow zero-voltage turnon of the two switches [8]–[11]. When S_1 is on, capacitor C_1 is charged up by the magnetizing current of T_1. At the same time, the polarity of T_1 is arranged such that D_1 is off. Proper design of the magnetizing inductance of T_1 will enable S_2 to turn on at zero voltage after S_1 is off. The energy stored in C_1 will then discharge through the primary winding of T_1 and S_2, and be coupled to the secondary circuit with D_1 forward biased. At this moment, the output voltage V_{out} is equal to V_{T1} which is simply ηV_{C1}, where η is the turns ratio of the output winding to the primary winding of T_1.

The operation of converter B is the same as that of converter A, with the gate drive signals for S_1' and S_2' in anti-phase to those of S_1 and S_2. The gate drive signals arrangement for $S_1, S_2, S_1',$
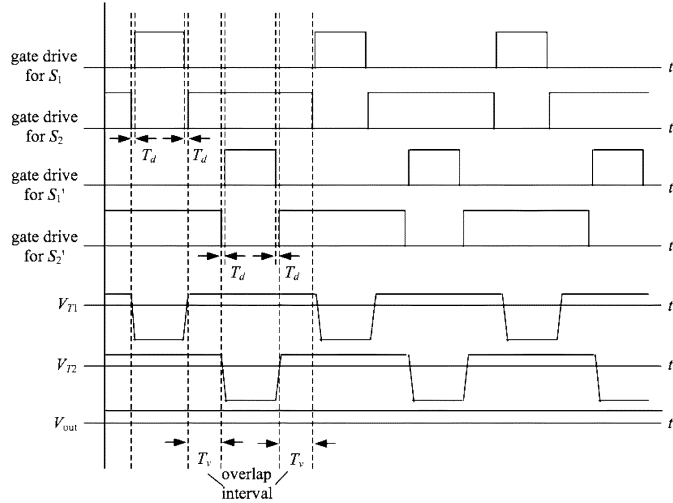
Fig. 2. Driving signals for the primary switches, transformer secondary voltages and output voltage, showing the key feature of overlapping intervals.
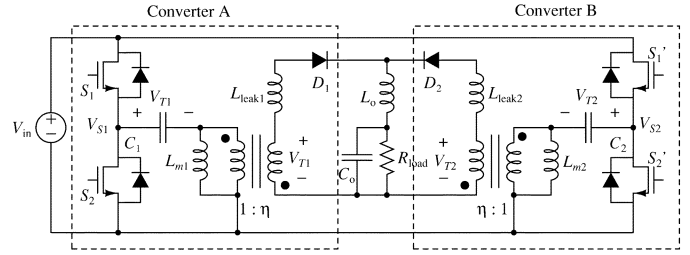

Fig. 3. Detailed circuit schematic of the proposed low-ripple output dc–dc converter including transformer magnetizing and leakage inductances and a very small output filter.

and S_2' makes sure that the on-periods of S_2 and S_2' always overlap for two intervals of duration T_v when the duty cycle is less than 0.5, as illustrated in Fig. 2. Here we assume that T_d is much less than the switching period and thus can be ignored.

The overlapping interval is the key feature of the proposed topology which ensures that there is always a dc voltage, equal to either ηV_{C1} or ηV_{C2}. If C_1 and C_2 are large enough, then the output voltage is a smooth and constant dc voltage whose magnitude is given by

$$V_{\text{out}} = \eta V_{C1} = \eta V_{C2} \tag{1}$$
$$V_{\text{out}} = \eta D V_{\text{in}} \tag{2}$$

where D is the duty cycle and η is the turns ratio of transformers T_1 and T_2. Note that the dynamic range of D is from 0 to 0.5.

It is worth noting that since the two converters are identical and symmetrically connected, the currents shared by the two output rectifiers are equal under all conditions, thus ensuring full utilization of the output rectifiers.

III. CIRCUIT OPERATION

In this section we describe the detailed operation of the proposed converter, taking into account the effects of the parasitic components such as the magnetizing and leakage inductances of the main transformers. We will show that with a proper choice of the primary series capacitors, the output rectifiers can be turned off at zero current. This greatly reduces the switching loss and reverse recovery loss of the output rectifiers.

Fig. 3 shows the detailed circuit schematic of the proposed converter. It should be noted that an output filter consisting of an inductor L_o and a capacitor C_o has been included. However, unlike conventional output LC filters which are required to filter out the rectified square voltage pulse in order to provide smooth dc output, this output filter is simply required to remove unwanted high-frequency voltage ringings and the ripple voltage reflected from C_1 and C_2. Thus, the size of this output filter can be much smaller than that of conventional output filters.

The gate drive signals for the switches, as described in Section II, produce pulsating voltages V_{S1} and V_{S2} across the primary windings of transformers T_1 and T_2 and their series connected dc blocking capacitors C_1 and C_2, as indicated in Fig. 3.

A. Current Commutation During Overlap Periods

Due to the presence of leakage inductances of T_1 and T_2, the output load current commutes from one converter to the other during each overlap period. The detailed waveforms with complete current commutation during the overlap period are shown in Fig. 4. Such commutation allows the output rectifiers to turn off at zero current. At t_1, the output current starts to commutate from converter B to converter A and ends at t_2, and likewise the output current starts to commutate from converter A to converter B at t_4 and ends at t_5.

The average current commutation rate I_r depends on the average voltage across the two leakage inductors L_{leak1} and L_{leak2}. It is equal to the average voltage difference, V_{cmm}, between C_1 and C_2 reflected to the secondary sides during the commutation periods. With $L_{\text{leak1}} = L_{\text{leak2}} = L_{\text{leak}}$, I_r is given by

$$I_r = \frac{V_{\text{cmm}}\eta}{2L_{\text{leak}}}. \tag{3}$$

The commutation ends when the output current is completely taken over by the other converter. The commutation time T_c is given by

$$I_r T_c = I_o. \tag{4}$$

The condition that ensures complete current commutation is that T_c should be less than the overlap period T_v, i.e.,

$$T_v = \left(\frac{1}{2} - D\right)T. \tag{5}$$

Thus, the condition for complete current commutation is given by

$$T_c \leq \left(\frac{1}{2} - D\right)T. \tag{6}$$

The essential parameter V_{cmm} can be calculated by first finding the current flowing through C_1 and C_2. The current waveforms I_{C1} and I_{C2} for capacitor C_1 and C_2 are shown in Fig. 4. It can be observed that the capacitor current is equal to the difference between the two current components, namely, the mag-
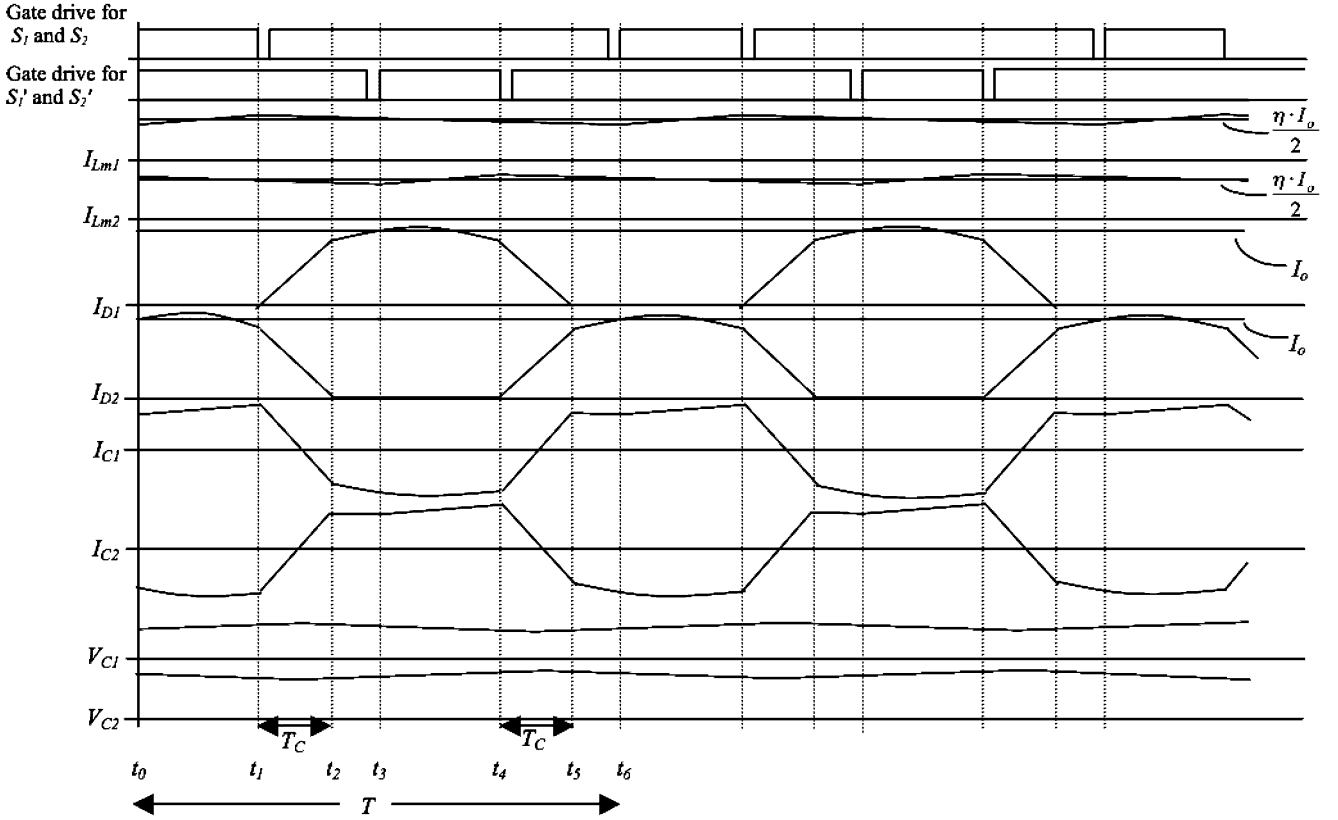
Fig. 4. Detailed operating waveforms showing commutation between converters during overlap periods.

netizing current and the reflected output current of the corresponding transformers and converters. Suppose $C_1 = C_2 = C$ and $L_{m1} = L_{m2} = L_m$. Referring to the capacitor current waveforms shown in Fig. 4, we can readily show that

$$V_{\mathrm{cmm}} = \frac{1}{C}\left[\frac{\eta(3T - 4T_c)}{12}I_o - \frac{(1-2D)T - 2T_c}{8(1-D)}\Delta I_{Lm}\right] \qquad (7)$$

where ΔI_{Lm} is the peak-to-peak value of the magnetizing current. Solving (3), (6), and (7), we get

$$T_c = \frac{1}{2b_1}[-b_2 + \sqrt{b_2^2 + 4b_1 b_0}] \qquad (8)$$

where

$$b_0 = \frac{2L_{\mathrm{leak}}I_o}{\eta}, \quad b_1 = \frac{1}{C}\left[\frac{\Delta I_{Lm}}{4(1-D)} - \frac{\eta I_o}{3}\right]$$

$$b_2 = \frac{1}{C}\left[\frac{\eta T}{4}I_o - \frac{(1-2D)T}{8(1-D)}\Delta I_{Lm}\right].$$

Since (6) has to be satisfied in order to ensure complete current commutation, the blocking capacitance should satisfy

$$C \le \frac{\eta^2 T_v}{24 L_{\mathrm{leak}}}(3T - 4T_v). \qquad (9)$$

Usually, since ΔI_{Lm} is small by design, the commutation time T_c can be approximated as

$$T_c \approx \frac{1}{8\eta}(3\eta T - \sqrt{9\eta^2 T^2 - 384 L_{\mathrm{leak}}C}) \qquad (10)$$

which provides important information on the characteristics of T_c. Specifically, T_c can be considered as constant and independent of the output current and input voltage when the magnetizing ripple current is insignificant compared to its dc component.

B. Output Ripple Current Analysis

At any time other than the commutation period, only one converter is supplying current to the load. Referring to Fig. 4, from t_2 to t_4, the dc blocking capacitor C_1 is discharged by the reflected output current and at the same time charged by the magnetizing current of T_1. To estimate the rate of change of the capacitor voltage, we assume that the output peak-to-peak ripple current ΔI_o is small compared to the output current I_o. Thus, the magnetizing current is approximately equal to $\eta I_o/2$, i.e.,

$$\frac{dV_{\mathrm{c1}}}{dt} = -\frac{\eta I_o}{2C}. \qquad (11)$$

The voltage drop across the output inductor L_o and the leakage inductance L_{leak} is imply the reflected voltage of C_1 minus the output voltage V_o. Since the output voltage is regulated, the output inductor current i_{Lo} is given by

$$\frac{d^2 i_{Lo}}{dt^2} = -\frac{\eta^2 I_o}{2(L_o + L_{\mathrm{leak}})C}. \qquad (12)$$
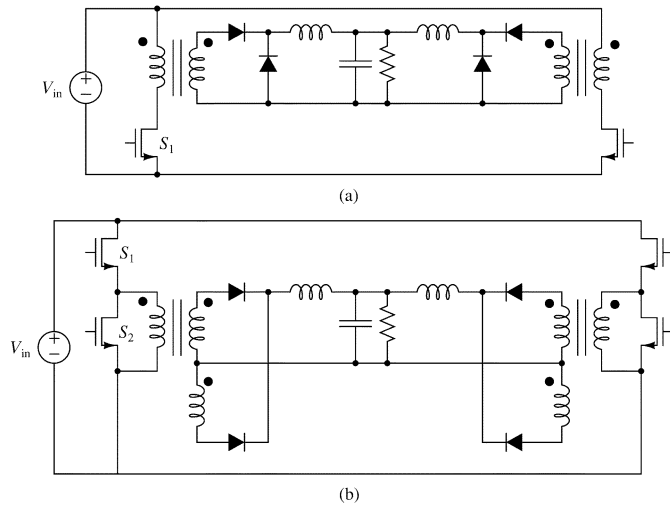
Fig. 5. Conventional topologies for comparison. (a) Interleaved dual forward topology. (b) Interleaved dual half-bridge topology.

Since V_o is equal to the average voltage across C_1 during the conduction interval, we can solve (12) to get the output current from which we have

$$\Delta I_o = \frac{\eta^2 I_o}{16(L_o + L_{\text{leak}})C} \left(\frac{T}{2} - T_c \right)^2 . \qquad (13)$$

Thus, we see that the ripple current is proportional to the output current and is insensitive to variation of the input voltage. Also, the ripple current amplitude can be reduced by increasing the inductance of the output filtering inductor and maximizing the capacitance of the dc blocking capacitor in accordance with (9) in order to maintain the zero-current turnoff condition for the output rectifier.

IV. COMPARISON WITH CONVENTIONAL TOPOLOGIES

Low-ripple dc–dc converters have been widely discussed in the literature. Two topologies from directly interleaving two dc–dc converters are particularly popular, i.e., the interleaved dual forward topology and the interleaved dual half-bridge topology for low power and medium-high power applications, respectively, as shown in Fig. 5. Both topologies require an additional second-stage filter. Comparing our proposed topology with these conventional ones, we can make several observations, as described below.

A. Power Component Counts

First of all, the power component count in the proposed topology is less. Our proposed topology has nine power components, including four primary-side MOSFETs, two isolation transformers, two output rectifiers, and one small output filter choke. The interleaved dual forward topology has 10 power components, including two primary-side MOSFETs, two isolation transformers, four output rectifiers, and two small output filter chokes. The interleaved dual half-bridge topology has 12 power components, including four primary-side MOSFETs, two isolation transformers, four output rectifiers, and two small output filter chokes.

B. Utilization of Power Transformers

The main transformers T_1 and T_2 work as both a flyback and a forward transformer. Referring to Converter A in Fig. 3, when the high-side switch S_1 is turned on, energy is transferred from the input to the magnetizing inductance of transformer T_1, and also to the dc blocking capacitor C_1. Energy transfer to the output takes place when S_2 is turned on. Thus, T_1 works as a flyback transformer. At the same time when S_2 is on, the energy stored in C_1 is transfered to the magnetizing inductance as well as to the output. In this sense, T_1 also works as a forward-type transformer, as it transfers energy directly to the output from C_1 when S_2 is turned on. A likewise operation can be found in Converter B and transformer T_2. Moreover, the flyback operation of the main transformers simplifies the output circuit configuration, as compared to the conventional dual forward topology. Only one rectifier is needed for each converter at the output in our proposed topology.

C. Device Stresses and Main Losses

To compare the stresses on the devices, we consider the voltage on the primary switches and the mean squared values of the primary and secondary switch currents.

For the interleaved dual forward topology, the voltage stress on the primary switch is $V_{\text{in}}/(1\text{-}D)$ and hence can be very high at large duty cycles. It is readily shown that the mean squared primary switch current is I_{in}^2/D, where I_{in} is the average input current and $D \leq 0.5$ normally. The mean squared currents for the two secondary switches are $I_o^2 D$ and $I_o^2(1 - D)$, where I_o is the output current.

For the interleaved dual half-bridge topology, the voltage stress is equal to V_{in}, which is a reasonable figure. The mean squared current of each of the primary switches is I_{in}^2/D, where $D \leq 0.5$. Moreover, the mean squared current of each of the two secondary switches is $I_o^2 D + 0.25 I_o^2(1\text{-}2D)$.

For the proposed topology, the voltage stress is same as that of the interleaved dual half-bridge topology, which is lower than that of the interleaved dual forward topology. It can be readily shown that the mean squared currents in the primary switches are I_{in}^2/D and $I_{\text{in}}^2/(1\text{-}D)$. Thus, we see that the current stress in one of the primary switches can be lower than that in the conventional interleaved topologies since $D \leq 0.5$. Moreover, the mean squared current in each of the secondary switches is $2I_o^2[1 - 2T_c/3T]$.

To probe further into the current stresses in the secondary switches, we may compare the conduction losses in the interleaved dual half-bridge topology and the proposed topology. For a fair comparison we assume that the sizes of the devices used in both topologies are identical. Suppose R is the on-resistance of each of the rectifiers (typically synchronous rectifiers) used in the interleaved dual half-bridge topology. Then, the on-resistance of each of the rectifiers used in the proposed topology will be $R/2$. Therefore, the total conduction loss in the rectifiers for the interleaved dual half-bridge topology is

Rectifier Loss$_{\text{interleaved half−bridge}}$
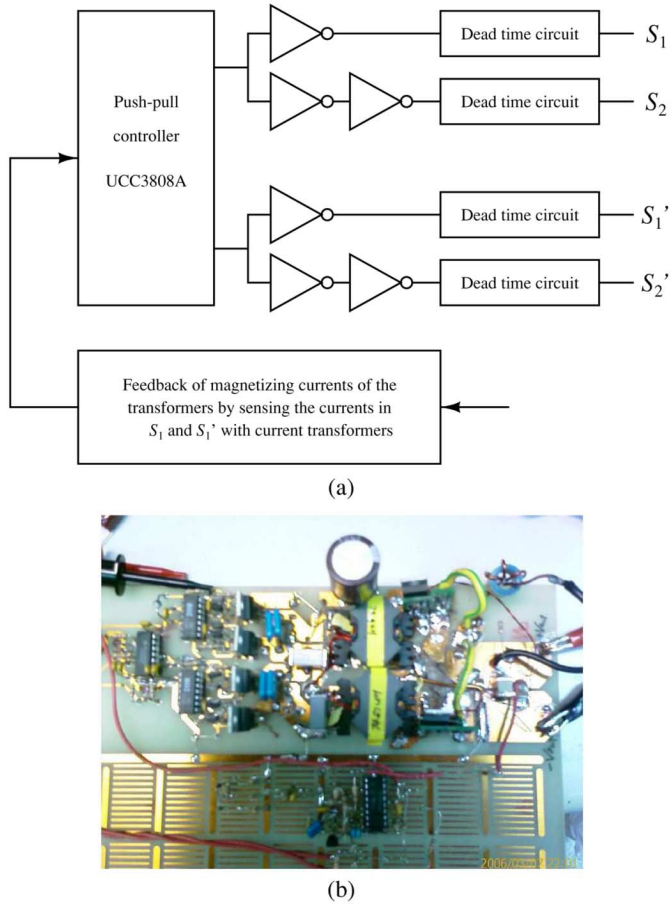$$= 4R \left[I_o^2 D + 0.25 I_o^2(1 - 2D) \right] \qquad (14)$$

(a)

(b)

Fig. 6.　(a) Control circuit schematic and (b) photo of the converter.

and that of the proposed topology is

$$\text{Rectifier Loss}_{\text{proposed}} = 2RI_o^2 \left[1 - \frac{2T_c}{3T}\right]. \qquad (15)$$

Clearly, the two topologies have the same loss for $D = 0.5$ and $T_c = 0$. Also, the rectifier loss in the interleaved dual half-bridge topology decreases with D, whereas that in the proposed topology is independent of D. However, when low output ripple is required, D must be kept very close to 0.5.

Finally, the proposed topology provides ZVS in the primary switches and ZCS in the output rectifiers, whereas the two conventional interleaved topologies do not. The loss due to transformer leakage in the proposed topology is recovered, whereas that in the two conventional interleaved topologies is dissipated. This further reduces the overall loss in the proposed topology.

V. EXPERIMENTAL VERIFICATION

A dc–dc converter using the afore-described topology has been built and tested. The input range is 36 to 72 V, the output voltage is 5 V, and the output current is 20 A (i.e., 100 W output power). To improve the efficiency, we have employed active diode technology for realizing the output rectifiers D_1 and D_2 [12], [13]. The control circuit of the prototype is realized by a push-pull PWM controller UCC3808A, as shown in Fig. 6. Each output of the push-pull controller is divided into two asymmetric signals by logic inverter gates to drive the upper and lower switches. The dead time for ensuring zero-voltage turnon operation is implemented by an RC delay circuit. Furthermore, a current-mode control scheme is employed to control the magnetizing current of the two transformers by sensing S_1 and S_1'. This control effectively balances the output currents from the two converters as the magnetizing current is proportional to the output current.

A. Selection of Components

First of all, from (2), the transformer turns ratio for T_1 and T_2 should satisfy $\eta \geq 2V_{\text{out}}/V_{\text{in,min}}$, where $V_{\text{in,min}}$ is the minimum input voltage and is about 36 V in this case. Thus, $\eta \geq 0.278$. In our circuit, we set $\eta = 0.347$.

To prevent transformer core saturation, the magnetizing inductance L_m at primary side, the number of turns at primary side N_{primary} and effective core area A_{eff} should satisfy

$$B_{\text{core}} = \frac{L_m I_{Lmp}}{N_{\text{primary}} A_{\text{eff}}} \leq B_{\text{sat}} \qquad (16)$$

where B_{core} is the flux density of the core, I_{Lmp} is the peak primary magnetizing current, and B_{sat} is the saturation flux density. In our circuit, the cores used are RM10 and the core material is 3C96 from Ferroxcube. The magnetizing inductances L_{m1} and L_{m2} are 75 μH and the measured output leakage inductance L_{leak} is 101 nH (including connection wiring to the output synchronous rectifiers D_1 and D_2). The number of primary turns N_{primary} is 14, and the effective area A_{eff} is 96.6 mm^2. The calculated peak primary magnetizing current I_{Lmp} is 4.323 A, corresponding to maximum input voltage. The calculated core flux density is 0.257 T, which is well below $B_{\text{sat}} = 0.43$ T for this material.

The maximum reverse voltage of the output rectifiers is ηV_{in}. At maximum input voltage (72 V) and $\eta = 0.347$, the required minimum reverse breakdown voltage of the rectifiers is 24.98 V. In our circuit, we choose MOSFET HUF76145P3 for D_1 and D_2, which has a reverse breakdown voltage of 30 V and on-resistance of 4.5 mΩ.

The switching frequency is set to 100 kHz and the output voltage is regulated at 5 V. To ensure zero-current turnoff of the output rectifiers, C_1 and C_2 should be less than 1.151 μF at 36 V dc input. For practical purposes, 1 μF metallized capacitors are employed. The inductance and capacitance of the output small LC filter are 900 nH and 100 μF (ceramic capacitor), respectively.

B. Results

Fig. 7 shows the measured waveforms of V_{s1}, V_{C1}, the gate drive signals of S_2 and S_2', the current of $D_1(I_{D1})$ and of $L_o(I_{Lo})$ at minimum and maximum inputs as well as light and full load conditions. The output inductor current waveforms are parabolic that matches with (12). The waveform of I_{D1} clearly shows that it falls to zero before S_2 turns off in all cases. The measured parameters, T_c and ΔI_o, are compared with the calculated values, as shown in Table I. The results show that the derived equations provide good estimation of the commutation time and output ripple current amplitude. It can also be observed that the measured output ripple current is insensitive to input voltage variations, which is consistent with (13).
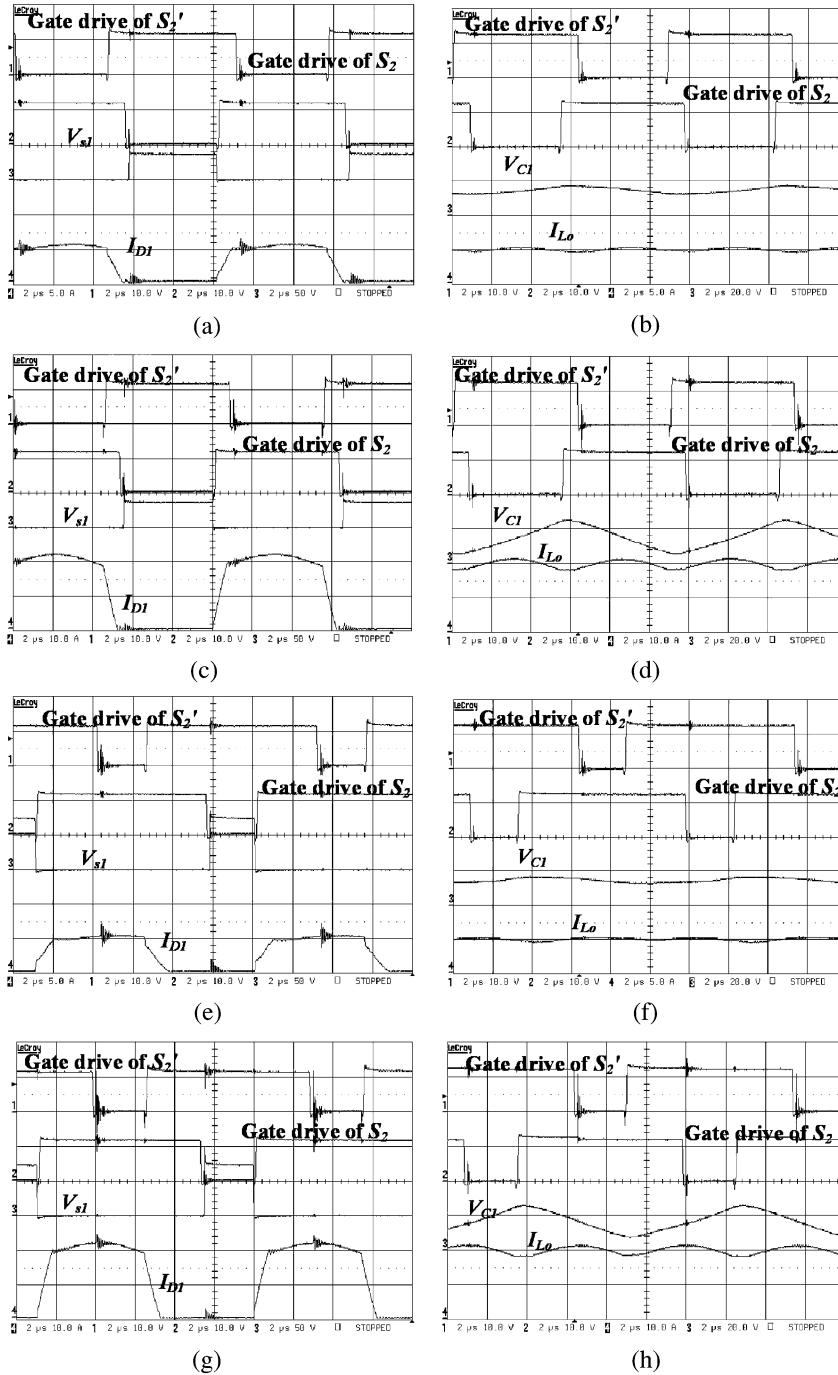
Fig. 7.   Measured waveforms of $V_{s1}, V_{C1}, I_{D1}, I_{Lo}$, and gate drive signals of S_2 and S_2' for different input and output conditions.

TABLE I
SUMMARY OF COMPARISON OF MEASURED AND CALCULATED RESULTS

Parameters	Measured and Calculated Values			
Measured output current I_o	5 A	20 A	5 A	20 A
Measured output voltage V_o	5.08 V	5.08 V	5.08 V	5.08 V
Measured input voltage V_{in}	36.8 V	36.6 V	72.0 V	71.8 V
Measured commutation time T_c	803 ns	740 ns	960 ns	789 ns
Calculated T_c from (8)	764.3 ns	743.3 ns	1030 ns	797.8 ns
Calculated T_c from (10)	736.8 ns	736.8 ns	736.8 ns	736.8 ns
Measured peak-to-peak output current ΔI_o	0.57 A	3.1 A	0.52 A	3.1 A
Calculated ΔI_o from (8) and (13)	0.675 A	2.727 A	0.593 A	2.658 A
Calculated ΔI_o from (10) and (13)	0.684 A	2.736 A	0.684 A	2.736 A

The conversion efficiencies of the prototype measured at the nominal input of 48 V dc are 93.12%, 93.056% and 90.33% at output current of 5, 10, and 20 A, respectively. The output ripple waveform (with noise) is shown in Fig. 8. With a small filter, the measured peak-to-peak output voltage ripple is 6.6 mV. Taking into account the high frequency voltage spike, the measured peak-to-peak ripple is 28.4 mV. Finally, Fig. 9 shows the zero-voltage turnon waveform of S_2 with the drain voltage fallen to zero before the gate drive signal takes on.

VI. CONCLUSION

A new dc–dc converter using a dual asymmetric half-bridge topology has been proposed for achieving very low output ripple
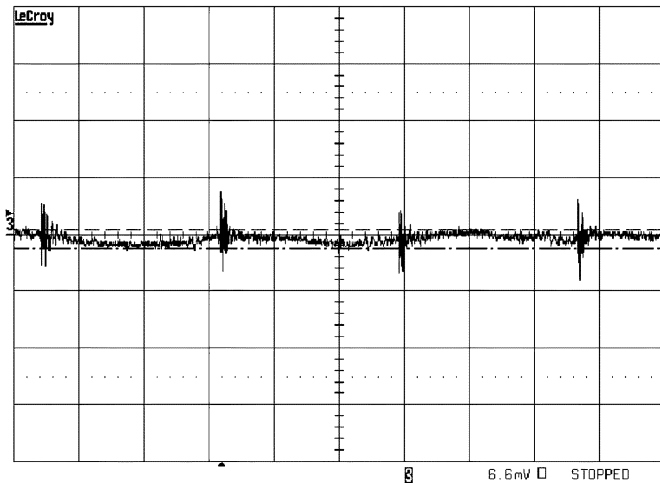
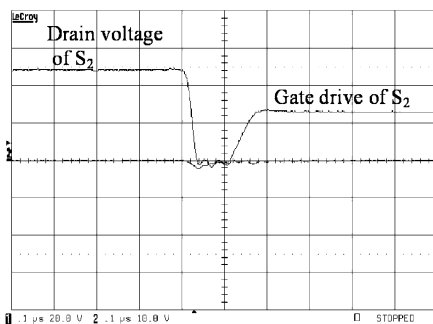Fig. 8. Measured output ripple voltage for $V_{in} = 48$ V and $I_o = 20$ A. Vertical scale: 20 mV/div.

Fig. 9. Verification of zero-voltage switching of S_2.

voltage. The proposed converter requires a very small output filter that improves the conversion efficiency. High efficiency is maintained as a result of zero-current turnoff of the output rectifiers especially when synchronous rectifiers are used. The symmetric structure of the proposed converter also guarantees equal current sharing of the two rectifiers, thereby maximizing their utilization. Experimental results show that the output ripple current is reduced 9 times in the worst case when compared with a two-phase isolated interleaved converter, and about 13.12 times when compared with a single-ended forward converter operating with the same output filter and at the same switching frequency. The measured results are consistent with the analytical equations. The low output-ripple converter topology described in this paper has been granted a U.S. patent [14].

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