Improved Electrical Properties of Ge p-MOSFET With HfO_2 Gate Dielectric by Using TaO_xN_y Interlayer

J. P. Xu, X. F. Zhang, C. X. Li, P. T. Lai, and C. L. Chan

***Abstract*—The electrical characteristics of germanium p-metal–oxide–semiconductor (p-MOS) capacitor and p-MOS field-effect transistor (FET) with a stack gate dielectric of HfO_2/TaO_xN_y are investigated. Experimental results show that MOS devices exhibit much lower gate leakage current than MOS devices with only HfO_2 as gate dielectric, good interface properties, good transistor characteristics, and about 1.7-fold hole-mobility enhancement as compared with conventional Si p-MOSFETs. These demonstrate that forming an ultrathin passivation layer of TaO_xN_y on germanium surface prior to deposition of high-k dielectrics can effectively suppress the growth of unstable GeO_x, thus reducing interface states and increasing carrier mobility in the inversion channel of Ge-based transistors.**

***Index Terms*—Germanium, high-k, pMOSFET, TaON interlayer.**

I. Introduction

With THE continual scaling down of the dimensions of metal–oxide–semiconductor field-effect transistor (MOSFET), high-k metal–oxide dielectrics, e.g., HfO_2 and ZrO_2, are used to replace SiO_2 as gate dielectric to reduce gate leakage, and also, high-mobility semiconductor such as germanium is used as channel material to increase the operating speed of the devices. High-quality insulator/channel interface is desirable for high-k/Ge MOS devices [1]–[4]. Kim *et al.* [5] reported that an ultrathin nitride interlayer (AlN: $k \sim 9$ and Hf_3N_4: $k \sim 20$) inserted between HfO_2 and germanium substrate could effectively passivate the Ge surface and increase the k value of the stacked gate dielectric as compared to the case with GeO_xN_y as interlayer. Sugawara *et al.* [6] demonstrated that Ge MOS capacitor with ALD HfO_2 and plasma-synthesized TaON interlayer showed superior electrical properties. Since TaO_xN_y has a high k value of ~26 [7], [8] and high thermal stability, it should be a promising candidate as an interlayer between high-k dielectric and Ge substrate. In this letter, Ge-based MOS capacitors and MOSFETs with $Al/HfO_2/TaO_xN_y$ stack gate are fabricated. Measurements show that, owing to the passivation role of the TaO_xN_y interlayer, excellent electrical properties with low gate leakage current, low interface-state density, good output characteristics, and high hole mobility can be obtained for the HfO_2/TaO_xN_y gate-dielectric p-MOSFET when compared with its counterpart without the passivation layer.

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II. Experiments

Ring-structure p-MOSFETs were fabricated on n-type (100) Ge wafers (0.1–0.2 $\Omega \cdot$ cm) from Umicore, using a self-aligned technology. Before depositing the gate dielectric, Ge wafers were cleaned using semiconductor-grade trichloroethylene, acetone, and ethanol for 5 min, respectively, and rinsed with DI water several times, followed by 15-s diluted HF (1 : 50) dipping and 15-s DI water rinsing for five cycles to remove Ge native oxide. The rms surface roughness of the Ge wafers after cleaning was 0.14–0.15 nm for a 5-μm^2 area, which was measured by AFM. After drying in N_2, the wafers were immediately transferred into the Denton Vacuum Discovery Deposition System. TaN_x of 1.0 nm was deposited by reactive sputtering of Ta in an Ar/N_2 (12 : 18) ambient, followed by the deposition of a nominal 9.0-nm HfO_2 by reactive sputtering of Hf in an Ar/O_2 (24 : 6) ambient. For comparison, a nominal 9.0-nm HfO_2 was directly deposited on the cleaned Ge substrate without the TaN_x layer to make the control sample. A postdeposition annealing (PDA) was carried out in wet N_2 at 500 °C for 5 min to improve the dielectric quality, transform TaN_x into TaO_xN_y [9], and also suppress the formation of unstable GeO_x [10]. The wet N_2 atmosphere was realized by bubbling pure N_2 through DI water at 95 °C with a flow rate of 500 mL/min. Subsequently, Al was e-beam evaporated, and ring gate electrode with inner and outer radii of 45 and 145 μm (so, the gate length = 100 μm) was patterned using optical lithography and etched in diluted H_3PO_4. Then, the samples were divided into the following two groups: one for fabrication of capacitors, and another for preparation of p-MOSFETs. For the p-MOSFETs, source/drain regions were formed by accurately timing the etching of the high-k dielectric in a CF_4-based plasma, followed by a self-aligned BF_2^+ implantation at 20 keV with a dose of 4×10^{15} cm^{-2}. Source/drain electrodes were formed by e-beam evaporation of Al through a lift-off process. Finally, dopant activation and forming-gas annealing were simultaneously completed in H_2/N_2 (5% H_2) for 20 min

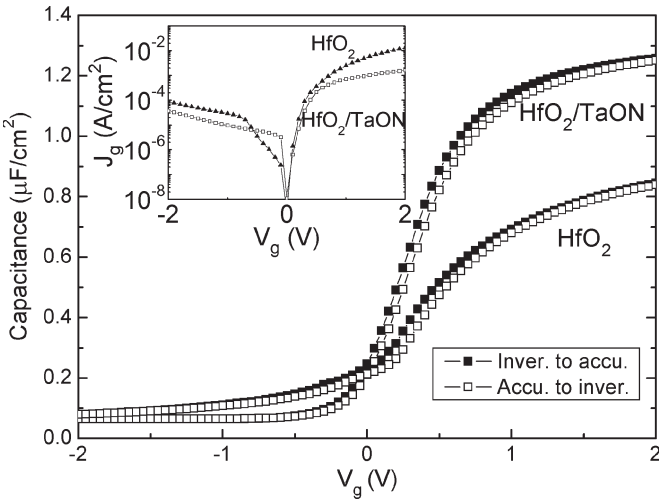

Fig. 1. Normalized HF C–V curves of the HfO_2/Ge and $HfO_2/TaO_xN_y/Ge$ MOS capacitors, with nominal HfO_2 thickness of 9.0 nm and nominal TaO_xN_y thickness of 1.0 nm. The inset is their gate leakage current density.

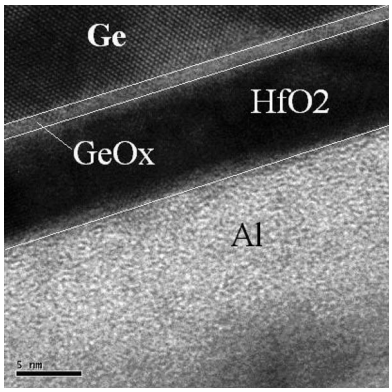

Fig. 2. TEM photograph of the HfO_2/Ge MOS sample after PDA, showing the formation of an unstable GeO_x interlayer.

at a low temperature of 400 °C to suppress Al diffusion into the gate dielectrics.

III. Results and Discussion

Fig. 1 shows the typical HF (1-MHz) C–V curves of the HfO_2/Ge (denoted as nonpassivated sample) and $HfO_2/TaO_xN_y/Ge$ (denoted as passivated sample) MOS capacitors. The total physical thicknesses of their dielectrics are 10.0 and 10.4 nm, respectively, measured by multiwavelength ellipsometer, in which the Cauchy model and light wavelengths ranging from 400 to 1000 nm with incidence angles of 65°, 70°, and 75° were used to obtain the film thickness. A 2.0–2.2-nm GeO_x interlayer, formed between the high-k dielectric and substrate, is estimated from the TEM photograph of the nonpassivated sample shown in Fig. 2. For the passivated sample, a 0.4-nm increase in dielectric thickness after PDA should be ascribed to the conversion of the TaN_x layer to a TaO_xN_y passivation layer. Although the nonpassivated sample physically has a thinner gate dielectric than the passivated one, it has a larger capacitance equivalent thickness extracted from the accumulation capacitance (C_{ox}) in Fig. 1 than the latter (3.9 versus 2.6 nm) due to the lower k value of its GeO_x interlayer. A small distortion occurs in the weak inversion region of the C–V curve for the nonpassivated sample, indicating that there exists a large amount of interface states. This is supported by the D_{it} distribution in bandgap, as shown in Fig. 3. The inset in Fig. 1 shows the leakage current density of the two MOS capacitors. The leakage current density of the nonpassivated sample at $V_g = V_{fb} + 1$ V is about one order of magnitude larger than that of the passivated sample, which should be related to the growth of a GeO_x interlayer leading to a large D_{it} and, thus, larger interface-trap-assisted tunneling current [11] (the $HfO_2/TaO_xN_y/Ge$ sample in [6] has smaller leakage current mainly because HfO_2 prepared by ALD has better dielectric quality, hence having smaller D_{it} and Q_{ox}). Thus, an ultrathin TaO_xN_y interlayer inserted between the high-k dielectric and Ge substrate can effectively suppress the formation of unstable GeO_x, leading to improved interface properties for MOS devices. Fig. 3 shows the frequency dependence of C–V curves measured at frequencies ranging from 1 to 800 kHz, and the interface-state distribution in the bandgap of germanium. The normal conductance method [12] was used to extract D_{it}'s just for the purpose of a relative comparison between the samples, although it has been shown to produce numerically inaccurate results for germanium [13]–[16]. The D_{it} near the midgap for the passivated sample is $5 \times 10^{11} - 1 \times 10^{12}$ $eV^{-1} \cdot cm^{-2}$, which is much smaller than that for the nonpassivated sample ($3.2 \times 10^{12} - 4.6 \times 10^{12}$ $eV^{-1} \cdot cm^{-2}$).

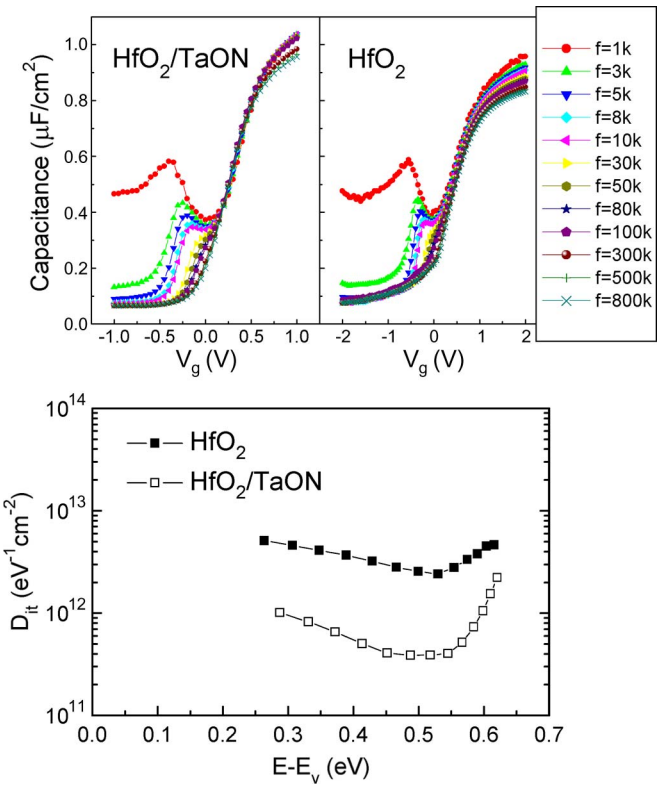

Fig. 3. Frequency dependence of C–V curves, measured at frequencies ranging from 1 to 800 kHz, and the interface-state distribution in the bandgap of germanium extracted by the conductance method.

The output characteristics of the p-MOSFETs are shown in Fig. 4. The HfO_2/TaO_xN_y gate-dielectric p-MOSFET shows a larger I_d than that of the HfO_2 gate-dielectric p-MOSFET. This should be attributed to the larger oxide capacitance (see Fig. 1)

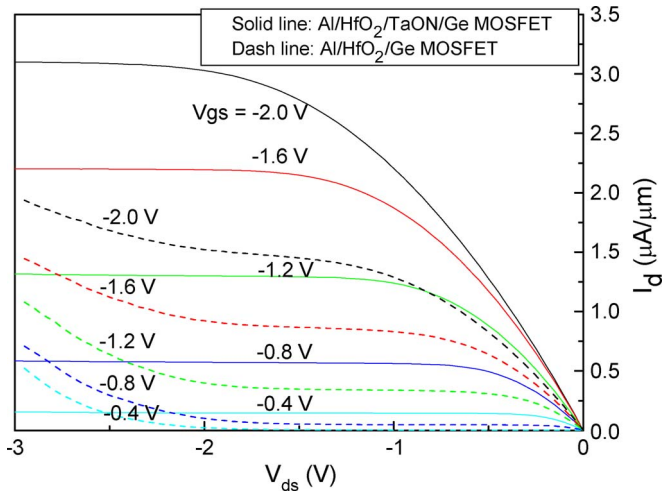

Fig. 4. Output characteristics of the HfO_2/TaON/Ge and HfO_2/Ge p-MOSFETs ($W_{\rm eff}/L = 537\ \mu$m/100 μm), with nominal HfO_2 thickness of 9.0 nm and nominal TaO_xN_y thickness of 1.0 nm.

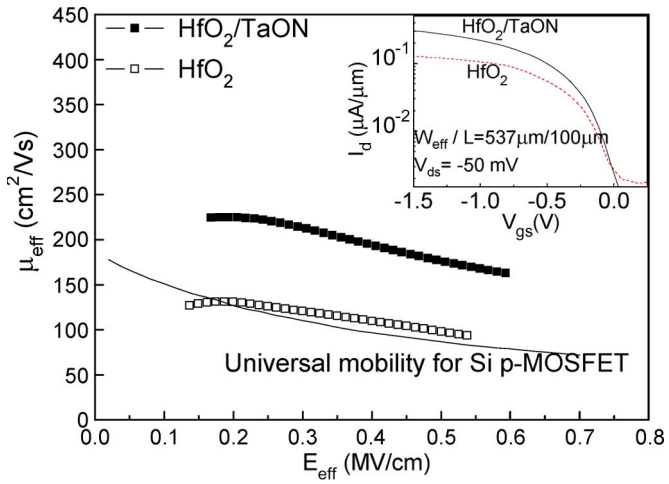

Fig. 5. Effective hole mobility of the two Ge p-MOSFETs and (solid line) the universal hole mobility for conventional Si p-MOSFETs. The inset is their transfer characteristics.

and higher carrier mobility (see hereafter) of the former device. The nonsaturated I_d characteristics of the HfO_2 gate-dielectric p-MOSFET at large $|V_{\rm ds}|$ (> 2 V) are probably related to gate-perimeter leakage current caused by the difference in the etching characteristics between the GeO_x and TaO_xN_y interlayers during the RIE process.

The effective carrier mobility ($\mu_{\rm eff}$) of the two samples was extracted from the linear region of the I_d–$V_{\rm gs}$ curves of the MOSFET with a gate length of 100 μm, which is shown as an inset of Fig. 5. From the $I_d-V_{\rm gs}$ formula, $\mu_{\rm eff}$ can be written as [17]

$$\mu_{\rm eff} = \frac{I_d}{(W_{\rm eff}/L)C_{\rm ox}(V_{\rm gs}-V_{\rm th})V_{\rm ds}}$$

and effective field ($E_{\rm eff}$) is expressed as [18]

$$E_{\rm eff} = \frac{Q_{\rm dep}+\eta Q_{\rm inv}}{\varepsilon_s} \approx \frac{C_{\rm ox}\left[V_{\rm gs}-(1-\eta)(V_{\rm gs}-V_{\rm th})\right]}{\varepsilon_s}$$

where $Q_{\rm inv} \approx C_{\rm ox}(V_{\rm gs}-V_{\rm th})$, $Q_{\rm dep} = E_{\rm ox}\varepsilon_{\rm ox} - Q_{\rm inv}$, $E_{\rm ox} \approx V_{\rm gs}/t_{\rm ox} = V_{\rm gs}C_{\rm ox}/\varepsilon_{\rm ox}$, ε_s is the permittivity of Ge substrate, and $\eta = 0.3$ is the fitting parameter [17], [18]. The effective channel width $W_{\rm eff}$ is calculated to be 537 μm [18]. For comparison, the universal hole-mobility curve for conventional Si p-MOSFETs is also shown in Fig. 5. At low effective field, the $\mu_{\rm eff}$ of the HfO_2/TaO_xN_y/Ge MOSFET exhibits $\sim$1.7-fold enhancement when compared with the hole mobility of conventional Si p-MOSFETs. A peak mobility of 225 $\rm cm^2/V\cdot s$ at 0.2 MV/cm is observed in Fig. 5. On the other hand, the effective hole mobility of the HfO_2/Ge MOSFET is seriously degraded when compared with that of the HfO_2/TaO_xN_y/Ge sample. This should be mainly attributed to enhanced hole scattering arising from more interface states (see larger $D_{\rm it}$ in Fig. 3, larger oxide leakage in Fig. 1, and larger subthreshold swing in Fig. 5) and possibly larger interface roughness associated with growth of the unstable GeO_x interlayer (see Fig. 2). Thus, it can be suggested that the ultrathin TaO_xN_y interlayer between the high-k dielectric and Ge substrate can effectively improve the interface quality (lower interface-state density) and thus significantly enhance the carrier mobility (roughly 1.7 times). In addition, from the I_d–$V_{\rm gs}$ curve, the threshold voltage ($V_{\rm th}$) and subthreshold swing are extracted to be -0.120 V and 114 mV/decade for the HfO_2/TaON gate-dielectric p-MOSFET, and -0.098 V and 157 mV/decade for the HfO_2 gate-dielectric p-MOSFET, respectively. The small negative $V_{\rm th}$ value, particularly for the nonpassivated sample, is due to the high negative-oxide-charge densities ($Q_{\rm ox}$)'s extracted from the HF C–V in Fig. 1, which are -9.7×10^{11} and -2.1×10^{12} $\rm cm^{-2}$ for the HfO_2/TaO_xN_y/Ge and HfO_2/Ge capacitors, respectively. The smaller subthreshold swing of the HfO_2/TaON p-MOSFET shows better interface quality, which is consistent with the results in Fig. 3(b). A possible origin of the negative oxide charges is the wet ambient of the PDA, which can introduce hydroxyl ions in the gate dielectric [10]. It is expected that further improvements in the electrical properties of the devices can be obtained if the device structure and processing conditions are optimized, e.g., higher activation temperature or longer activation time for the source/drain implant to activate more dopants, and rectangular gate (smaller than the ring gate) resulting in smaller transistor, thus having smaller gate leakage current and smaller S/D leakage current.

IV. Summary

Germanium-based p-MOS capacitors and p-MOSFETs with high-k materials as gate dielectric were fabricated. The MOS devices with HfO_2/TaO_xN_y stack gate dielectric demonstrate excellent electrical properties, such as low interface-state density, small gate leakage current, and good output and transfer characteristics when compared with the control samples with HfO_2 gate dielectric, and also an $\sim$1.7-fold hole-mobility enhancement relative to the universal hole mobility of Si p-MOSFET. All these are due to the ultrathin TaO_xN_y interlayer, which can effectively passivate the dielectric/germanium interface. Therefore, HfO_2/TaO_xN_y stack gate dielectric should be a promising high-k gate dielectric structure for fabricating high-speed Ge-based MOSFETs in the future.

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