Off-State Gate Leakage Current in N-Channel MOSFET's with Gate Dielectrics Prepared by Different Techniques.

Zeng Xu, P. T. Lai, and W. T. Ng[+]

Department of Electrical and Electronic Engineering, University of Hong Kong.
[+]Department of Electrical and Computer Engineering, University of Toronto, Canada.

I. Introduction

Drain corner-field induced band-to-band (B-B) tunneling in thin-oxide MOSFET's has been identified as a fundamental limit in MOS device scaling [1]-[3]. The LDD structure provides a simple solution to this drain leakage problem [2], [3]. Under the same bias condition, gate current (I_g) is also observed for a wide range of oxide thickness. This charge transport through oxide in the gate-drain overlap region plays an essential role in electrical erase for a class of non-volatile memories commonly known as "flash EEPROM's" [4]-[6]. However, it also raises the issue of device degradation and gate oxide breakdown because it can lead to charge trapping in the oxide. The origin of this off-state gate current in SiO_2-gate n-channel MOSFET's , which occurs at high drain voltages, has been attributed to Fowler-Nordheim (F-N) tunneling of electrons from the gate for SiO_2 thinner than 100Å, and to hot-hole injection from the drain for thicker SiO_2 [3], [7]. For NH_3-nitrided gate oxide (NO) prepared by rapid thermal nitridation (RTP), a significant I_g at drain voltages as low as 4V and I_g injection efficiency as high as 0.8 were reported in the n-channel MOSFET's [8]. On the other hand, an N_2O-based nitridation technology has been extensively studied recently as a more promising alternative to NH_3 nitridation because of its simpler processing and absence of detrimental H-related species in the nitridation ambient [9]-[12]. Nevertheless, the off-state I_g characteristics in MOSFET's with N_2O-based oxides as gate dielectrics has not yet been reported in literature. This work studied the characteristics of off-state I_g in n-channel MOSFET's with thin N_2O-based gate dielectrics. N-MOSFET's using conventional thermal oxide (OX) and reoxidized NH_3-nitrided oxide (RONO) were also investigated for the purpose of comparison.

II. Experimental

The n-MOSFET's used in this study were fabricated on p-type (100)-oriented Si wafer (6~8 Ω-cm) using conventional n^+ polysilicon-gate technology. The channel doping (~$2 \cdot 10^{17}$ cm^{-3}) was controlled by boron implant through a sacrificial oxide which was stripped after the implant, followed by gate dielectrics formation as described in Table 1. All gate oxides were finally annealed in N_2 at 950°C for 25 min. The final thickness of all gate dielectrics was around 140Å as measured by CV technique. No passivation film was used. Since off-state leakage is independent of channel length, devices with larger dimensions (L/W=20 μm/20 μm) were adopted in this work to prevent possible punchthrough during measurement and minimize fringe effect.

Table 1. Preparation sequences of gate oxides employed in this study

samples	oxidation	nitridation	reoxidation
OX	O_2 , 850°C, 70min	-------	-------
RONO	O_2 , 850°C, 60min	NH_3 , 950°C, 35min	O_2 , 950°C, 30min
N2ON	O_2 , 850°C, 60min	N_2O, 950°C, 10min	-------
N2OG	N_2O, 950°C, 120min	-------	-------

III. Off-state gate leakage characteristics and discussion

Fig. 1 shows the gate current (I_g) characteristics of n-MOSFETs with OX, N2ON and RONO, N2OG gate dielectrics. In the V_d region (5V~10V), where the drain leakage is dominated by B-B tunneling in drain corner, a V_d-exponentially dependent I_g was observed in RONO and N2OG devices, as shown in Fig.1. In contrast, no detectable I_g was found in this V_d region for OX and N2ON devices. I_g only appeared in the high V_d region (>11V), where avalanche effect occurs in drain junction. F-N tunneling of electrons from n^+ poly-gate cannot account for this low-field I_g, because the slopes of F-N plot for RONO and N2OG devices in low field region, depicted in Fig.2, are much smaller than normal values (~10 A/cm•V), which would yield physically unreasonable low barrier height. While studies performed on MOS capacitors have indicated that the barrier height for e-injection in N_2O-grown oxides is similar to that in pure SiO_2 [12]. Mechanism of hot-hole injection from the drain to the gate, proposed in [8], also cannot be responsible for the observed low-field I_g, even if the nitridation-induced barrier height lowering effect is taken into account. We measured the off-state drain and gate leakage current on N2OG device under four different substrate bias. The results are given in Fig. 3. It can be clearly seen that although drain leakage is strongly affected by the avalanche effect in the drain-substrate junction, indicating hole trapping in gate oxide, the corresponding I_g remains unchanged for all V_{sub} bias, suggesting that I_g cannot be attributed to hot-hole injection. Similar results were also observed in RONO devices (not shown here). The model of shallow-trap-assisted tunneling of electrons from the gate [14] can readily explain the low-field I_g observed in RONO and N2OG devices. This argument is supported below by the channel hot-carrier stress experiments. Presented in Fig. 4 is the measured I_g after different stress times of channel hot-electron injection. I_g decreased monotonicly as the e^--injection and trapping proceeded because electron traps are filled by the injected electrons. This behaviour is contrary to the hot-hole injection model, since e^--trapping should lead to increasing I_g due to electric field enhancement in the drain junction. Experiment of hot-hole injection effect on I_g, shown in Fig. 5, further confirms the trap-assisted tunneling mechanism. Off-state I_g remains unchanged during the whole hot-hole injection stress since the gate current conduction is not related to the holes but electrons only.

IV. Summary

Off-state gate current of n-channel MOSFET's with OX, RONO, N2ON, and N2OG oxides as gate dielectrics was investigated in this work. It is revealed that gate current conduction mechanism in low field region is very different for these oxides. Enhanced conductivity is observed in RONO and N2OG oxides, which is attributed to the trap-assisted tunneling mechanism. Therefore, in view of gate leakage, the method of nitridizing pre-grown thermal oxide is more

feasible than directly growing oxide in N_2O ambient, especially in leakage sensitive applications, such as very-low-power battery-based circuits, DRAM cells, etc..

References

[1] C. Chang and J. Lien, "Cornor-field induced drain leakage in thin oxide MOSFETs," in *IEDM Tech. Dig.*, 1987, pp.714-717.

[2] T. Y. Chan, J. Chen, P. K. Ko, and C. Hu, "The impact of gate-induced drain leakage current on MOSFET scaling," in *IEDM Tech. Dig.*, 1987, pp.718-721.

[3] C. Chang, S. Haddad, B. Swaminathan, and J. Lien, "Drain-avalanche and hole-trapping induced gate leakage in thin-oxide MOS devices," *IEEE Electron Device Lett.*, vol.9, no.11, pp.588-590, 1988.

[4] G. Samachisa et al., "A 128K flash EEPROM using double-polysilicon technology," *IEEE J. Solid-State Circuits*, vol. SC-22, no.5, p.676, 1987.

[5] H. Kume et al., "A flash-erase EEPROM cell with an asymmetric source and drain structure," in *IEDM Tech. Dig.*, 1987, pp.560-563.

[6] G. Verma and N. Mielke, "Reliability performance of ETOX based flash memories," in *26th Proc. IEEE Reliability Phys. Symp.*, Apr. 1988, p.158.

[7] J. Chen, T. Y. Chan, P. K. Ko, and C. Hu, "Gate current in off-state MOSFET," *IEEE Electron Device Lett.*, vol.10, no.5, pp.203-205, 1989.

[8] A. T. Wu, S. H. Lee, V. Murali, and M. Garner, "Off-state gate current in n-channel MOSFET's with nitrided oxide gate dielectrics," *IEEE Electron Device Lett.*, vol.11, no.11, pp.499-501, 1990.

[9] A. Uchiyama, H. Fukuda, T. Hayashi, T. Iwabuchi, and S. Ohno,"High-performance dual-gate sub-halfmicron CMOSFETs with 6-nm-thick nitrided SiO_2 films in an N_2O ambient," in *IEDM Tech. Dig.*, 1990, pp.425-428.

[10] H. Hwang, W. Ting, D-L. Kwong and J. Lee, "Electrical and reliability characteristics of ultrathin oxynitride gate dielectric prepared by rapid thermal processing in N_2O," in *IEDM Tech. Dig.*, 1990, pp.421-424.

[11] Z. H. Liu, H. J. Wann, P. K. Ko, C. Hu, and Y. C. Cheng, "Effects of N_2O anneal and reoxidation on thermal oxide characteristics," *IEEE Electron Device Lett.*, vol.13, pp.402-405, 1992.

[12] A. B. Joshl, G. Yoon, J. Kim, G. Q. Lo, and D-L. Kwong, "High-Field Breakdown in Thin Oxides Grown in N_2O Ambient," *IEEE Trans. Electron Devices*, vol.40, no.8, pp.1437-1444, 1993.

[13] A. Ditali, V. Mathews, and P. Fazan, "Hot-carrier-induced degradation of gate dielectrics grown in nitrous oxide under accelerated aging," *IEEE Electron Device Lett.*, vol.13, no.10, pp.538-540, 1992.

[14] H. Wong and Y. C. Cheng, "Electronic conduction mechanisms in thin oxynitride films," J. Appl. Phys. vol.70(2), p.1078, 1991.

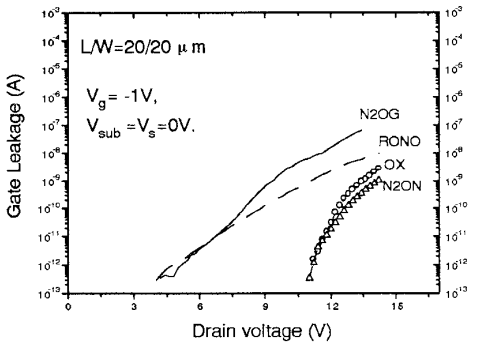

Fig. 1. Gate leakage current for N2OG (full line), RONO (dashed line), OX (circles), and N2ON (up triangles) devices.

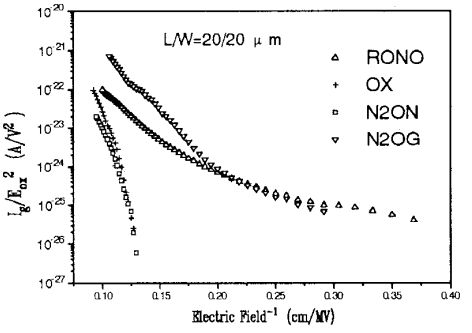

Fig. 2. F-N plot for gate current of the n-MOSFETs with OX, RONO, N2ON and N2OG gate dielectrics.

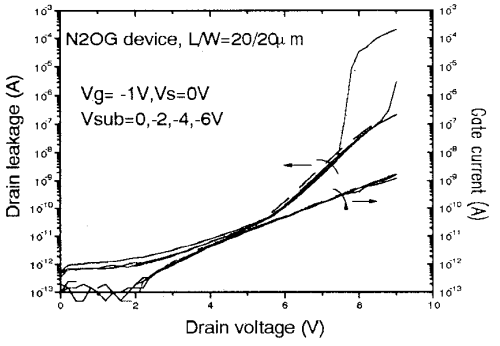

Fig. 3. Drain and gate leakage current at V_{sub}=0, -2, -4, -6V (from right to left).

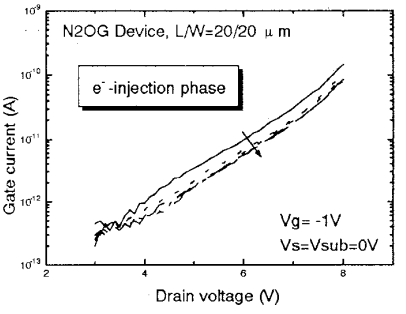

Fig. 4. Off-state gate current measured at stress time=0, 50, 400, 2200, and 4000s (in the arrow direction). Hot-electron stress condition: V_g=7.5V, V_d=7V, V_s=V_{sub}=0V.

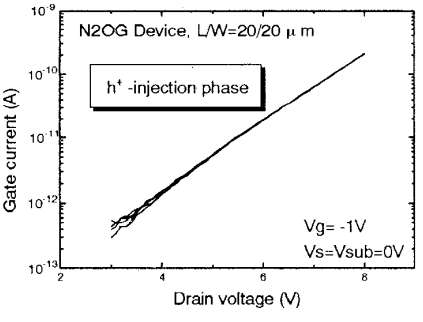

Fig. 5. Off-state gate current measured at stress time=0, 50, 400, 2200, and 4000s. Hot-hole stress condition: V_g=0.7V, V_d=7V, V_s=V_{sub}=0V.