Improved Performance for OTFT with $HfTiO_2$ as gate dielectric by N_2O annealing

W.M. Tang, K.H. Cheng, C.H. Leung, P.T. Lai, J.P. Xu and C.M. Che

Abstract - OTFTs with $HfTiO_2$ as gate dielectric have been successfully fabricated. The devices show small threshold voltage and subthreshold slope, and thus are suitable for low-voltage and low-power applications. This work also finds that OTFT with gate dielectric annealed in N_2O has larger dielectric constant, smaller threshold voltage, smaller subthreshold slope and larger on/off ratio than the N_2-annealed sample. This demonstrates that the N_2O annealing is an important surface treatment for preparing a high-quality insulator/organic interface.

I. INTRODUCTION

Organic thin-film transistors (OTFTs) have attracted a great deal of interest in recent years in the field of microelectronics and optoelectronics. They can be used to make sensors [1], flat-panel displays, low-end smart cards and electronic identification tags [2]. OTFTs based on polymers have several advantages and become a promising alternative to silicon-based transistors for many applications. They are particularly suitable for large-area and flexible electronics applications because organic semiconductors are strong, soluble and flexible. They can be deposited by spray coating and screen-printing, which are simple to process and can cover a large area. In addition, these processes can be done at low-temperature to minimize the production cost. Several organic semiconductors have been used to make OTFTs, such as pentacene, rubrene, perylene, poly(3-hexylthiophene) regioregular (P3HT) and dihexylquin-quethiophene (DH-5T). Among these organic materials, pentacene is commonly chosen as the active layer for making OTFT. It is because pentacene has a strong tendency to form molecular crystals and well-ordered film by evaporation which is an important factor for obtaining high carrier mobility [3, 4]. Moreover, pentacene is a p-type semiconductor, which is stable in air and less sensitive to moisture.

Silicon dioxide (SiO_2) and oxynitride have been traditionally used as the gate insulator in OTFT. They can be easily fabricated by conventional thermal oxidation and patterned by photolithography. However, these kinds of insulators are not very suitable for making high-performance OTFTs for high-speed and low-power display driving circuits. The required insulator must be very thin in order to get high gate capacitance but scaling down the thickness of silicon dioxide creates a lot of problems such as high leakage current, intermixing of materials at the interfaces and direct tunneling in the thin film. In order to solve these problems, insulator with high dielectric constant (k) should be used. High-k materials can allow thicker physical thickness to suppress gate leakage current while maintaining a high gate capacitance to reduce the operating voltage of OTFT. Several high-k dielectrics have been employed to fabricate OTFT, for example HfO_2 [5], Al_2O_3 [6], TiO_2 [7], Ta_2O_5 [8] and $BaTiO_3$ [9]. In this study, high-k dielectric material hafnium titanium oxide ($HfTiO_2$) is used as the gate insulator. The purpose of adding Ti into HfO_2 is to get higher dielectric constant while maintaining good thermal stability with Si [10]. As the interface between the organic layer and the gate insulator can greatly influence the performance of OTFT,

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the high-k dielectric is annealed in nitrous oxide (N_2O) in order to improve its surface quality. The electrical characteristics of the devices are measured, and then used to calculate the carrier mobility, threshold voltage, sub-threshold slope and on-off ratio of the devices.

II. EXPERIMENTS

N-type <100> Si wafers (resistivity of 0.2 - 0.5 Ωcm) were used in this study. The wafers were cleaned using the conventional RCA method followed by a 60-sec dip in 5% hydrofluoric acid to remove the native oxide. The wafers were then loaded into a Denton vacuum LLC Discovery 635 sputterer, which was then pumped down to 2 x 10^{-6} Torr. $HfTiO_2$ was then deposited at room temperature by co-sputtering of hafnium metal (99.99 % purity) with a RF power of 25 W and titanium metal (99.995 % purity) with a DC current of 0.1 A in a mixed Ar/O_2 ambient (Ar to O_2 ratio = 8:1). One sample then underwent an annealing in a furnace at 700 °C in N_2O for 10 min. For the purpose of comparison, a control sample with N_2-annealed $HfTiO_2$ as gate dielectric was also fabricated. In order to use the substrate as the gate of the device, the back oxide was removed by using 20 % HF. A layer of 30-nm pentacene was then deposited onto the insulator by vacuum evaporation at 10^{-6} Torr. The pentacene was purchased from Aldrich and used without further purification. The source and drain gold pads were then deposited on top of the organic layer by evaporation through a stainless steel mask with a channel length L of 30 μm and a channel width W of 200 μm. The structure of the high-k OTFT fabricated is shown in Fig. 1. In order to deduce the dielectric constant, capacitor structures were also fabricated by evaporation of Al onto the dielectric films. The area of capacitors was 7.85×10^{-5} cm^2. The capacitance-voltage (C-V) characteristics were measured by a HP4284A LCR meter and a HP4140B pA meter at 100 kHz. The current-voltage (I-V) characteristics were measured by a HP4156B semiconductor parameter analyzer. All measurements were conducted in a dark environment at room temperature. The final thickness of the oxide layers t_{ox} was measured by an ellipsometer.

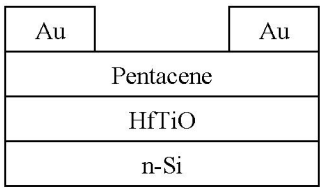

Fig. 1 Structure of high-k OTFT

III. RESULTS AND DISCUSSION

Fig. 2(a) and (b) show the drain current I_d versus drain voltage V_d characteristics of the OTFTs with insulator annealed in N_2 and N_2O respectively. The operating principle of OTFT is similar to that of traditional MOSFET. OTFT with a p-type organic semiconductor (e.g. pentacene) as an active layer is called p-type OTFT. When a negative gate voltage V_g is appl-

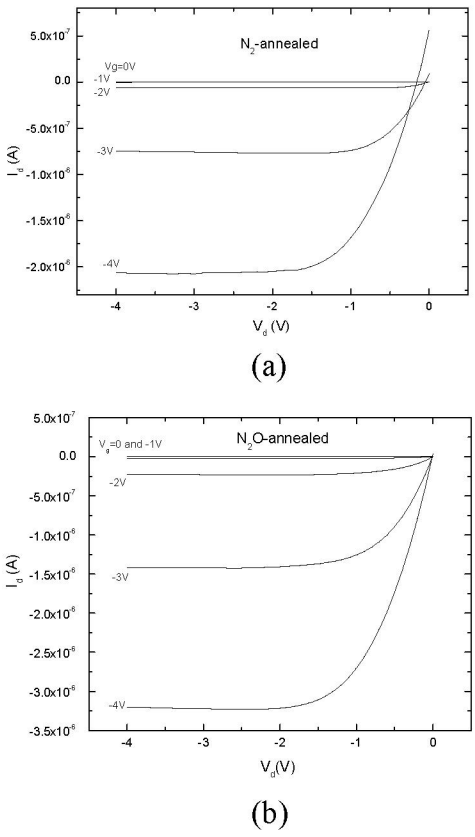

Fig. 2 I_d vs V_d characteristics for the OTFT with gate dielectric annealed in (a) N_2 (b) N_2O

applied to the p-type OTFT, positive charges or holes will accumulate at the insulator/organic interface. A conductive channel will be formed and the transistor is in the on state when the applied negative gate voltage is large enough to accumulate sufficient amount of holes in the channel. The voltage required to turn on an OTFT is called the threshold voltage V_t. Current will flow through the channel from source to drain when a negative drain voltage is applied to the device. The drain current I_d in the linear and saturation regions can be given by equations (1) and (2) respectively

$$I_d = \frac{W}{L}\mu C_o(V_g - V_t - \frac{V_d}{2})V_d \qquad (1)$$

$$I_d = \frac{W}{2L}\mu C_o(V_g - V_t)^2 \qquad (2)$$

where C_o is the capacitance per unit area of the insulator, and μ is the carrier mobility. Presented in Fig. 3 is the logarithmic plot of I_d versus V_g for the N_2 and N_2O-annealed samples. The subthreshold slope (S) is a very important parameter for OTFTs used as switches because it shows the voltage needed to separate the on and off modes of the switch. The S parameter is defined as $\frac{\partial V_g}{\partial \log_{10}(I_d)}$ which can be calculated by taking the reciprocal of the steepest slope of the plot.

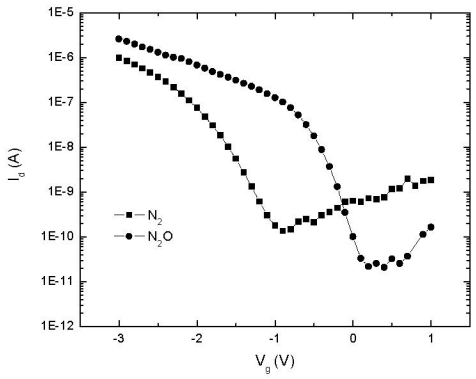

Fig. 3 I_d vs V_g characteristics for the N_2-annealed and N_2O-annealed samples

The important parameters of the samples are summarized in Table 1. The N_2O-annealed sample has higher dielectric constant and hence smaller threshold voltage than the N_2-annealed sample. It is because during the N_2O annealing, atomic N is decomposed from this nitridation gas and then diffuses into the oxide film. These N atoms can hinder the diffusion of O into the oxide, thus suppressing the formation of a low-k SiO_2 interlayer between the high-k dielectric and the substrate. The incorporation of nitrogen in the insulator can also passivate the insulator surface by forming strong triple bonds with the dangling bonds of silicon. These strong Si ≡ N bonds can improve the interfacial diffusion barrier, decrease the interfacial strain and remove fixed oxide charges. N_2O nitridation can also reduce the traps and defects inside the oxide layer. Hence, the N_2O-annealed samples show significant reduction in gate leakage current and great improvement in on/off or I_g/I_d ratio. The subthreshold slope is also improved by the N_2O annealing.

	Annealing gas	
	N_2	**N_2O**
C_o (μF/cm^2)	0.531	0.599
t_{ox} (nm)	18.9	18.1
k	11.3	12.2
μ (cm^2/Vs)	0.24	0.22
V_t (V)	-1.73	-1.28
S (V/decade)	0.27	0.25
on/off ratio (10^4)	7.1	17.5
I_d (μA) (at $V_g = V_d = -4V$)	2.33	4.58
I_g (μA) (at $V_g = -4V$, $V_d = 0V$)	1.24	0.32
I_g/I_d	53%	7%

Table 1 Device parameters of OTFTs with $HfTiO_2$ as gate dielectric annealed in N_2 and N_2O gas ambients

IV. CONCLUSION

Organic thin-film transistor with high-k material $HfTiO_2$ as gate insulator has been fabricated and studied. This study has

demonstrated the use of $HfTiO_2$ as gate dielectric can obtain low operating voltage and high switching speed. In addition, the gate leakage current and on/off ratio are greatly improved by the N_2O annealing. The excellent electrical characteristics of the N_2O-annealed sample are attributed to nitrogen incorporation in the gate insulator during nitridation, which can passivate the insulator surface to produce a better insulator/organic interface. In conclusion, N_2O-annealed $HfTiO_2$ is a promising gate insulator for fabricating high-performance OTFTs.

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